FUSE HANDBOOK
ON

BEST PRACTICE
IN
ASIC DEVELOPMENT

DRAFT

28.12.99

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1 FOREWORD

Successful innovation, as applied to production processes and manufactured products, today relies mainly on the adoption and combination of the following two approaches: quality management i.e. a methodology and new technologies.
Amongst the most appropriate technologies to help organisations and enterprises to widen and differentiate their markets, microelectronics is one of the most pervasive and encompassing. All technologies, and microelectronics is no exception, needs to be understood., at least in their basics. This ensures that it is properly exploited in order to prevent serious shortcomings, which are mainly economical.
What follows aims to help managers to understand the various facets of a particular aspect of microelectronics, more specifically the Application Specific Integrated Circuit (ASIC) development flow, devised, managed and controlled through Best Practice methodologies. Such methodologies, which are ever-improving, are based upon established procedures applied to real cases, which feed-back adjustments and tune the process .
Managers, who are adopting ASIC technology for the first time can find in this guide a practical description on how to approach such a development. Such a description mainly arises from the collection of methodologies and examples, showing both best practices and shortcomings coming from the experience of more than 200 European companies and about 30 TTN's that took part in the First User Action (FUSE) programme.
The main focus of this handbook is on the methodologies that are used in order to succeed in any innovation process; the technologies available, and in this case the adoption of ASIC, and some specific conditions to the general methodological rules.
Clearly this is not a technical guidebook on the design of ASICS or their technologies, it's a description of the best practice that has to be used to properly manage an ASIC project. In the next chapters, a basic description of the technical issues is provided, to familiarise the user with the technicalities of such a challenge.

This presentation, therefore, will give the Readers, in Paragraph 2, a flavour of the Asics technologies, which are the advantages and disadvantages expected from their use, and which are the problems and costs of such technologies. We'd like to stress the term "flavour", as technologies and related costs and approaches are on an ever-improving track: that means, especially for First Users, the need of competent advice and help in order to make the proper choice.
Then- in Paragraph 3- the Best Practice concerning the management of the entire ASIC development program will be described, with major emphasis on the quality procedures to follow in order to avoid the worst problems that can be encountered. In so doing, also the technical facets of the Design, Testing and Approval of ASICS are also covered.
In Appendix I we have made available a more detailed view on the technologies and the relevant information, together with tools and methods to be used for best managing a Project. Also a view of the ASICS developments undertaken in FUSE, illustrated from the applications and technologies side, is there available.
Although programmable logic devices are considered to be an ASIC, this guide does not cover such devices. However, the handbook may make reference to them. For more detailed information on such devices, please refer to the "FPGA Training Material".

2 THE ASICS SOLUTION

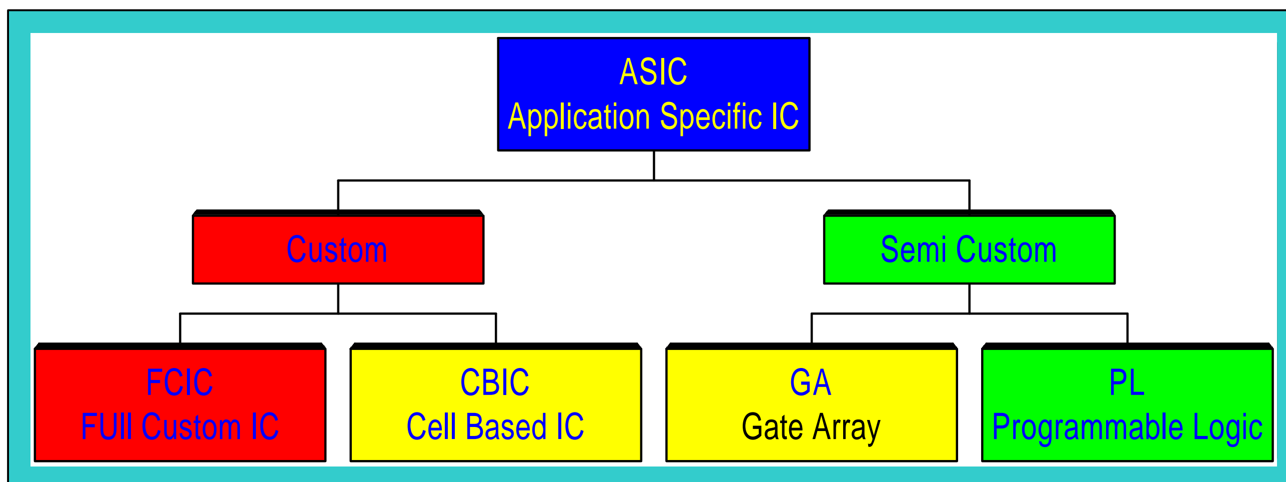
In this chapter a brief overview of Asics's Technologies, Advantages and Disadvantages for their adoption is given; also a few examples, coming from the FUSE database are presented.
To show the importance, today, of the Asics solution, a Market's overview and trend is also provided.

2.1 ASICS: TYPES AND ECONOMICS

ASIC is an acronym for Application Specific Integrated Circuit:
Integrated Circuits (IC's) are devices that implement, on Silicon or other semiconductor materials, passive and active components to perform complex functions , housed into packages presenting a wide choice in the number of pins (from less than ten to some hundreds). Usually the performed functions are analogue (such as signals amplifying and conditioning, rectifying, controlling, regulating, etc.), digital or logic (such as additions and other mathematical operations, comparison, counting, gating, latching, datapath up to Microprocessors, Microcontrollers and Digital Signal Processors etc.), mixed (such as Analogue/Digital and Digital/Analogue converters, line drivers, memories, sample & hold amplifiers, sense amplifiers, up to peripheral devices).
Integrated circuits can be found as:

- **Standard Components**: Discrete and IC's Devices manufactured in large volumes by silicon foundries, to perform standard functions, and to be used by any customers as building blocks in their design. Those devices are found and sold through retailers and representatives world-wide.
- **Semicustom and Custom Components**: Integrated Circuits that perform functions that are tailored to satisfy specific users' needs. The silicon foundries (as with standard IC) manufacture such devices according to the customer specifications and to the foundries' available technologies, for the unique use of that customer. Those custom devices are called **Application Specific IC's (ASIC)**

Asics are basically divided into two families: Semicustom and Custom.



The above illustration is the widely, and workable, accepted one: however it represents a mixed view that might be, for a newcomer in the field, a bit confusing. Please go to the ASIC chapter of the Appendix to get a more expanded view of this world.

The Custom branch is so defined because, the monolithic circuits can be customised from scratch to satisfy specific users' needs, and therefore a dedicated, complete mask set must be used for each different customer. For what concerns the Semicustom branch, only the interconnections amongst a pre-diffused array of transistors or cells are left to be defined by the user and therefore the masks that need to be developed for each customer are limited to the few necessary for the interconnection (metalisation) layers. As an extreme case of Semicustom devices, programmable logic devices do not need any customer specific processes to define the interconnection during the manufacturing stage, since interconnection can be directly "programmed" by the users through the development of

As an example, when using a Custom approach, the surface of the chip is like a blank drawing board, leaving the designer free to position and interconnect transistors and cells, resistors and capacitors in the best way they achieve the minimum occupied area with the maximum performance. When using a Semicustom approach, the designer has a drawing board (the Silicon base wafers) already filled with a predefined cells (exhibiting various functions) array. The designer then has to choose which cells to use and define the interconnections between them.

The Custom branch is divided into the Cell-based (CBIC) and Full Custom (FCIC) ICs, while the Semicustom arm is divided into the Programmable logic and Array Based circuits.

2.1.1 Custom

- **FCIC** (Full Custom Integrated Circuit): is a custom ASIC where the customer designs the cells' layout and their connections, mainly by means of handicraft work, so as to fully optimise some of their main characteristic (i.e. speed, area, consumption and linearity) of the design. Such circuits, being full custom, by definition can be designed to fit any need and do not require any validated library. However that flexibility is expensive in terms of development time, as the design is done at resistor/capacitor/transistor level, and the final result heavily relies on the designer's own skills.

  CBIC (Cell Based Integrated Circuit): is a custom ASIC that uses libraries of standard cells that have already been defined, designed and characterised by the Silicon Vendor. These cells can have different complexity, can be freely used and interconnected to build up the final circuit, but cannot be modified by the customer (otherwise it would be a FCIC). ICs that are designed by means of silicon compilers are included in this category. The cells available, and there are an enormous quantity, cover all the functions of COTS (Components Off The Shelf) of low and medium scale of integration, as well as a good number of microcontrollers and microprocessors (and peripherals) functions (IPR).

2.1.2 Semi-custom

- **Gate Array** (**G.A.**) is a Semi-custom ASIC, which is customised by the Vendor, using one or more metal layers to create electrical connections between a pre-diffused array of similar basic cells, in accordance with the user's Requirements. G.A.'s are digital devices where cells are based on simple elements, such a CMOS pair, which cannot be chosen or modified by the customer, likewise in custom devices. G.A.'s can seldom make full use of the gates available in them, mainly because of the relatively limited routing capabilities. A particular G.A. manufacturing process that has to be mentioned, due to its fast turnaround time, is the one based on Laser technology that "writes" on the last metalisation layer to personalise the chip. For those reasons G.A. are cheaper and faster to prototype, as only one operation (the interconnections deposition or "writing") is required to customise them, but silicon real estate is not optimised and the possibility of integrated analogue functions is strongly reduced.

- **Linear Arrays**, which are the analogue version of G.A.'s, are mainly based on bipolar transistors and passive cells, such as resistors and small capacitors, that can be tied together to perform the function of several linear ICs. These arrays are offered both in CMOS and bipolar technologies, the latter being more popular. Their market share is quite limited, due mainly to design difficulties. These are mostly related to the fact that analogue circuits often require the customisation of an individual function, an individual functions' customisation which cannot be obtained with a limited set of predefined transistors and passive components.
- **PL** (Programmable Logic) is a Semi-custom ASIC that is customised directly by the customer after its fabrication. These devices can be programmed after manufacturing by means of internal switches (fuses to be electrically blown or laser cut connections), which can appropriately tie a system of predefined connections with a pre-diffused array of cells.

2.1.3 Technologies

IC's and Asics are constructed from materials called Semiconductor Materials which have the correct electrical characteristics; amongst these are Germanium (Ge), Silicon (Si) and Gallium Arsenide (GaAs) which have been, and are being, extensively used. However, silicon material covers more than 99% of the devices manufactured in the whole world, while GaAs is used for niche applications where, generally, ultra high frequencies (> 1 GHz) are involved. By using Silicon, as starting material, the following main technologies, and the respective implementable functions, are attainable:

Main Technologies-Families-	Main Functions
BIPOLAR	Analogue and Digital
CMOS	Mainly Digital
BiCMOS	Mainly Analogue and Mixed
Gallium Arsenide (GaAs)	Analogue and Digital UHF

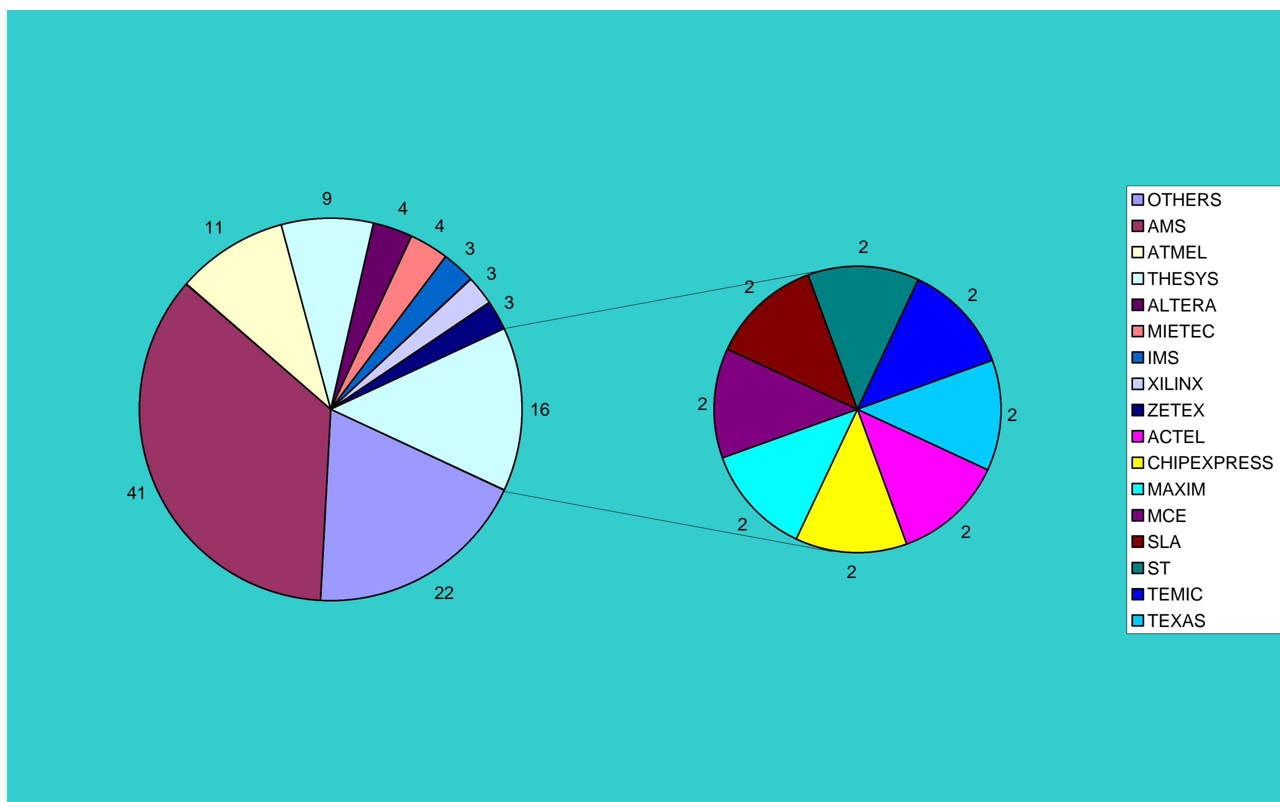
In addition to this, each of the mentioned technologies, is divided in subfamilies, according to the minimum dimensions achievable for a transistor (in bipolar technology) or its gate (the equivalent of a FET transistor's base) length in CMOS and BiCMOS technology.
Therefore a Technology is identified not only by the family name, but also by the transistor or gate dimensions: each technology has its own strong points and weaknesses in terms of performances, power consumption, speed, stability, price etc., therefore the prerequisites and limitations of the applications require a thorough analysis to identify the best technological choice and, quite often, the best compromise.
The methods to realise transistors, as well as the differences in the manufacturing process and the starting base materials, mark the four main technologies:

1. CMOS. This is a mature, silicon-based, technology (more than 20 years old) and whose limitation are still to be reached. Its main characteristics are low power consumption and low manufacturing costs. This has allowed the manufacturing of high-density chips contributing to the substantial miniaturisation and the introduction of truly portable systems. CMOS technology offers the best trade-off in terms of costs/benefits, and is offered by many reliable silicon foundries.

2. BiCMOS, is a mix of CMOS and bipolar technologies, offering a reasonable trade-off between the density of CMOS and bipolar performances. It is still a silicon-based technology, more expensive to manufacture (more than double the masks needed compared with CMOS), but offering analogue and digital possibilities, higher switching noise immunity, more bandwidth and higher driving capabilities.
3. Bipolar is a mature technology which is also silicon-based-, still used for niche applications, where very high speed and special analogue functions are necessary. Due to its power-hungry characteristics, high-density integration is very difficult and requires special packaging and cooling- down precautions. It is mainly used for small (few transistors) analogue circuits, where high bandwidth, high noise immunity and high drive (current/voltage) capabilities are necessary.
3. GaAs (Gallium Arsenide) technology: this term covers a whole series of GaAs-based technologies with respect to silicon-based devices. GaAs devices exhibit much higher speed characteristics at the price of a higher power consumption (it does not increase substantially with frequency !) and it has better radiation-resistance characteristics. Nowadays digital CBIC libraries allow the fabrication of devices well over 5 GHz with a power consumption of 0,1mW/gate. This technology has been pushed by telecommunication industries, and is also used by space and nuclear industries and organisations, due to its radiation-resistance characteristics. On the other hand GaAs has higher manufacturing costs, very few foundries world-wide, modest number of cells available and high power requirements.

A large number of silicon foundries that support ASIC development can be found both in Europe and in the rest of the world; their number and names change rapidly, as new companies appear every year or older companies, according to their strategies, develop alliances or favour spin-offs to cover technologies/markets segments. The following chart shows a few of the many ASIC foundries that have operated within . Those ASIC users that have already dealt with silicon foundries know how to find the right technology provider: however the ASIC First User requires external reliable help to find the right track.

ASICS foundries in FUSE



The following other foundries have also operated in FUSE: Alenia, Alfa, Amd, ASIC, AT&T, EKA, GMMT, HNT, Melexis, MicroE., MSC, Nec, Orbit, Plessey, Qgate, Sames, Samsung, SemeFab, Timet, Xfab, ZMD.

More than 50 different designs have been implemented using Multi-Project-Wafer runs.

2.1.4 ASICS Costs:

With the various technologies, with ever increases in performances and manufacturing processes and types, it is quite clear that prices can vary widely. There can be two updates per year to the price listings and almost as often technologies are phased out.

In general, however, the manufacturing of an ASIC have two types of costs associated to it. The cost of prototyping the first few parts in order to check them in the target environment, and the production (low or high volume) costs.

2.1.4.1 Non Recurrent Costs

Non recurrent costs are the costs incurred-in for the prototyping of an ASIC. They include:
- The costs for the chip design,
- The costs for prototyping it.

The latter cost (Non Recurrent Manufacturing) are non recurrent because:
- The masks set for silicon processing has to be manufactured just for that design,
- A non-standard flow for processing, handling, testing and packaging the devices has to be installed and controlled.

Today no silicon foundry is willing to sign a contract with a single unit price, which includes prototyping parts' costs and production costs, unless the business is really substantial (in the neighbourhood of 500.000 Euro). This is because there is always a risk of failure (small but not zero and whose responsibility may be hard to determine) in the manufacturing of the first prototypes, and secondarily because a non standard procedure has to be installed when dealing with a few prototypes. Those costs for prototyping are called Non Recurrent Manufacturing costs (NRM) and are part of the overall Non Recurrent Engineering costs.
The Non Recurrent Engineering costs, or NRE-, are typical of the ASIC approach, because they are linked with the development and manufacturing flow of the devices, leading to the delivering of a limited (usually 2 to 10) prototypes. In order to proceed with the volume production of the chips, the manufacturing and test process of the components has to be set up and then verified through a pre-production run that has to be paid for by the customer. This allow the evaluation of the conformance of the first few samples to the original specifications. In addition, especially for a first user, the actual designer of the chip usually is a third party, and such costs must be determined and included in the development costs. All those represent the NRE costs: NRE= MRM + ASIC development costs
The pricing approach (NRM) to silicon will probably decrease drastically or disappear, as it already now appears partly justified. It will probably be one of the new entries into the silicon suppliers arena that will be the first to develop a modified and advantageous-for-the-customer approach to the problem.
MPW- Currently, the Multi Project Wafer (MPW) approach has been installed and used to minimise, as much as possible, the prototyping costs, solving the problem for quite small volume production (less than 1.000 per year).

This MPW approach is based upon the figure of a broker who, having booked in advance the manufacturing of a certain number of wafers (at his own risk) in determined technologies with the silicon foundries, gathers different designs to be implemented with the same technology and assembles them on the wafers. Therefore the cost per design is shared amongst the different designs and the individual user's economic advantage is evident, also in the case of low volume production.

The disadvantage of such an approach is that the booked lot of wafers is manufactured at precise dates (2-3 times per year), which means that a user has to wait if he is not able to match the deadline for the release of the design.

The MPW approach is a good economical solution for First Users with low volume production, and it is currently supported by companies such as Imec, Fraunhofer-Institut (FhG-IIS), Nordic and Delta.

The main technologies supported today by the MPW centres and the relevant silicon NRE costs are:
CMOS- 2µ, 1,2µ, 0,8µ, 0,7µ, 0,5µ, 0,35µ with prices ranging from 130 to 900 Euro per mm^2 ,
BiCMOS- 1,2µ, 0,8µ, 0,6µ, with prices ranging from 520 to 580 Euro per mm^2.,
GaAs at 1500 Euro per mm^2.

The packages costs must be added to the silicon prices', and they range from 15 Euro for Dual in Line (DIL) 16 pins package to 129 Euro for the PGA 256 pins package.
Also the testing costs have to be added, but those have to be contracted specifically, as testing depends on many factors, such as the complexity of the chip, the kind of testing needed etc..

As an example, 10 prototypes of a 5 mm^2 chip, manufactured in 2 µ CMOS technology and housed in a 48 pin DIL package, untested, cost to the user 10x (130x5+31) Euro, through an MPW run.
The formula is straightforward: 10 is the prototypes quantity, 130 is the mm^2 price of the technology, 5 is the die size in mm^2 and 31 the price of the 48 pins DIL package.

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2.1.4.2 Production Costs

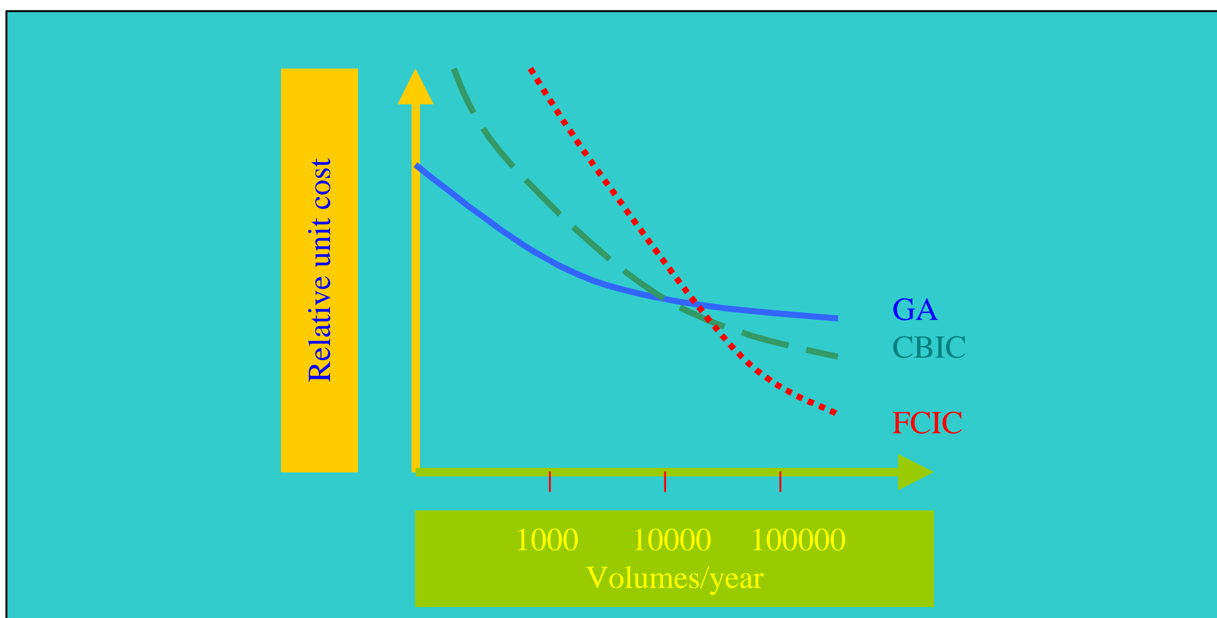
After the NRE costs there are the Production costs. These are related to the costs of series manufacturing, and they are typical of the production phase and are sensitive to several main parameters. For the different vendors those costs are mainly functions of :

A. the chip area, *Example A= 25 mm²*
B. the total quantity needed to be used, *B=50.000*
C. the wafer area (therefore the number of chips per wafer), *C=18232 mm² (6")*
D. the technology, *D= 0,7 CMOS*
E. its process yeld, *E= 80%*
F. the wafer test yeld, *F= 0.99%*
G. the encapsulation cost (per type of package and packaging process), *G=1,5 Euro*
H. the packaged devices' yeld, *I=0,95%*
I. special screenings, *none*
J. wafer test cost *J=10 Euro (4 sec/wafer)*
K. encapsulated device test cost. *K=1 Euro (4 sec/dev.)*

It is therefore important to have defined all those parameters since the early definition stage of the project, in order to get a reliable quotation and to draw a transparent and unambiguous contract with the silicon vendor.

1. Usually, each manufacturing process has established and standardised yeld: therefore E and H are fixed and known. Also F can be considered a standard value if the proper test strategies have been implemented into the design.
2. As B is pre-determined, B/ (E*F*H) gives the total number of devices that should be manufactured (Q). *Example Q= 66455*
3. Q*A/C gives the number of wafers to be processed (Wt). *Example Wt=91*
4. Wt* (cost per wafer) gives the total wafers investment (Wc). *Example Wc= 91000 Euro*
5. (Wc + B*G + Wt*J + B*K + I)/B gives the cost per manufactured unit. *Example Unit cost = 4,3 Euro.*

If the user deals directly with the silicon foundry, the unit cost for the volume production is heavily dependent on the quantities involved: an indication is given below.

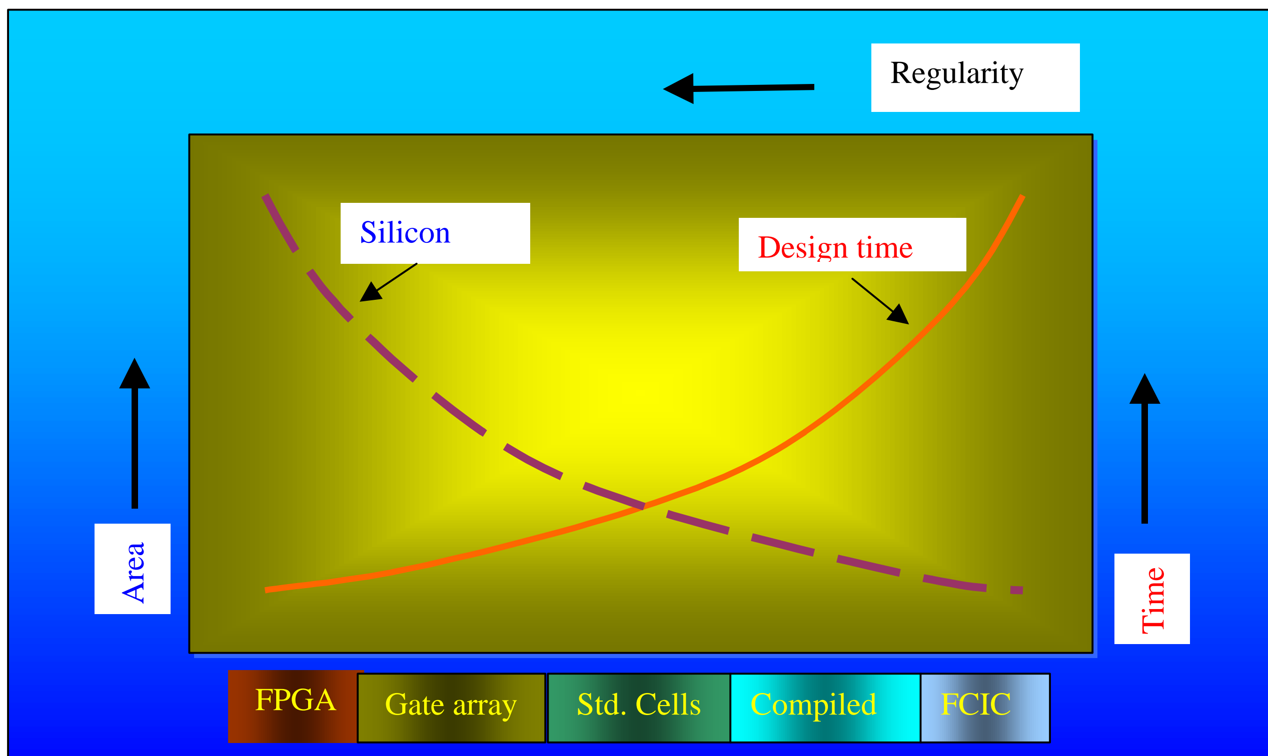


MPW services can be used also for low volumes production: in this case, a much smoother flow is to be expected, but with the advantages of a much lower starting price, which in turns gives the user the possibility of being supplied with low volumes. The manufacturing unit costs of the ASICS that have been manufactured through the FUSE program and through MPW runs , range from 1 to 80 Euro.

2.1.4.3 Overall Costs

The Overall costs for a company embarking on an ASIC design for the first time can be substantial: the internal competence at the start of the project and the complexity of the chip to-be-designed affecting the design time, while the type of ASIC, the technology and the silicon area affect the unit costs.

The following chart gives an idea of the interrelations amongst the main factors affecting an ASIC development.



The above table gives only a qualitative behaviour of the parameters: the estimated cost comes out only after performing a thorough feasibility study (see par. 3.2.1.9).

2.1.4.4 Costs in FUSE

Following is the breakdown of the total cost of innovation through an ASIC development and is roughly divided, in man-power. This table is mainly derived from the ASICS developed in FUSE and is averaged for throughout the execution phase (this phase is related to this handbook).
Relative weight and duration of the other phases come from other experiences, as very few FUSE experiments have started the Industrialisation and Production phase, when this handbook was written.

Table 1

	Time Phases	Activities Costs	
		Operative	Management
1 : 3 months	Idea conception	2,5 %	0,5 %
2 : 12 months	Execution Phase or Prototypes Development	48,0 %	14,0 %
3 : 4 months	Industrialisation & Production	33,0 %	2,0 %

Table 1 gives an idea of the personnel costs involved: to those costs, the following have to be added:

Table 2

Non Recurrent Manufacturing Costs (NRM)

CBIC devices	from 30 KEuro to 70 KEuro for prototyping of up to 10 devices
Array-based devices	from 15 KEuro to 30 KEuro for prototyping of up to 10 devices
Design assistance by Subcontractors	Between 15 and 40 KEuro

In terms of manpower, for a first user and based upon the data from the FUSE Experiments, the execution phase requires anything between 150 and 250 person-days, with such variations due to the starting technological competence of the first user and/or by the project complexity.

2.2 MOTIVATION OF THE TECHNOLOGICAL CHOICE

In this chapter the main advantages and disadvantages of using ASIC instead of other technologies, with particular attention to discrete standard devices and FPGA/CPLD, are provided.

2.2.1 Asics advantages with respect to Standard Devices

Asics can replace and integrate in a single chip standard components and their functions and in addition to this, one can design and implement on such chips special functions or groups of them that are not available, with the right performances, by standard devices. Therefore the main advantages of the ASIC approach are:

Reduction of physical parameters, such as area, volume and weight,
Reduction of power dissipation,
Performances improvement,
Enhancement in reliability
Reduction in Parts counts,
Reduction in cost-per-unit,
Overall protection against copying of the solution implemented within the ASIC, and, consequently, strengthening of the proprietary design implementation and system differentiation,
Improvement of the EMI/EMC system's characteristics.

The above listed advantages, match with the markets' requirements and expectations from new electronic systems: they have to be small, lightweight, portable, reliable, easy and friendly to use,

compatible with new applications, and last but not least, cheaper.
Such Requirements are certainly achieved by adopting an ASIC Solution. The current technologies used to manufacture Asics can also be the same as that used in the manufacture of standard components with several millions of transistors present, with a footprint of the packaged device of up to 25 square centimetres. Presently tens of thousands of gates can be integrated into a square millimetre or Silicon. Hence an ASIC solution can allow a reduction in printed circuit board's area of some orders of magnitude, with similar savings in volumes and weights.
Such miniaturisation means that the physical dimensions of the transistors and connecting lines on the chip are so small that parasitic paths are drastically reduced, decreasing power dissipation while allowing higher operating frequencies. As an example, the improvements in the ASIC technology allow typical dissipation of the order of some 100nW/MHz/gate, depending on the adopted CMOS technology. Practically this allows portable devices such as calculators, mobile phones, camcorders, portable PCs, etc.
The reliability improvement results from the drastically decreased parts count, together with the reduction in soldering joints and connections. The principle is very simple: the fewer are the number of parts and possible sources of malfunctions the higher is the related reliability.
Space, military, biomedical and transportation sectors and some environment-constrained applications require from the electronic systems a very high standard of reliability. The reliability that comes from the high integration that Asics can offer, together with the adoption of well proved technologies, such as those used for the realisation of CMOS ICs, often represents a good solution to such problem.
A reduction in the unit costs comes mainly from the replacement of a high number of standard parts with a single chip, as very often the total purchasing costs of the replaced parts is higher than the cost of the replacing ASIC. In addition, using an ASIC to replace a certain number of standard parts or **COTS** (Components-**O**ff-**T**he-**S**helf), other costs reductions are obtained, related to the systems' manufacturing process: assembling, soldering, testing, repair. Hence it is clear that replacing a single standard IC with an ASIC, unless the Company is forced to do it, (in the case of ICs obsolescence) barely provides economic benefits, and this mainly because of the higher production volume that is usually behind COTS.
Property of Design, IPR (Intellectual Property Rights) are issues that sometimes are as important as the costs reductions, as they allow a company to have a complete ownership both of the chip and of the systems' functions and architecture, giving them a head start with respect to their competitors or to the ever-present cloning companies.
The miniaturisation connected with Asics allows a drastic reduction of the electromagnetic interference and susceptibility of the circuit implemented in the chip, increasing its field of possible applications.
Due to all, or part of the above benefits, ASIC allow to create brand new products that wouldn't have been even thinkable only a few years ago. A few examples are given below:

EXAMPLES
1: Reduction of Physical parameters-
In AE 24571 the First User introduced a new "Life Guard System" to monitor children's heart and respiration against SIDS (Sudden Infant Death Syndrome), based upon an advanced ASIC. The mixed signal ASIC, developed in 13 months at a cost of 100 KEuro, incorporates many standard IC's and performs the filtering, amplification and conversion of low level ECG and respiratory signals. The main advantages arising from using that technology, besides cost reduction, come from the small size of the final system, that allows the product to have a negligible impact on the normal children's activity.
2 : Parts counts and unit costs savings-

In AE 25815 the FU, in order to reduce parts count, assembly costs and system' size, while adding extra features, developed an analogue ASIC for its Laser Control Systems, used by textile and instrumentation companies. The ASIC, developed in 8 months at a cost of 55 KEuro, incorporates a laser driver, a circuit for inhibition, reference and error amplification and a new detection capability. The cost savings amount to ca. 70% of the actual production costs, for 50.000 units/year.

3 : Performances improvement and power reduction-

In AE 23717 a digital ASIC has been developed by a First User, to control motorised spindles to be used by the textile industry. The ASIC, developed in 13 months at a cost of 70 KEuro, controls the motor's speed and the working sequences, by incorporating a microcontroller with peripherals (8 bit CPU, 16 bit timer, 8 bit PWM timer, serial interface, output encoder and sense input). The main reasons were to improve system performance (better revolution accuracy), reduce power consumption and a decrease in the noise generated.

4: Improved performances and new markets opening-

In AE 23627, the First User developed a JPEG codec ASIC that gave the company a low cost solution for the application of speeding up the transfer of images with wireless modem; in addition they will offer it , through the silicon manufacturer, on the market as a building block for application requiring temporary storage or transmission of image data. The development of the chip required 12 months at a cost of 97 KEuro.

5: Sector's new standard -

AE 26552 is based upon the innovation of an electrical frying pan in which, up to today, no significant electronics have been used. The proposer developed a digital ASIC to allow a friendly interface (a touch pad and numerical display), a better temperature control which consequently added a new "simmering" facility. The proposer, by attaining technological leadership in the field, estimates not only to stop its market share's erosion by low cost eastern manufacturers, but to double its share in a conservative five years period. The ASIC, developed over a 12 months period with an expense of 76 KEuro, is a simple one, occupying a silicon area of less than 5 mm^2.

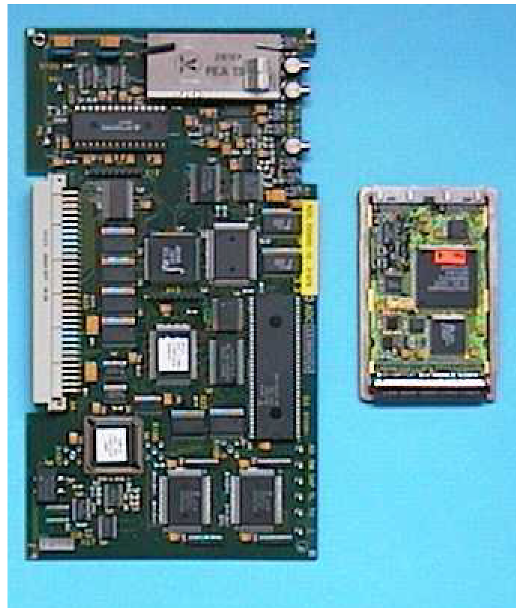
6: Size and cost reduction-

AE 22895 developed a digital ASIC, taking 10 months at a cost of 101KEuro in Gate Array technology to integrate the many digital functions necessary for their hand held ultrasonic tester. The need for the ASIC derived from the necessity to use PCMCIA Card, which has very small dimensions, and in the process they obtained a tenfold reduction of the costs of the overall functions implemented into the ASIC. The size and power reduction obtained is 1:5.

7: Low power: many Application Experiments have resorted to the ASIC solution to decrease either the power supply voltage or the power consumption in general. Just two examples are here given.

AE 22842 developed a digital ASIC to make electronic pricing labels to be used in shop windows. Each label has its own battery and the size of the label has to be maintained equivalent to the existing ones. Therefore the use of Low Power ASIC is mandatory.

AE 22876 developed a Mixed ASIC to make a battery operated hearing protection unit. For size reasons(the hearing protector must be worn by the user) and for battery duration, Low power technology was used.



In Fuse, all the advantages mentioned at the beginning of this chapter are given as justifications for the experiment's undertaking: however, a careful examination and interpretation of the available documents allows to get a feeling about the real issues that have determined that choice.

By far, the unit production cost of the ASIC appears to be the most mentioned justification (> 90%), followed by the performances improvements, including EMI/EMC characteristics,(> 70%) and the production and post-production savings- from inventory, PCB and overall system size, test time, assembly and repair, field maintenance, etc- (> 60%) . Low power requirements represent an exclusive condition in the 10% of the ASICS AE's.

2.2.2 Asics Disadvantages

From what has been already discussed, it is apparent what the disadvantages connected with an ASIC development are, some of which are general to any innovation process, a few peculiar to the technology. In the following list, the latter are discussed:

Availability of skilled designers and up-to-date SW CAD Tools,
Limited allowance for last minute changes,
Development, or prototyping, costs still high,
Delivery time,
- Risks connected with the SW tools, with the change of usable technologies, with personnel turnover, and, in general, with the unfamiliarity of a first user with the ASICS matters.

Whether a Company, who is to develop an ASIC , undertakes the design internally, or commits the development to an external design house, there is always the need to have people in-house that understand at least the pro and cons of the various technologies and methodologies, as well as the overall system's requirements. This is necessary in order to successfully manage and to efficiently interface with all the resources involved in the project. Furthermore, if the Company wants to develop the ASIC in-house, an engineer who has been trained on the CAD tools to be used, as well as the appropriate hardware and software tools, and for the former the costs can be quite high.

Last minute changes, although always possible, can be very expensive (in terms of time and money)

depending when, in the design and manufacturing flow, they are requested. If the changes are requested at the beginning of the design phase, especially when a behavioural design approach is chosen, the caused delay can be calculated in hours or days. If changes are requested when the manufacturing process has started, that may well mean doubling the total effort (time and money).
The conclusion is that design should start only when specifications are definitely fixed and the software tools and libraries are agreed upon and available.

As it is explained later, the prototyping of the first few Parts, necessary to verify the success of the implementation, is expensive, due to the fact that the Silicon vendor has to be paid for the dedicated processing of the silicon. It also includes the fabrication of a dedicated Mask set, which represents one of the highest costs for the fabrication of a silicon chip. Such Non Recurrent Engineering costs (**NRE**) can be sometimes distributed evenly on the future volume production or attenuated, by choosing alternate routes (see later) for the prototyping, but they are always taken into account as they are never negligible.

When using COTS, once the design is frozen, to receive a prototype is just a matter of procuring the parts and assembling them. Therefore such process can be very quick, and also the transition to the production phase once the prototype has been tested and if necessary fixing the problem is also quick. When developing an ASIC, once its computer based design has been validated, the silicon foundries' time to manufacture has to be accounted for, and the testing of the prototype has to be very thorough before committing to the full production of the chip. Then, again, one has to wait for the Silicon Foundries' time to manufacture the first volumes. There is a delay due to foundries' time to manufacture the first volumes, also in the case that the prototype conforms absolutely to the initial specifications and no corrections or add-up has to be implemented.

Risks connected with the ASIC approach, beside those that are typical of any new design in any new technology, are mainly connected with the disadvantages listed above. Despite the usefulness of the SW tools (and their continuous refinements and updates) and the use of well assessed technologies there's roughly a 5% probability that prototypes of digital Asics's do not work at the first trial, and for analogue or mixed ones such a likelihood is often worse. Very often, especially for digital Asics's, the main source of errors can be identified in ambiguous specifications that lead to failures once the components are placed in the final system.
But the major risks, that will be examined later, are those not connected with the technology but coming from the overall management of the project, especially those stemming from the interfaces amongst the various components of an ASIC development program.

EXAMPLE 1: Problems arising from choosing obsolete Technologies
AE 2032 aimed to develop an ASIC to allow the application of the C51 microcontroller family throughout all the company's products, in practice a company standard interface chip. This would have saved inventory costs, together with a simplification of the current and future architecture, a reduction of size and production costs.
They reached the expected result in terms of prototype availability, but they cannot go into volume production of that chip because the prototype technology has been phased out. If they now want to go to production, they have to redesign the device in a current technology with all the costs associated with the new design and prototype cycle.
EXAMPLE 2: Problems arising from choosing obsolete CAD tools
The same AE as above would have not incurred this problem if the supporting design house had behavioural design capability: this would have allowed for a less traumatic retargeting of the design to a current technology, for which NRM costs had to be paid for..

EXAMPLE 3: <u>Problems connected with last minute changes to the initial design architecture</u>
AE 516 developed a Digital Asics to be used within an Electrocardiograph: the duration of the AE 516 developed a digital ASIC to be used within an Electrocardiograph: the duration of the Project was estimated to be 12 months but it took nine more months to be completed. Most of the delay was due to the fact that during the Design phase a standard device with better performances than the proposed ASIC, was presented on the market. The proposer asked its design subcontractor to upgrade the original design with a more powerful macrocell that the subcontractor indicated was available, while it was not and which had to be developed and tested.
EXAMPLE 4: <u>Problems connected with personnel turnover</u>
The same AE 516 experienced the Project Leader's resignation in the middle of the experiment: almost three months passed before the replacement could take full charge.
EXAMPLE 4: <u>Problems connected with delivery time by external suppliers</u>.
In AE 23717 the First User had a delay of about three months. The problem was generated by the development of another part of the system's design, and precisely by the development of a brushless micromotor. The latter which was built abroad, was not part of the FUSE AE funding scheme but it was essential for the completion of the product innovation . The First User chose that manufacturer because few companies in the world could provide it and because of their previous positive experience. But the First User had to wait the availability of the motor prototype to be able to end the test of the board with the FPGA prototype. This test was considered essential before performing the ASIC synthesis and layout, the motors delayed delivery caused a similar delay in the retargeting of the FPGA to the ASIC manufacturing.

ASICs represent today an ever growing demand by the electronic industry, being developed and used by an increasing number of small and medium industries, allowing for a growing number of applications where the advantages are far more significant than the disadvantages.

2.2.3. Main overview of Asics's versus FPGA/CPLD

(see also the FPGA training Material)

This paragraph provides an overview of the main benefits and constraints of the ASIC solution, including the advantages or disadvantages of ASICS with respect to programmable logic. These figures are useful to have to hand when an ASIC solution to a problem is considered, but they can only provide an indication that should always be weighted against the particular kind of design and the ever changing technological offer.
With respect to Programmable Logic (PL) such as FPGA and CPLD, ASICs are faster, smaller and consume less power since they only use the necessary implemented resources, and do not have the parasitic capacitance that PL use to create the internal interconnections. PL vendors are offering more and more dense devices, however ASICs can generally offer greater density, since they waste less silicon on interconnections. The state of the art PL's can offer hundreds of thousands of gates versus the millions ASICs can. In evaluating the complexity, attention must be paid to the number of logic gates that vendors of PL offer, when compared to "ASIC gates". Usually these are a factor of three to five times less dense than those of ASICs, because of the utilisation of the PL's internal resources.
Unit costs for production volumes are lower for ASICs especially if devices with more than ten thousand gates are used. However, the lower the complexity or the smaller the volume the more competitive that PL devices are.
In fact, PL unit prices increase almost exponentially versus their complexity, while the possible price decrease for high volume reduces linearly.

Another advantage of ASIC devices is that the package that is chosen may well have smaller dimensions than its PL equivalent, and only has the number of I/Os that is actually required. Very often, especially with complex PL devices, only large packages with hundreds of I/Os are available, in order to optimise the manufacturing cost of such general devices. Using ASICS, PCB costs can therefore be reduced accordingly to the reduced number of strictly necessary I/O. Analogue functions and different technologies can be integrated or are available with Asics's, whilst, apart from few and simple programmable analogue devices, such functions and technologies are not available with PL.
However Asics's present some disadvantages such as NRE costs that are not present for PL, because the latter can be customised directly by the customer. This fact makes also PL more flexible especially when designs are subject to changes or to errors, for instance when a product is not yet consolidated or during the prototyping phase. PL can be programmed and reprogrammed several times, whilst ASICs cannot. This, together with the absence of NRE costs, makes PL's less risky than ASICS and also allows for any last minute modification the customer requires.
The appeal of PL to the First User is that a FPGA can be bought off the shelf, avoiding any discussion or negotiation with the silicon foundry.
Furthermore, as it will be explained later on, if the proper design methodology has been chosen to customise the FPGA, and if the required volumes ramp up, the same design can be easily retargeted to ASIC. This effectively zeros the design times and costs, leaving only the NRM to pay for.

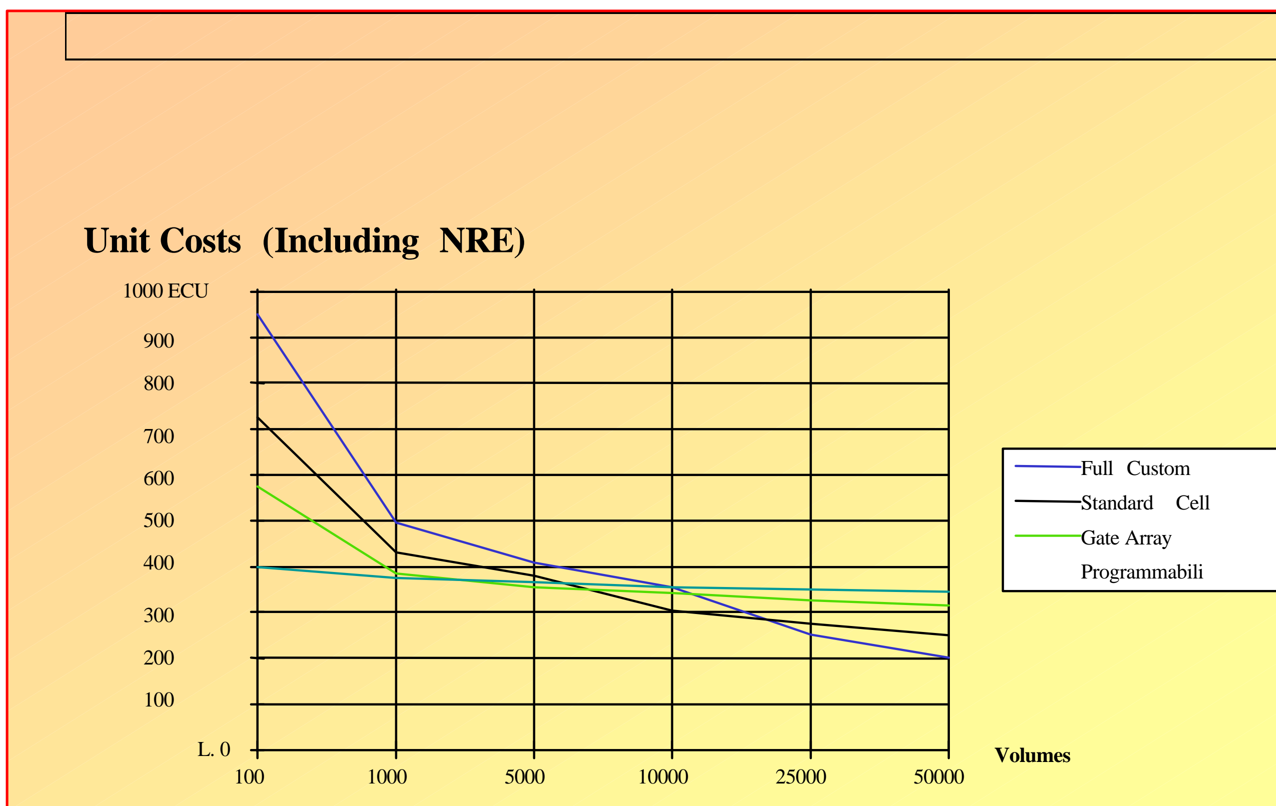
The next table summarises the main characteristics, such as speed, power consumption, costs and other parameters between the different technological solutions (COTS, ASIC and PL) considering different design and applications requirements, and assumes a design with a complexity between 10 to 50 Kgates.

Parameter	DISCRETE (COTS)	PL	ASIC
Speed	Limited	Good	Optimum
Density	Limited	Acceptable	Optimised
NRM	None	None	High
Unit Costs (per system)	High	Acceptable	Low
Design Time	Shortest	Short	Long
Development Time	Long	Short	Longest
Risks	Very Limited	Almost non-existent	Existent and Consistent
Last Minute Modify	Easiest	Easy	Difficult and costly
Power consumption	As COTS require	Reduced	Lowest
Analogue capability	Unlimited	Not Available	Available
Other functions availability	Almost unlimited	Quite limited	Ample choice
Technologies	Almost unlimited	Only one	Ample choice
PCB Dev. Costs	Highest	Medium	Lowest
Dimensions	Largest	Medium	Smallest

The next table illustrates, for the various ASIC types, the different features.

Parameter	Full Custom	Cell Based	Gate array	PL
NRE	Very High	High	Medium	Very Low
Design Time	Very High	Medium	Medium	Very Low
Last Minute Mod.	Very Low	Low	Low	Very High
Unit Costs	Very Low	Low	Medium	High
PCB costs	Very Low	Low	Low	Medium High
Density	Very High	High	Medium	Low
Performances	Very High	High	Medium	Low

The next table gives the approximate Unit Costs Vs. Volume and for each ASIC Technology .



2.3 THE EUROPEAN ASIC MARKET CONSUMPTION

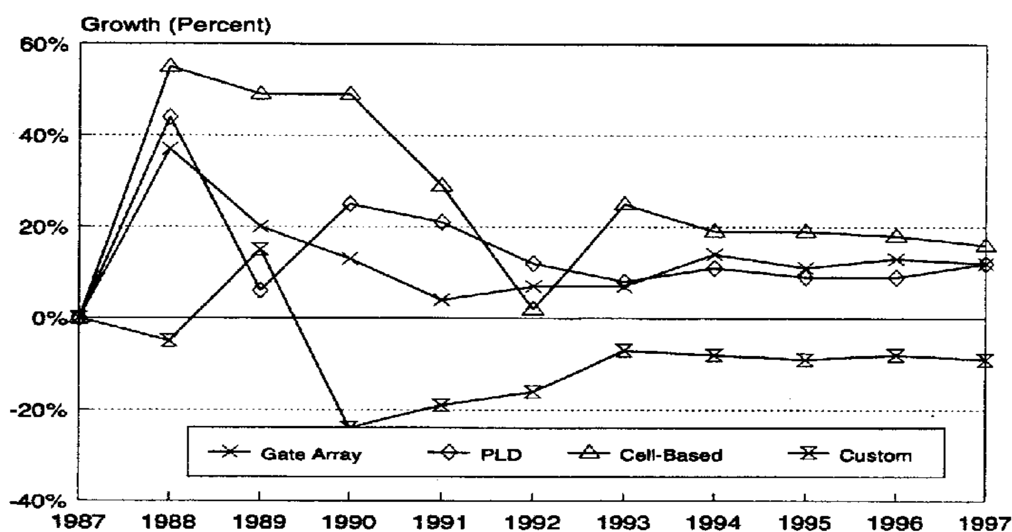
2.3.1 Market trend

Looking at the whole Asics's market for Europe, Analysts foresee a conservative doubling of that business in the years between 1995 and 2000 (from ca. 2.2 B$ to ca. 4.6 B$), based upon the fact that, from 1992 to 1997, such market has shown a 13% compound annual growth.
Europe represents a steady 15% of the world-wide ASIC market consumption.

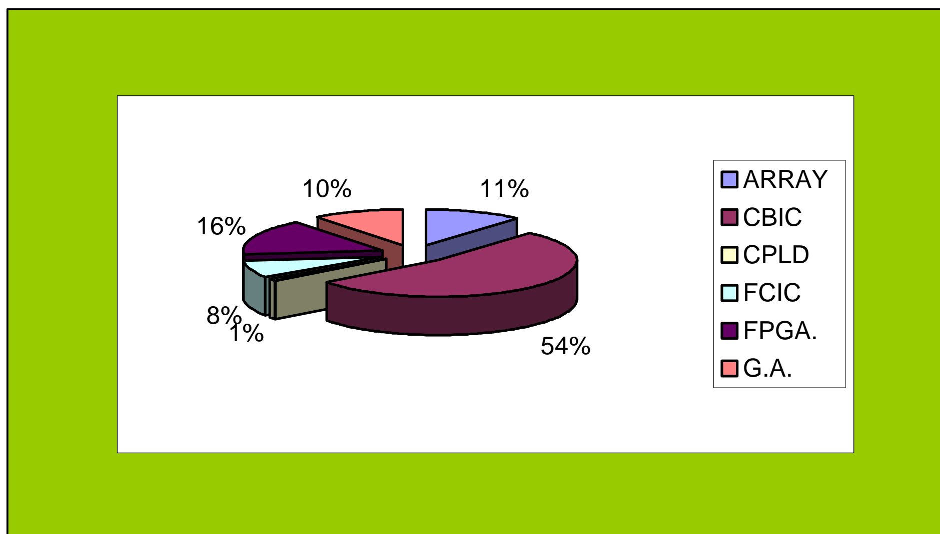
In the past few years, due to various initiatives offered by the European Commission, such as the Special Actions for the less technologically advanced regions, Jessi SME, Chipshop and Europractice and especially the most recent FUSE Project, many more Industries, especially SME's, have started to develop, alone or in conjunction with supporting organisations, their own Asics's: between 1996 and 1998, more than 200 different designs, mainly from SME's, have been successfully executed in FUSE. And that gives at least an idea of the potential growth connected with that business

Of the products that comprise the ASIC market, cell-based (CBIC) is the only one that has grown above the 13%. While much of the CBIC growth is from mixed signal applications, digital CBIC show a good long term growth as specialised functions are continuously developed and made available.
The Gate Array market shows the second highest growth, and will maintain its position as the second -largest product area in the ASIC market.
PLD, over the period, have been relatively weak, but the quite recent introduction of BiCMOS arrays is allowing an annual compound growth of ca. 13%, with a forecast of ca.20% for the year 2000.
Custom devices show a major decline, as most custom design are displaced by cell-based or gate-arrays designs.

TABLE 1



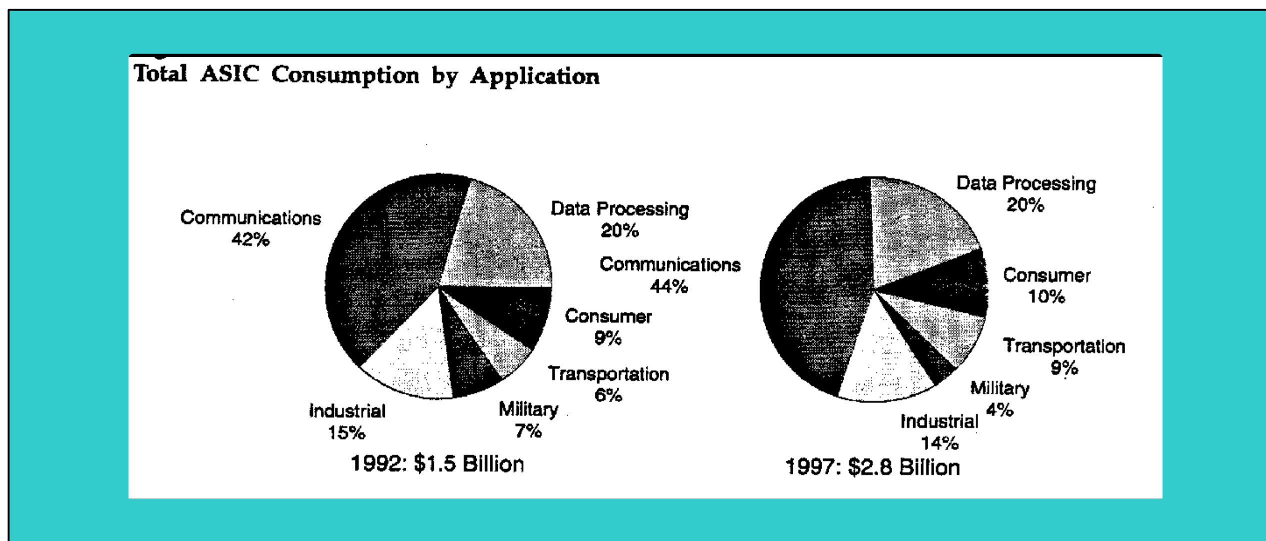
ASICS types in FUSE



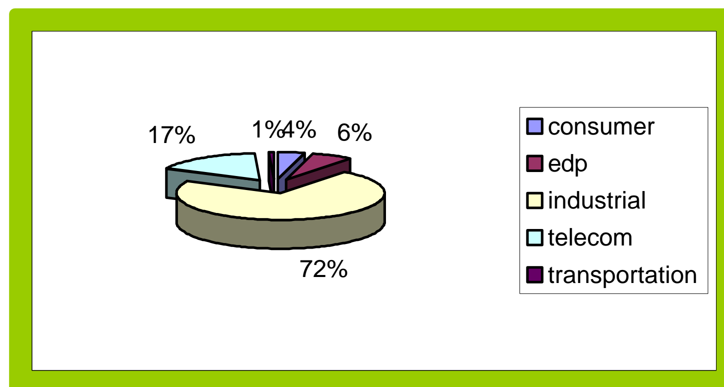
2.3.2 Market share by application

For Europe the leading sectors in the use of Asics's are Telecommunications, with a share of 44%, Consumer (15%), EDP (15%), Industrial (12%), Transportation (9%) and Military (4%).
The Consumer market is the most rapidly growing sector in the very recent past.

TABLE 2



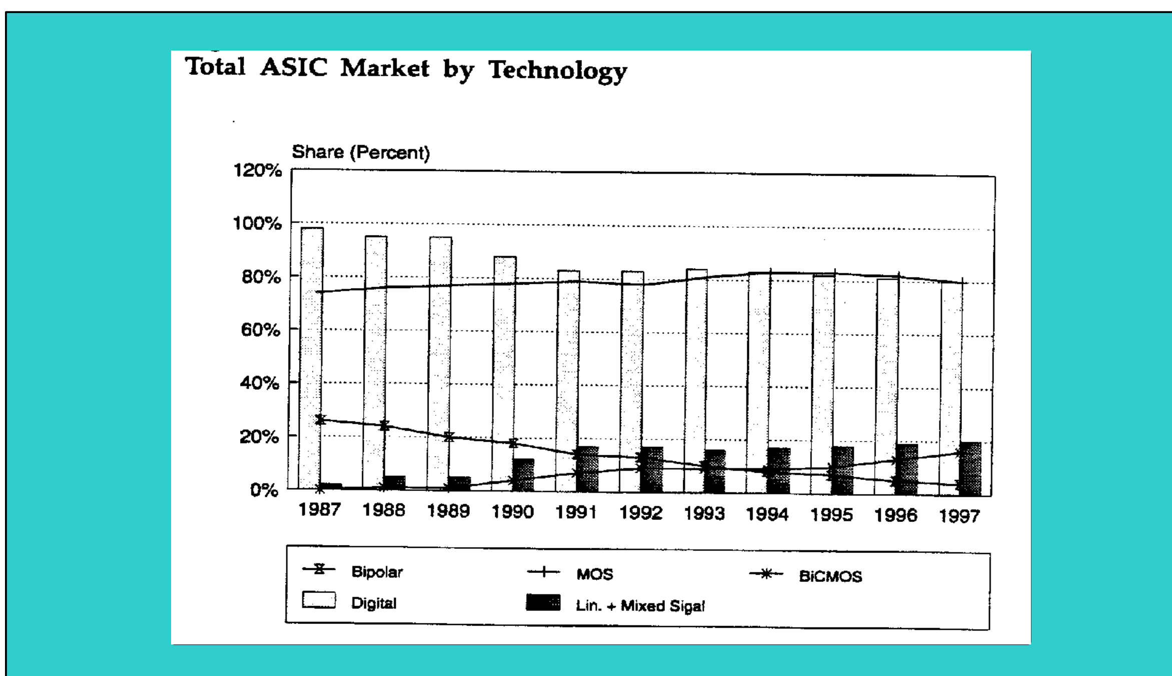
In Fuse the following has been verified:



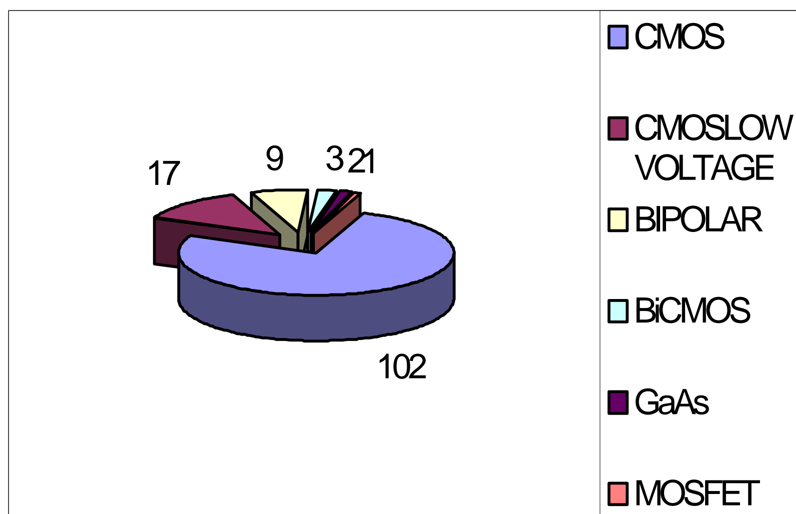
2.3.3 Market by Technologies

CMOS is still the preferred technology, although BiCMOS products are being used more and more. BiCMOS is inherently more expensive and so is used mainly for high performance and analogue applications. The performance advantage gained through the use of BiCMOS is relatively short term, though; CMOS performance generally catches up with BiCMOS given time. Currently a 0,7-micron CMOS process is cheaper than a 1,2-micron BiCMOS process, but offers similar performance. The net result is that the decision can be a difficult one, and as the time is the biggest advantage gained through the use of the more advanced BiCMOS process, this can prove to be expensive.
Bipolar Asics's are declining significantly, as CMOS performance matches most of the demands of existing bipolar solutions. The number of applications where only bipolar offers the required solution is declining. BiCMOS is furthering this decline, encroaching even more on the high-performance end of ASIC applications. The only two benefits offered by Bipolar are higher switching speed and flexibility of the analogue capability; but, for the most difficult cases, a BiCMOS or CMOS solution meets the demand of the application.

TABLE 3



Technologies in FUSE



2.3.4 Emerging applications

Some areas are beginning to show a potential for high volume ASIC sales, but the future of the applications is uncertain. Among these is image compression.
The development of visual communications is proceeding apace, but the amount of data associated with an image is huge. To make the manipulation of these images manageable, compression of the image must be sought after. Image Compression application can be found in the transmission of still images, but the greatest opportunity is in the transmission of moving images.
Initially, the development of the equipment will rely heavily on the ability of the ASIC to provide the required performance, as volumes won't be sufficiently high to make a standard product solution cost-effective. There is also the uncertainty of the transmission standards to suggest that the ASIC solution is the optimum, as pre-emptying the standard with an ASIC can attain an early success chip-set. Adjustments can be made later, but the early adoption of some proposed specifications can gain several months in the crucial time-to-market issue. The risk associated with this approach is high, though, as the wrong choice of standard can be costly.
Other speculative, but potentially rewarding ventures include data encryption where, again, an early understanding of algorithms can reap rewards in their implementation later.
In FUSE, AE 23627 has developed an ASIC just for a data encryption application; however most of those applications are addressed by experienced users only and therefore do not appear in FUSE

Low Voltage Issue**:** The growing use of portable equipment is putting more pressure on the power budget available to devices. While greater integration reduces the chips' count, and hence drives the demand for larger chips, the greatest saving in most portable equipment is in reducing the number/weight of the batteries needed. Higher integration can contribute, but the greatest saving can be made through reducing the voltage. Standard components have already appeared which operate at lower voltages, pressurising ASIC suppliers to lower the operating voltage. It will be still some

time before 3.0V or 3.3V will be the standard, but the trend is inevitably towards lower voltages technologies.
In Fuse 17 Experiments made use of Low Voltage technologies(see Appendix).

3 THE ASICS DEVELOPMENT FLOW.

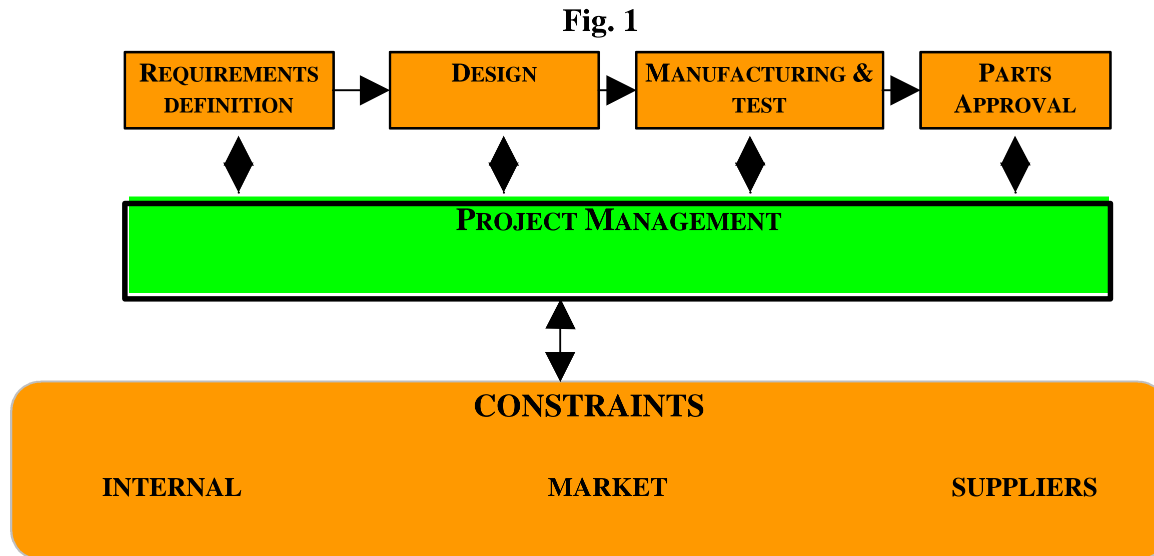
This chapter is the core of the handbook, the introduction gives a brief description of the essential phases relevant to any ASIC development project, to become accustomed with the specific activities and the main issues that affect the project.
One section has been included to explain and emphasise the role of the Technical Manager (or Project Leader/Manager) as these skills, managerial preparation and a Best Practice attitude rely the project' success. Then, with reference to a typical ASIC development flow, all the activities are described.
Relevant examples from the FUSE database are provided.

3.1 INTRODUCTION:

Any Innovation Process starts after the following three checks:
1: The company's top management is already convinced (by competitors' products for instance) that production problems or market needs require the upgrading of the production processes or products offered,
2: A technical/ technological solution (Hardware/Software) for the problem already exists or can be developed,
3: Such solution is economically consistent with the company's possibilities and expectations.

Points 2 and 3 make up what is called "Pre-Feasibility" study, which is carried out by a trustworthy delegate (usually a Company's employee, who can use internal/external resources to acquire the necessary data) of the top management. This pre-feasibility study consists in a sufficiently detailed assessment of the possibilities to find at least a couple of technical solution and their rough cost estimate.
Based upon the pre-feasibility study's indication the top management decide if there are grounds to investigate further on one solution.
Usually this nominated person becomes the manager of this project, and sometimes the technical innovation consists of the development of an ASIC.
All what follows, therefore, is based upon the assumption that the pre-feasibility study had convinced the decision makers that ground exists to determine exactly if an ASIC development project can be launched. In Fig. 1 the necessary flow to follow to decide if the ASIC solution is actually correct and what has to be done to reach success is shown.

Fig. 1



Sometimes the complex of the above activities can be called "execution phase" although the final go ahead depends on the outputs of the requirement definition phase.

In the figure shown above, the constraints and limitations imposed on the project are by the company itself, as well as by the external suppliers and market. These are reported, as this information represents the starting hypothesis for the whole project and they are the main factors against which to assess the whole feasibility.
This information appears to affect only the management task, but actually it is the responsibility of the project manager to transfer, judiciously, the necessary information to the other tasks. This is because all the parties involved in the Project should know what it is necessary, in order to properly carry out their job. This information also has intrinsic involvement and motivation properties, which favour mutual understanding and support.

- Amongst the internal constraints, resources availability is one the most important. Where Resources include manpower, in terms of sheer workforce and quality of it (i.e. competence and motivation), financial (i.e. the availability of the proper amount of money at the right time), and HW and SW instrumentation. Other typical internal conditioning come from the production floor and its flows and technologies.
- The market, in turns, impose conditions on the selling prices (i.e. production costs), time-to-market deadline, performances and functionality.
- The suppliers can present limitations and constraints, as they have their own interfacing procedures, their delivery times and terms and conditions of payments and which presents a difficult to control provider.

The management task, whose responsibility is assigned to the project manager, has as inputs, the previous constraints and all the other information provided by experts, internal and external, in the different sectors. The only output from this task is to define, implement and control a successful program, to get a correctly functioning ASIC in the right time and at the right cost.

- The Definition Phase or Requirements Definition Phase is the MOST important one as it is upon its outputs that the fate of the project is based. In fact this Workpackage groups together many different activities with only one objective: <u>to assess if it is worth to adopt the ASIC technology</u>, through the analysis of the associated risks as well as the time and resources needed. It is within this phase that the ASIC's final specification is defined, that the possible external suppliers or

subcontractors are chosen, the ASIC trade-off is performed, the risks' are assessed, the interfacing procedures defined, inside the company and towards the external suppliers.

Sometimes this phase's result contradicts the pre-feasibility study, re-routing the search for the actual solution to different alternatives.

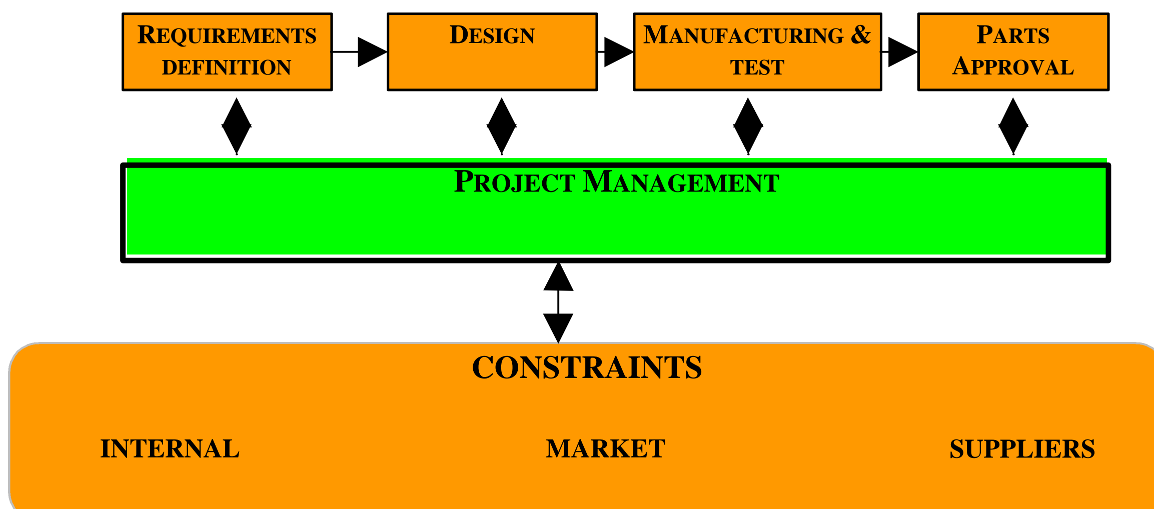
- The design phase is a purely technical task, whose purpose is to transform the paper based ASIC' specification into software instructions for the mask set fabrication, required for the actual manufacture of the chip, and its testing strategies and packaging.

. The manufacturing and test phase represents the activities, usually commissioned to external suppliers, necessary for the fabrication and testing of the chip. When the activity is commissioned outside, very little operative effort is requested from the commissioner, but it is in this phase that sometimes the interfacing between the commissioner and the suppliers is put under stress, and the managing capabilities of the project manager are measured.

- In the part approval phase, the actual performances and functionality of the devices are verified on an environment as close as possible to the final application. These tests may include quality and reliability tests. This involves the designers and the foundry, as this phase is the one that measures the real success of the project. As it will be explained later on, the manufacturers test the devices, both at wafer level and as finished parts, with stimuli (test vectors) developed by the designers of the chip during the design. If the test vectors, and the Design For Test (DFT) strategies are used throughout the design, there's a very high probability (> 99%) that all the possible defects are screened in the device supplied to the customer. However, as the number of stimuli is limited, testing the device in its target environment is mandatory, before approving the parts.

3.2 PROJECT MANAGEMENT

Fig. 2



From Figure 2, the central and vital role of the management task can be seen. It is the manager that has to find an agreement between the different kind of constraints with the technological possibilities, finding the right solutions at the right time and at the right costs.
The project manager has to impose the use of reliable project and design procedures that can be adapted to any new situation, due to the demands of an ever more competitive market as regards quality, documentation and communication. This requires to study, devise and implement project and design methodologies that reflect and take into account the relationship between designers, manufacturers and end-users, and to consider the ASIC within the context of the system in which it is to be placed.
The manager's role is not an operative one in the strict sense, as this person doesn't actually design or assemble or purchase, but it is the glue of the project, and if the glue is not that good, the various project pieces can fall apart.

Ideally an ASIC Development Program Manager should know:

- The system's requirements, in terms of overall performance, size, weight, power consumption, ambient temperature, reliability, etc.,
- The overall expected production costs, particularly those connected with the use of the ASIC- i.e. the expected cost of the assembled ASICs pcb.
- The company's, or subcontracting Companies', assembling/production/testing processes to make the correct action in the case of incompatibilities with some of the requirements.
- How to get, directly or indirectly, internally or externally, reliable information/services about any issue outside his direct experience, but necessary for the project.
- How to manage and motivate different people, not necessarily all of them employees of his company.
- The tools, methodological and operative, to properly plan the activities..

This because he has the following responsibilities:

1. After being placed in charge, a preliminary project (the feasibility study) should be formulated to be approved by the upper management, involving all the necessary groups of people,
2. After the approval of the feasibility study, in a short time, the execution plan should designed.
3. The manager has the full responsibility, on behalf of the participants in the project, of the results, therefore a control procedure should be implemented.
4. He/she has to act quickly to overcome crisis's, idling, stops, and problems in general.
5. He/she has to propose the rationale to any modifications to the original execution plan.
6. He/she has to keep the team informed, involved and motivated.
7. He/she has to suggest, if it is the case, the cancellation of the project in the interest of the company.
8. He/she is the main interface to the customer (the company), to the suppliers and any external organisation or individual.

He helps to devise, to implement, to maintain and to control the whole Project through a minute breakdown of every activity or Task, its links and dependencies from other activities, its objectives (technical, economical, time related etc.) definition, its inputs and outputs, the participants and who leads, who checks how-what-and-when, and a proper documentation preparation and maintenance. The manager is the depository of all issued documentation related to the project.

The methodology that should be used is based upon the quality management, which includes

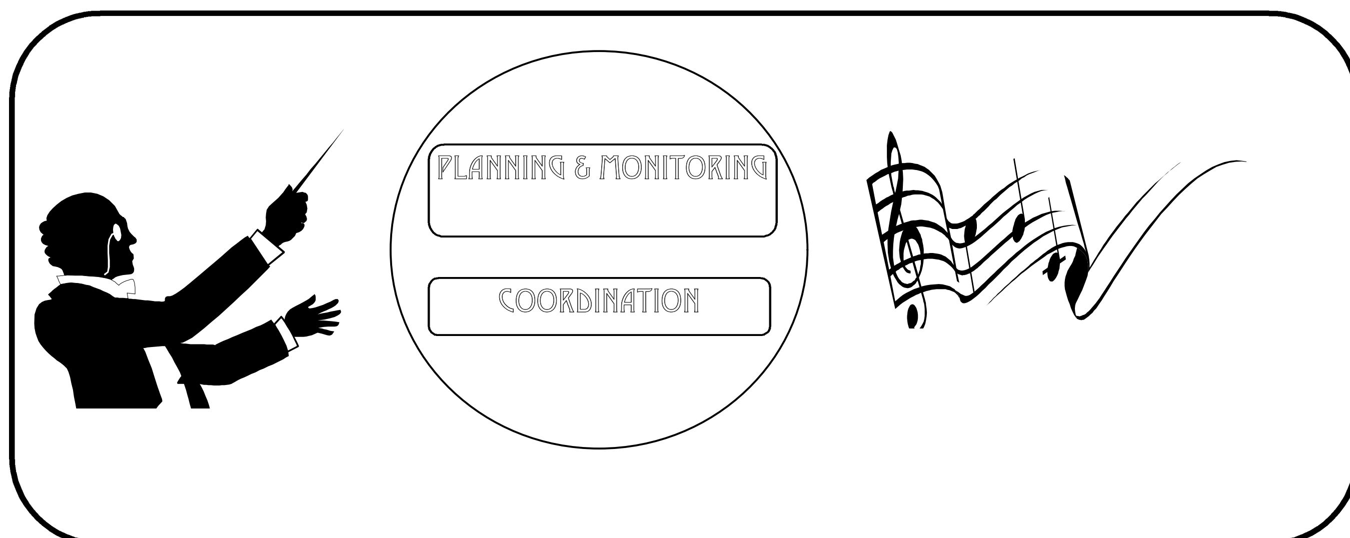
Process Analysis, where each activity or task is described minutely by its objectives' identification. It defines the needed inputs, which and when will be the expected outputs available, who must participate and who is in charge of checking.
Planning tools should be put in place, together with the instruments to monitor and control the whole flow of activities.

A thorough description of planning tools and methods, process analysis and monitoring techniques is provided within the APPENDIX.

In summary, the manager leads the entire project, especially the Feasibility Study (in the definition phase), where he/she represents the customer, and which includes the ASIC designer(s) as adviser, and any third party that has to be involved. As leader of the project, the project manager has to be able to motivate and, in the same time, control the work through the Review and Milestone meetings. At these meetings, it is the managers' responsibility to devise the agendas, to identify the necessary and useful attendees, and to record the outcomes in the relevant meetings' minutes.

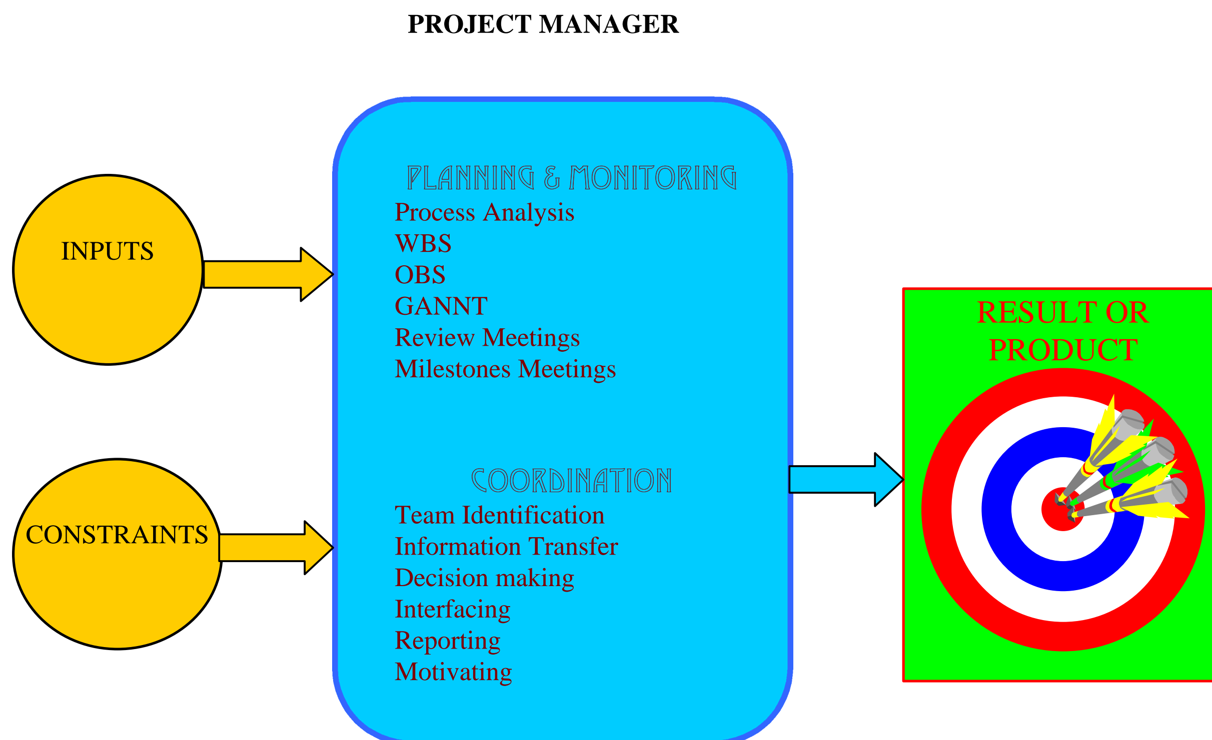
The project manager is the leader of the whole project, and his/her motivation, involvement and managerial capabilities are a paramount factor for success; it is not necessary for him to have a great deal of technical competence. Others, with more specific experience can be delegated to lead particular activities, and his/her main job is to make the whole project transparent to the upper management. To make its operation as smooth as possible, without dangerous idling or overstressing phases of work, trying to reach the best compromise between economy/time and efficiency/effectiveness.

The Project Manager's role will be further defined throughout this document.



Or, in other graphical form:

PROJECT MANAGER



Some examples of project management from FUSE projects :

AE 240 developed an ASIC (Gate Array) for video scaling in multi-image displays.

The user says that "The project management experience gained was really useful. The first user had never previously managed a project in conjunction with 2 sub-contractors. This is particularly significant when one considers that one of the sub-contractors was providing design services and expertise in an area where the first user had little prior knowledge.

The planning of the AE was a useful experience since it required the generation of a detailed work plan containing milestones and deliverables. The first user would normally have produced a far less detailed work plan for an internal development project so it was a new experience in producing the technical annex for the experiment………

The AE also involved the generation of a detailed ASIC design data sheet. This is similar to the IC data sheets that semiconductor companies provide with their products."

The Company also adds: " It is difficult to keep track of a project if it's specification changes but the changes are not reflected in the work packages set out in the technical annex. The danger exists for the project to go out of control because the deliverables may have changed or their delivery dates may have altered. This is mostly to do with good project management discipline."

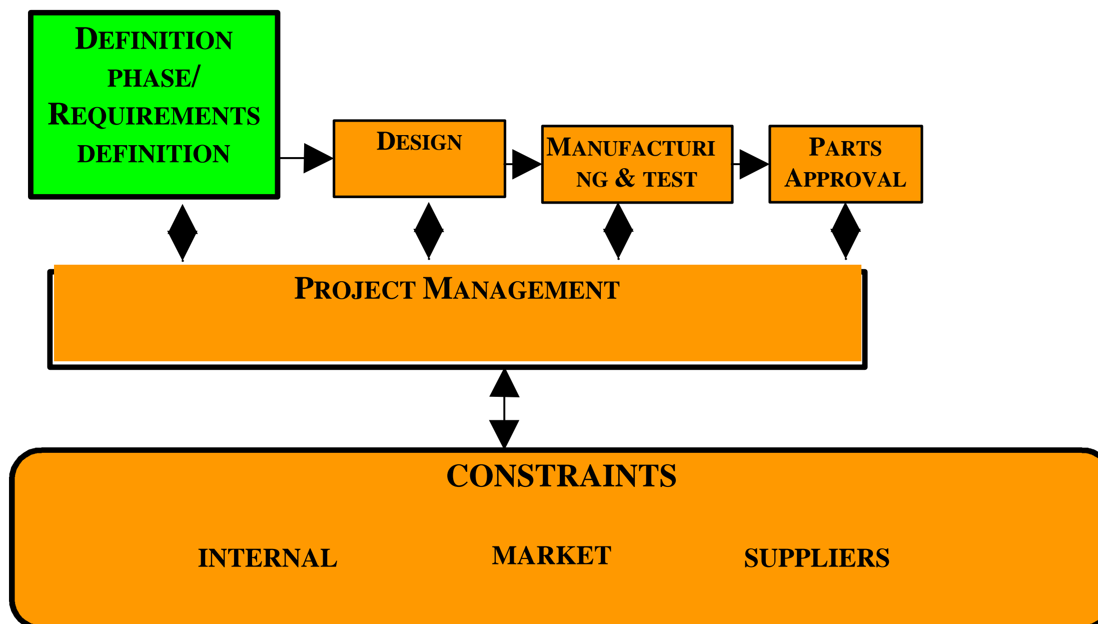
AE 23295 refers that " **….***Since the beginning of the project, ongoing activities were* <u>*constantly monitored*</u> *to ensure that they were in line with the scheduled planning. When required, corrective actions were taken to solve pending problems and to avoid delays*

After a few months, it however resulted that the design activities were evolving in such a way that it was more and more <u>*difficult to comply*</u> *with the original Work Package breakdown. After a discussion with the relevant subcontractors, the following problems were identified ….*

To minimise the previously identified problems, besides to allocate additional resources to recover the existing delays, a Work Package breakdown revision was considered mandatory to reflect the more effective design approach that had been identified (namely, use VHDL in a "bottom-up" way to meet the informal specifications resulting from the Architectural Design and Detailed Design phase). This later resulted a sound choice, permitting to recover some of the initial delays and to get anticipated synthesis results, which in turn made possible an optimised design (6K gates against the planned 10K), a very important element in our cost-sensitive context."

From AE 23295 *yet: " No dedicated Work Package or Task should be allocated for simple activities. As a rule of thumb, tasks shorter than one month (time and/or man effort) should be avoided."*

3.3 The Definition Phase or Requirements Definition Phase



The first operation in the flow is the definition phase, where through the co-ordination of the project manager, a complete feasibility study is carried out.
From the output of this phase, a decision is made whether the project will go ahead or not.
Strictly speaking, the definition phase is a management task, but because of its complexity and its importance on the future of the project, it is sometimes advisable to single it out as a Workpackage. In the example that will follow, however, we have still considered the definition phase as a management task, to stress the importance of the leading role of the project manager.
The definition phase can be broken down into at least five main tasks, to be carried executed serially:

a. Preliminary ASIC functional requirements, to be detailed in section. 3.3.2.1
b- Costs, size, time and risks estimation, together with the identification of subcontractors and foundries, from sections 3.3.2.1 to 3.3.2.8
c- ASIC trade-off or Feasibility study, and final decision,
d- ASIC final specification and Costs, Size, Time reassessment,
e- Final Workplan.

Each of the five results expected from the definition phase can be reached if a complete list of the required inputs is detailed, the methodology described in the Appendix allows the project manager and his team to identify the resources, and the time needed to carry out the relevant activity.

The output of this phase is reference documents and it is of the utmost importance they are edited and maintained as required. Some advice on this is given in Appendix. The minimum set of documents this phase has to produce is indicated below.

3.3.1 - The ASIC Spec.'s :

One of the main document of the requirements phase, and the first to be produced, is the ASIC specification, because the majority of project failures are due to vagueness or errors in this document, which is the result of the specification task.

In other words, failures generally come not from an inappropriate use of design techniques, but from lack of communication between the marketing people and the designer and manufacturer. As the "language" is usually different between these groups, due to the sensitivity to problems, this leads to the underevaluation of parameters or functionalities.

In addition, the ASIC specification has to be a guide for the designer, for the ASIC manufacturer and for the project manager, therefore proper documentation, formulated according to Best Practices, is absolutely mandatory.

Such documentation should consist of a conventional paper-based document, discussed and approved by the system manager, the designer and the project manager, with the external support of whoever maybe useful, such as silicon manufacturers, CAD providers and such.

The paper documentation should list only the exact requirements of the ASIC is required to produce, such a document should appear exactly as the specification of a standard component. This should be as concise as possible, but certainly including the block diagram, the power requirements, DC and AC characteristics, pin-out, package, storage and operating temperature with the eventual derating of parameters, functional description, interface capabilities, test strategies.

AE 240 relates, as one of the most important lessons learnt, " Have a clearer definition and specification of the product using the ASIC prior to commencing the AE".

More specifically " The first user only discovered the limitation, when the initial design was submitted to the sub-contractors for a quotation. The result was a loop back to

specification where it was necessary to add a memory management unit to the ASIC. This is just one example of many changes that had to be made to the specification during the design phase. While it is probably impossible to avoid such loops, more time should have been spent in avoiding as many loops as possible." But that is not all. They add: " ***The refinement of the spec. as the AE proceeds****, is particularly important for ASIC design and ……….it relates to the product and component specification. It is not possible to produce a refined specification at the beginning as there are many 'don't knows' such as technology limitations etc. The refinement of the specification as it proceeds prevents the possibility of out of date documentation. It is also important to avoid the pitfall of 'creeping elegance' where the specification is gradually improved with each small improvement not affecting deadlines or budgets but in their entirety, making the experiment non-viable."*
AE 2209 refers of a similar experience for this task: " A lesson learnt was that specifications should have included a greater grade of detail, which have avoided confusions and saved time. "

3.3.2 - The Subcontractors' selection :

This document is part of the second set to be produced (together with the documents concerning the foundry selection, overall cost and time needed).
Very rarely, a project can start and finish in-house without any external help, where "external" can also mean a different department within the same company. Such external help selection and management is a very sensitive issue, because the subcontractor's effectiveness and efficiency can impair the whole project, especially in the case when a new technology or methodology, unfamiliar to the customer, is going to be used.
In general, whenever a choice of any kind has to be made, such choice is dictated by some requirements, such needs should be listed and weighed up relative to one another, so that all the possible solutions to these requirements can be rated.

The following Best Practices rules should be followed in choosing and dealing with subcontractors :

- If you want your people learn something from the subcontractor , that should be clearly asked for, detailing your requirements as contents and modalities, in the request for quotations,
- Get a quotation from more than one possible subcontractor,
- Be suspicious of an exceptionally good quotation : it may mean that the efforts have been underestimated, or the specifications have not been properly understood,
- Take great care for developing, together with the subcontractor, contingencies plans when only one vendor is apparently capable of doing the work,
- If more than one subcontractor is needed, verify they can work together and that a proper interface is established,
- Check for references,
- The ASIC specification must be generated together with the subcontractor(s), silicon vendor or design house or both,
- Bear in mind to make some time allowance for the subcontractors' tasks in the Workplan, as, uthe subcontractor can have other concurrent, and time-competing, activities,
- Set-up procedures, terms and conditions for unforeseeable technical problems and delays caused by the subcontractor,
- Payments should be made in conjunction with clearly defined deliverables,
- Decide on matters regarding the ownership of the work when committing to a subcontractor,
- Review the progress of the work as often and as thoroughly as necessary,
- Regulate the subcontractor's involvement through a clearly written contract, including penalties and termination clauses.

This part of the requirements document should certainly contain the subcontractors' contracts as

well as all the resultant information, by abiding to the previous Best Practice rules, allowing a complete tracing of the flow that brought the correct choice. The following paragraphs give some Best Practice hints on the matter.

Example taken from AE 1005 , summarising how the choice of subcontractor has been made.
"Selected after a study of quotations from a number of candidates. The parameters studied included technology, NRE, circuit pricing and possibilities to support PartnerTech during our design process."

The following are examples illustrating delays coming from an insufficient contractual agreement with the CAD vendor:

- *AE 22964 and AE 2177 – In both projects the design package of Xilinx (Foundation Std VHDL Package) revealed several problems to fit and simulate the device in some FPGA that needed constant upgrade and frequent requests for additional help. These projects had one-month delay. During the negotiation phases of both these projects TTN warned FUs on the risk related to the choice of non-mature development tools and advised to purchase CAD tools offered by a Competitor. Due to the higher price, FUs chose the XILINX one.*

The following is an example of a delay coming from an incomplete assessment of the subcontractor's resources

- *For the development and delivery of an Integrated Circuit (mixed ASIC) to interface piezo-resistive bridges (AE 2091), the First User choose a subcontractor with the necessary know-how and operating as a Design house. However, the first agreement with them was terminated due to the resignation of a third party contractor (managed directly by the design house and not visible to the company) and to the insufficient availability of the personnel resources in the design house for design and layout. For this reason the First User needed a six months project extension.*

The next two examples tell about virtuous subcontractors' selection and contract .

- *In AE 27771 the FU chose a University Institute as Subcontractor. To cover any risk for the ASIC development, the company enclosed heavy Penalty clauses in the contract. In case the subcontractor doesn't meet the performance, the subcontractor must redesign the ASIC without any FU additional financial support.*
- *In AE 23550 the subcontractor's choice was one of the first milestone to be posed and it was surely influenced by the FU management conviction to find not only a subcontractor for the AE but a partner and a supplier. So the Company signed a co-operation agreement with a subcontractor to be more guaranteed about the industrialisation and the development of the new products and the internal planned replication. Thanks to this co-operation, the subcontractor's worth has been proven by its advice to use a part different from what initially planned, that actually passed all the necessary tests.*

From AE 23295 comes the following lesson: " For critical subcontractors, frequent Review Meetings are important and became paramount for contingencies management. Don't underestimate the problems related with geographically remote partners."

For more information on contractual matters, please refer to the "Managing Subcontractors" training material.

3.3.2.1 Silicon Foundry Selection and Management

General considerations.
The Silicon Foundry selection process can significantly affect the entire development, and, if not properly managed, can lead to significant time delays and even to failures. Once selected, the Manufacturer has to be deeply involved in all the activities-from the specifications assessment to the system prototype test and full production's quality and reliability issues. A kind of partnership should be achieved, where both parties can gain and develop a trusting long term relationship. That, however, must not prevent the customer from checking, and sometimes the prices and services of some of the manufacturer's competitors.
In carrying out the silicon manufacturer selection a prerequisite must be fulfilled, and the exact ASIC technology selection: whenever possible, a technology should be chosen that can be offered from more than one manufacturer, albeit with slightly different performance characteristics. This can help, in the unfortunate case that the chosen manufacturer experiences problems of such a nature that it's impossible for it to complete the job. Having to trim and tune the original design to the requirements of the second supplier represents certainly an additional delay, that might even be acceptable by the customer's marketing team, but also represents a way out of a stalling situation.
This type of occurrence is quite rare, but for a first user, it may happen. In FUSE, 2% of the designs had to be retargeted to a different foundry because it was impossible to complete the experiment with the initial one.
There is a cost, because almost any retargeting requires minor or major changes to the original design, and one has to re-run all the simulations and invest additional time on it.

COTS second sourcing objective aims to avoid supply shortage. It consists of using infrequently, on the same product, components from different manufacturers, provided that they are "pin-out" compatible and the main parameters, functionality, performance and reliability equivalent. In the case of very large volumes, there is a price competition amongst the various vendors and can provide additional cost advantages. For COTS this can be obtained because of the "standard" nature of the devices. Being standard, it means that its market existence has been determined and considered worthy by at least a silicon manufacturer, therefore other manufacturers are attracted to emulate and compete in it.
The objective of ASIC second sourcing is almost the same as for COTS and aims to avoid the ASIC possibility of not being able to manufacture. But, unlike COTS, once manufactured the price competition effects are non-existent.
Therefore, in strict terms (the same device made by two vendors), ASIC' second sourcing is not an issue, as it is too expensive to set up, and it makes worse the cost per unit (as the whole quantity is split between two manufacturers). For ASICS second sourcing means keeping open the possibility to change the manufacturer, in case of really bad manufacturing problems, through a high level design and a proper technology selection.
Regardless of the second sourcing issue, the silicon manufacturer's selection should be based on the assessment of four items, with the objective of evaluating the manufacturer in terms of them as an organisation, a technology provider, an economic institution and their reliability:

⇒ The company as an organisation of people, dedicated to the business of silicon wafer processing.
⇒ What are the products they manufacture, and with which tools.
⇒ How do they interface to and support their customers.
⇒ How reliable are their processes and products.

COMPANY'S BUSINESS AND ORGANIZATION ASSESSMENT

The right time and effort must be dedicated to a thorough assessment of items such as:

- Structure, organisation and key personnel of the manufacturer.
- Marketing and selling policies, strategies and future plans.
- Market share, revenues and financial status.
- Number and production volume of products (Are they limited to large volume production or do they support small volumes or do they just prototype ?)
- History of successful products and indication of their keys to success,
- History and analysis of failure, not easy to obtain-.

All of the above information is required to understand and assess the effectiveness and efficiency of the manufacturer, its economic stability (in order not to be abandoned halfway), its plans (to understand if a long term relationship is advisable), its understanding of the work needed before the actual implementation on silicon and its willingness and capability to solve interface problems.

COMPANY'S TECHNIQUES AND TECHNOLOGIES ASSESSMENT

On the technical side, the following verification should be done :

- Do the available technologies meet the system's requirements ?
- What is the foreseeable lifetime of the chosen technology?
- Which kind of interface, and when do they propose ? The simpler the interface the better it is, but it is useful to have thorough verification or assistance in case it is required during the design phase,
- Which kind of flow, and which tools do they propose for the project ? Do they have guides for the flow and manuals for the tools ?
- If the customer has its own tools, are they compatible with, or supported by, the manufacturer environment ? This item should be well analysed, starting from the operating system to a compatibility analysis, integration level and limitations, versions, completeness, etc.
- Simulation tools have to be completely aligned ; sometimes the silicon vendors have a reference simulator (the " golden simulator") : can it be used to have a validated simulator ? the ASIC has to behave exactly as the simulator indicates !
- Which testing strategies do they use ? do they support cells (Scan register, Macros BIST, JTAG support, LSSD ...) to improve the testability of the chip ?
- Are the library cells well documented and compatible ? Does the library content meet the need of the design ? are there constraints about the use of Macros (IPR for instance) ?
- Is technical support on the design provided ? which are the people who will help, and can they provide also some kind of training on design, technology, process, and tools' usage ?
- Which kind of instrumentation do they use to test the devices ? is it compatible, in terms of Voltages/currents, speed, temperatures, test duration, number of pins, complexity of test pattern with the needs ?
- What is their cycle time commitment for delivering the finished and tested parts?
- Do they work in a Quality Regime ? What kind of certification do they have, and what kind of organisation do they have to maintain it ? How do they document it, and how long do they assure traceability of production lots ?
- What is the cells' library validation flow ?
- What is the current yeld of the technology proposed for the Asics ?
- Is reliability data available ?

The above questions, that represent a general example, are clearly aimed at assessing how and with which tools the silicon vendor work, what kind of technical relationship can be made, how credible is its capability to undertake the job and to finish it successfully, how reliable is its

process, how much under control, and how good and how fast it is in taking corrective actions.
The results of the technical selection has to be compared with the economic quotation for undertaking the job, and this is the answer to a set of requests from the requirements document.

THINGS TO REMEMBER WHEN ASKING FOR A QUOTATION

A request for quotation should include:

* The ASIC specifications (this should be already known to the silicon vendors) with a list of the tools that will be used to develop it, the transfer formats and die size estimates. Good Practice suggests to name the ASIC or the Project.
* The requested technology.
* The package.
* IPR (if any).
* Test (Quality) and reliability requirements.
* Interfacing procedures.
* Milestones, both technical and economic.
* Requested start and end time, delivery time of production lots.
* Number of prototypes/volume production.
* What kind of on-going support is required.
* Training on specific issues (if needed) with indication of location, duration, number of people,
* A request for the individually pricing for:
  the requested number of prototypes (subdivided into design support (if any), IPR (if any), silicon processing, testing, packaging),
  each volume production's chip,
  any specific Q&R requests,
  support,
  training,
  any other issue relevant to the Customer.

* a request for guarantees on respecting the delivery times and on assistance,
* a request for maintaining for a certain period of time the manufacturability of the ASIC,
* a request for a time validity of the quotation,
* a request for terms and conditions of payments.

The request for quotation should be as unambiguous as possible : the example given tries to encompass any possible item of possible attrition.
When receiving back the formal quotations, if the requests have been detailed as above, it should be quite straightforward to compare them, item by item, sorting the one that best suites the need.
The answers are not always as clear or as complete as one would have expected: sometimes clarification and some compromise is often necessary.
A **Confidentiality Agreement** is requested from the silicon vendor prior to starting the work, and it should be signed as soon as a silicon vendor is involved in the discussions over the architecture/application of the future chip.

In the cases where a Multi-Project Wafer broker is involved, instead of a silicon foundry, nothing should be changed in the methodologies, as the problems, for the Customer, remain the same.

EXAMPLES :

<u>No proper checking of the willingness to support small companies</u>
AE 23020 – In this project the Cadence Hit-Kit for AMS CBZ technology was made available, in its full layout capability, by the foundry two months out of schedule. During the definition of the contract, the foundry maintained that it was immediately available. The company discovered that the immediate availability was true only for big customers and not for small ones like the FU .
<u>No proper checking of the technologies performances</u>

- *In AE 23020 the company had to change the technology from MIETEC HBIMOS to AMS CBZ since the first simulations had shown that HBIMOS was not able to provide the required HI-FI compatible harmonic distortion. The early choice caused one-month delay in the project.*

<u>No contractual precautions for change or termination of technologies</u>
In AE 23208 during the design of an analogue ASIC, the Silicon Vendor advised the FU not to use the CBR 2u process for its new design and to replace it with the new CAR 1,2u technology. This required more time to modify, re-simulate and re-layout the circuits already designed. This forced change happened with the project in progress and caused a big delay. At the beginning of the project TTN asked to the foundry when the obsolescence of such a technology would have occurred and the answer was that for the next 5 years such a technology would have been supported. The Foundry itself delivered an updated offer for the MPW Service (in CBR 2u, the old process) after the project beginning, without mentioning any obsolescence problem.
AE 24675 found out a more general consideration, i.e.: " A close engineering working relationship is required with the ASIC manufacturer. In this Application Experiment fully understanding how the foundry process works was a key lesson that was learned. Incorporated with that is the effect that implementing layout changes causes and its impact in time-scales……. A detailed understanding of the various process stages, revisions and task implementations would be a distinct advantage. ……..Therefore it is important to fully understand the manner in which the sub-contractor works."

Keep the contact with the silicon foundry continuous because the support for a certain technology may vary along the time of the experiments and the production may not be anymore possible at the cost estimated at the start of the project. "

3.3.2.2 Interfacing the subcontractors

For a company starting an ASIC development for the first time, two important subcontractors have to be envisaged: the design house and the silicon manufacturer. In order to avoid problems generated by unclear or overlapping responsibilities about the final chip, one of the following three different ways of dealing with these two subcontractors has to be chosen and formalised:

1. <u>Two</u> points interface:
The company, in the way described later, generates the ASIC Specification; an external design house develops the data files describing the "virtual chip" and these are approved by the company. A silicon foundry manufactures, tests and delivers it to the company; which approves it in the target environment. The responsibility of the chip is with the company.
2. One point with a <u>high level</u> (i.e. specification) interface :
The Company issues the specifications; an external design house (or the silicon foundry itself) takes charge of the design, (which has to be approved by the company) and also interfacing with the silicon foundry for the manufacturing and delivering of the tested parts to the company. In this way, the whole responsibility is focused on a single interface (design house) making all the process simpler to the First User company, who still has to finally approve the ASIC on the real environment,
3. One point with a <u>low level</u> (i.e. netlist or layout) interface:

The company issues the specification and design of the chip; the silicon foundry, directly or through a broker, manufactures, tests and delivers it to the company, which approves it in the target environment. In FUSE, as this project deals only with First Users, the companies passed through a "training on the job" which was carried out with skilled subcontractors willing to introduce them to their first ASIC design. In this case the company takes the full responsibility.

EXAMPLE 1: A one point-high level interface- company and design house AE 1029 developed a mixed ASIC for diagnostic instrumentation (eddy currents). Together with an external Design House, they finalised the specifications. The external Design house had the responsibility for designing (while teaching) the chip and interfacing the Silicon Foundry.

EXAMPLE 2: A two points interface- company, design house, silicon manufacturer
AE 1213 deal with an ASIC for controlling pumps for biomedical applications: an external Design house generated the Specs (together with the company) and designed the chip. The Company, under guidance and advice from the Design House, interfaced directly the Silicon Broker.

EXAMPLE 3: A one point low-level interface- company, silicon manufacturer (with training
In AE 23717 a Mixed ASIC has been developed by the First User with the assistance of a subcontractor, which did an on job training for the company designer and management. The Company interfaced directly the Foundry.

Interface problems

Lessons learnt by AE 240 (two-point interface) in interfacing the foundry: "Talk to the foundry directly as early as possible about technology specific issues and limitations." More specifically " The first user learned after the ASIC prototype was fabricated that the foundry had a number of DSP IP cores that could have been used to speed up and optimise the design. The foundry had optimal multipliers and dividers and other arithmetic functions which could have been utilised if the first user had investigated the availability of such cores more thoroughly".
AE 24606, which developed a Mixed ASIC, learnt that " Interaction with subcontractors and silicon foundries taught us to depend more on our own knowledge, or lacking that, to gain more knowledge to base our decision to known facts. In spite of lengthy presentations and discussions, the representatives of subcontractors and silicon foundries are only human: they can make errors and faulty recommendations. All decisions that are based solely on unilateral knowledge are subject to misunderstanding."

3.3.3 The Risk Management

Any action undertaken is subject to mishaps: more so the more complicate is the activity. Introducing an ASIC in a Company, especially when the Company itself is a First User of that technique, is a risky business, whether methodological, technical, technological and economical. Therefore all the possible precautions should be taken to minimise risks of failure.
Those precautions are based upon the sensitivity, competence and experience of the people involved in the project, the project manager must always ask the question "What if?" and "How do we overcome?" These are questions to and from the various groups of people who are involved in the project.
Below are a few general rules to follow, reminding that the situations and possible causes of failure vary widely according to the project, the external supporting organisations, the company's expertise

and general situation.

Risks are accidents that can prevent the meeting of a deadline, or reaching the expected result. This can be the final device does not meet the expected requirements or it cannot be manufactured at all.
Reasons for those mishaps can be categorised into two families; accidents that cannot be foreseen, being independent of the capabilities and best knowledge of the various partners, and those that can. The first category has rare accidents; such as natural events (fires, earthquakes e.g.) or human driven events (such as union strikes, riots etc.), that encompasses problems much larger than those connected with an ASIC development project. These cannot be controlled by those working on the project.
Regarding the many different, foreseeable causes by definition can be identified and controlled, However, there still exists the problem of the identification of all the possible causes of accidents, as they are many, and being related to that particular project with those particular partners no specific rules can be given, only general and generic guidelines.

The project management methodology is the most, and very often the only, important instrument to control the possible risks; a such methodology has to be based on quality management techniques or Best Practices. Again, we'll try to highlight how a proper methodology can help in driving out possible problems (risks), evaluate them and foresee possible solutions. Certainly one has to be prepared, despite the fact that risk analysis has been done at the best, to face unforeseen problems. If the advanced analysis has been carried-out thoroughly, those extra problems should be minimal in number and seriousness.

The methodology explained in the following is absolutely necessary in the Definition phase, where, as minutely as possible, the activities to be carried on, with the participants and the time needed, are defined.

- ♦ It is in this stage that the project manager, together with the development team, has to try to envisage all the possible misshappenings of any activity. This is done by using the brainstorming technique (by which everybody is entitled and solicited to give his own view, even the most farfetched, and regardless of qualification and status of attendees. A Ishikawa fishbone diagram (by which all the accidents identified by brainstorming are represented and weighed, according to the attendees sensitivity and experience), or a simple weighed listing are the most important instruments that allow the most probable picture of what can go wrong.
- ♦ The same people, then, have to devise, if necessary using the same two techniques, which are the most effective and efficient ways to overcome such problems.

These alternate routes usually mean time delays or extra money or both . The documentation and Workplan have to report and detail them to the company's upper management. The probability figures associated with the accidents and their implications (time/money), coming out from the company's and external experts brainstorming, give the upper management an additional view on the feasibility of the whole project. This will allow them to approve, or disapprove, on the basis of a calculated overall risk analysis and its time/money implications.

Therefore a risk assessment document is necessary, with its implication on the economics and Workplan.

A few guidelines :

I. Accidents and unwanted surprises, related to external suppliers of materials, equipment and services are minimised if the company abides to the Best Practice selection process described in par.'s 3.3.2.2 and 3.3.2.3 of this chapter, that have to be operative as soon as the definition phase starts :

   A. for parts, materials etc.. have more than one supplier ready to serve ;
   B. for hardware and software needed for the design, and for which there are no second sources, demand guarantees on the delivery, installation, functionality, upgrading, interoperability, interfaceability, maintenance, training and technical support ; negotiate penalties.
   C. for externally commissioned design, and for the ASIC fabrication, regardless if through a silicon manufacturer or an intermediate broker, negotiate penalties.
   D. if you do not design the ASIC in house, and it's your first time, look, before choosing, for a couple of design houses with equal tools and maintain an open door, as long as you can, with the one not chosen,
   E . for the silicon implementation, chose, as first step, the technology and try to have more than one supplier that can provide, with that technology, similar performances.

II. For the in-house activities, their risks should be minimal if :

   a. One person = one activity is avoided: make allowance for possible personnel turnover,
   b. Assurance, from the upper management, that the human, technical, organisational and economical resources are available at the agreed dates,
   c. The appropriate competencies exist and have been chosen,
   d. The proper training process for competencies to be created is planned (what, who, where, how long, how much, and any follow-up) ,
   e. Time allowances have been made to allow trainees to be self-sufficient, and tutors allocated,
   f. Tools (i.e. hardware and software) are available, properly maintained and updated,
   g. A proper flow of information throughout the company is in place and maintained.

EXAMPLE :

Personnel related problems

- *In AE 23175 the Project time was much longer than what the First User scheduled. This considerable delay was due to the FU decision to entrust the project to a junior engineer. In Milan the job market offers many opportunities to a junior engineer. Three trained junior engineers, involved in AE, resigned and FU got many difficulties in replacing them. To break this loop, after that the company manager directly experienced such difficulties, the TTN convinced him to involve a senior engineer to complete the project.*
- *In AE 22930 a second time-slot of four months delay was due to the fact that the First User) lost the designer in charge for the project from his team. He developed the specifications of the product and carried out their description in the VERILOG format. These files were synthesised by a subcontractor and fitted in one FPGA. The new designer, who replaced the previous one, encountered several difficulties in carrying out the project, and he had to update his skills in order to support the modifications of the VERILOG file while testing the FPGA on its printed circuit.*

AE 240 states "*Plan the deployment of staff more carefully: The first user ran into many difficulties when staff were re-deployed to perform the AE. Other aspects of the first user's business suffered. This was particularly acute given that the Company has six full time people of which one third were re-deployed to perform the AE. An increase in business during the AE along with personnel*

changes presented many difficulties and challenges to the first user. There was no scope to take personnel off the AE for more than a day at a time as the AE was already running behind time."

3.3.4 Workplan

The objective of this section is to provide the ASIC project manager with some Best Practice baselines in order to build, a time-dependant flow of activities together with the necessary technical and economical resources. Such a Workplan should allow for delays and contingency (i.e. alternate routes).
The allocation of adequate resources, human as well as financial, with clear attribution of responsibilities, make any plan credible and feasible.
Information on this issue will be given in the form of real examples from FUSE, except in a couple of cases, regarding sensitive matters (internal costs). The examples (still from FUSE) lack the AE reference and have the costs figures varied for obvious reasons.
Each step of the Workplan structure will be discussed to make the reader understand the rationale. It is important to note that the following is just an example with its intrinsic limitations, as a true Workplan discussion depends heavily on the consistence of the initial competence of the company and on the complexity of the project itself.

There are standard software tools, that help to devise all of the following tables and provide an omni-comprehensive easy-to-read Workplan ; however, in order to provide a thorough rationale, those tools have not been used here.

A good Workplan consists of :
1. a description of the activities in time, divided, as proper or convenient, in Workpackages, Tasks , Subtasks (WBS and GANNT);
2. a description of the personnel involved in the various activities with the relevant costs;
3. a time dependent description of the expenditures per activity, to be able to predict the cash (economic) flow.
4. to be able to predict the cash (economic) flow.
5. a description of the roles and responsibilities (OBS);
6. a description of the milestones and deliverables.

The Workplan is a provisional set of document developed with the best support of many and different people.
Its primary objective is to enable the company's management to assess the technical and economical feasibility of a project.
After the start of the project, it MUST be maintained and updated.

1- WBS and GANNT

All ASIC project activities, should be summarised by the following anticipated Workpackages , Tasks and Subtasks (WBS):

Table 3.3.4-A Sample of WBS

Workpackages	Tasks	Subtasks
1-Management	1.1-Requirements Definition	1.1.1-ASIC Requirements
		1.1.2-Costs, Size, Time first Estimation
		1.1.3-ASIC trade-off
		1.1.4-ASIC final specification and Costs
		1.1.5-Final Workplan with Resources
	1.2-Monitor the experiment	1.2.1-Best Practice implementation
		1.2.2-Support, Control and Adjust
2-Design	2.1-Behavioural Description-Simulation	Subtasks can be defined as required
	2.2-Gate level design-Simulation	Subtasks can be defined as required
	2.3-Test vectors generation	Subtasks can be defined as required
	2.4- PLD implementation *	Subtasks can be defined as required
	2.5-Layout-Simulation	Subtasks can be defined as required
3-Manufacturing	3.1- Silicon Foundry Interface	Subtasks can be defined as required
4-Board/System pro-totyping	4.1-Board Design	Subtasks can be defined as required
	4.2- Materials Purchase	Subtasks can be defined as required
	4.3- Assembly & Test	Subtasks can be defined as required
5-ASIC Part approval	5.1-Board level approval	Subtasks can be defined as required
	5.2-System level approval	Subtasks can be defined as required

- The summary table above has to be completed by the description of each anticipated activity:

What follows is a cut-out example of the WBS description of the specification Workpackage from AE 516

Workpackage 2: ***Specification***

Objective: Cardiotest will be a complete digital electrocardiograph with 12 leads for home use. It is for the memorisation and transmission of ECG tracks to a listening centre.
WP outputs*: Cardiotest integration will be carried out by using a hybrid circuit, which will include:*

-An ASIC, planned and realised by the company in ***CMOS 1.2m*** *technology. The ASIC is used for the acquisition and elaboration of analogic signals and serialised A/D conversion, taking advantage of the* ***MULTI PROJECT WAFER*** *process because of its low costs compared to a dedicated RUN.*
-An E2PROM serial memory to permanently memorise the ECG tracking.
-An 8 bit microcontroller (Nation Cop 8782 CL or better) for:
- the management of the interface for the user
- the management of the A/D conversion
- lead selection
- FSK modulation
- the direction of the data, the reading, the writing of the memory.
–Passive Components
*To realise the project, Hardware (****Workstation****) and Software (****CAD -****description paragraph 4.3.5.3) will be bought and installed. The total cost of the Workstation is 20 KEuro. This cost is calculated on a pro-rate base: 7KEURO.*

Duration: *2 months*

Roles and responsibilities

First User	*Definition of the technical details and of the realisation time,* *Hardware (SUN SPARCstation) and Software (CAD Cadence) installation.*
Subcontractor 1	*Furnishing the characteristics of the library Parts*
Subcontractor 2	
Subcontractor 3	

Task 1: Functional specification of the system

Cardiotest will be able to acquire the 12 leads necessary for taking the ECG tracks. Treated and elaborated, these signals can be sent via telephone to a medical listening centre for a preventive diagnosis by the specialists.

Duration:*½ month*

Task 2: System specification of component

The device used in the final product must be complete and independent of other components; it must satisfy the aforementioned characteristics described. During this phase, the planning decisions to satisfy these characteristics will be made.
The final blocks and their relative functions that globally realise the component will be defined in this phase.

Duration *: ½ month*

Task 3: Technical specification of component

For each of the blocks defined in the preceding task, the relative technical specifications will be defined. They are:
- Selection of the twelve leads;
- Amplification of the input analogue signals
- Low band filtering;
- Determining the analogue gain;
- Analogue digital conversion;
- Data memorisation;
- Modulation and management of the asynchronous communication protocol;
- Pass band filtering;
- Interface management of the user's keyboard.

Duration*:1 month*

- The flow of the activities in time is represented by a GANNT diagram.

<u>*Bar Chart or GANNT from AE 22895*</u>

Months	1	2	3	4	5	6	7	8	9	10
Workpackage 1 Management										
Task 1 Project management	X	X	X	X	X	X	X	X	X	X
Task 2 Final report										X
Task 3 Reviews and reporting	X	X	X	X	X	X	X	X	X	X
Workpackage 2 Specification										
Task 1 System's spec.'s.	X									
Task 2 Gate array spec.'s	X									
Task 3 verification		X	X							
Workpackage 3 Training										
Task 1 VHDL	X									
Task 2 Synthesis	X									
Task 3 B-scan	X									
Workpackage 4 Design										
Task 1 Synthesis			X							
Task 2 Simulation			X	X						
Workpackage 5 Evaluation										
Task 1 Prototyping					X	X	X			
Task 2 Test set-up							X			
Task 3 Functional test								X	X	
Task 4 B-scan test					X					
Task 5 Field test									X	X

The Workplan is, at this stage, a provisional, but agreed upon, flow of activities, with the required time to carry them out, but without the resources and any other costs to be incurred.

TABLE 2- PERSONNEL COSTS BREAKDOWN (KEuro)

Names	Costs EURO/month	WP 1 Costs & Months	WP 2 Costs & Months	WP 3 Costs & Months	WP 4 Costs & Months	WP 5 Costs & Months	Total months	Total costs
A	10	40- 4		5-0,5			4,5	45
B	7.8	15,6- 2	15,6- 2	7,8-1	3,9-0,5	1,9-0,25	5,75	44,8
C	6,5	19,5- 3	19,5- 3		6,5-1	3,25-0,5	7,5	48,75
D	6	21- 3,5	18- 3				6,5	39
E	5,1					6,25-1,25	1,25	6,25
F	4				4-1		1	4
Totals	**Costs**	!Syntaxfehler, (	**53,1**	**12,8**	**14,4**	**11,4**		**187,8**
Totals	**Months**	**12,5**	**8**	**1,5**	**2,5**	**2**	**26,5**	

Table 3- EQUIPMENTS, MATERIALS, EXTERNAL SERVICES, FINANCIAL FLOW

Legenda:
O= Order or Contract
A= Availability of E, M or EX

Accounts	Cost	Month 2	Month 3	Month 4	Month 5	Month 6	Month 7	Month 8	Month 9	Month 12
	KEuro									
Travels	2	2								
Subcontractors	1		1							
TOTAL WP 1	**3**									
Travels	1		0,5	0,5						
PC A	10	O	A	10						
Printer B	4	O	A	4						
Package Y	2	O	A		2					
Programmer D	3			O		A	3			
Package Z	1			O		A	1			
Other materials	5	O	A	A	5					
Miscellanies	5	1	1	1	1	1				
Subcontractor	2				2					

TOTAL WP 2	!Syntaxfehler,)									
Travels	7		2	4	1					
Subcontractor J	27	O	A/7						10	10
TOTAL WP 3	**34**									
Travels	1					1				
PC boards	3				O		A/3			
Components	7				O		A	7		
Miscellanies	1							1		
TOTAL WP 4	**12**									
Tester	3				O		A		3	
Subcontractor	1								1	
Miscellanies	1							1		
TOTAL WP 5	**5**									
TOTAL	**87**									
Expenditures flow	**87**	**3**	**11,5**	**19,5**	**11**	**2**	**7**	**9**	**14**	**10**

AE 26002 started after an accurate cost planning because the First User had some financial problems. This methodology allowed the project development without breaks.

Table 4- PROJECT'S COSTS SUMMARY TABLE (KEuro)

Workpackages	Task	Personnel (see above Tables)	Travels	Equipments (see above Tables)	Materials (see above Tables)	Subcontr.	Others	**TOT.**
1	1.1	56,1	2			1		
	1.2	40,1						
Costs WP 1		**96,1**	**2**			**1**		**99,1**
2	2.1	25,1		15		0,5		
	2.2	11				0,5		
	2.3	7	1			0,5		
	2.4	5		5	5		5	
	2.5	5				0,5		
Costs WP 2		**53,1**	**1**	**20**	**5**	**2**	**5**	!Syntaxfehler,)
3		12,8	7			27		
Costs WP 3		**12,8**	**7**			**27**		**46,8**
4	4.1	7	0,5					
	4.2	2,4	0,5		8			
	4.3	5			2		1	
Costs WP 4		**14,4**	**1**		**10**		**1**	**26,4**
5	5.1	5,2		1,5		0,5	0,5	

	5.2	5,2		1,5		0,5	0,5	
Costs WP 5		**11,4**		**3**		**1**	**1**	**16,4**
Tot. Costs		**187,8**	**11**	**23**	**15**	**31**	**7**	!Syntaxfehler,)

3.3.4.2 The Responsibility matrix or OBS

The responsibilities matrix identifies the role and responsibilities of the personnel and external consultants in the project, attributing the necessary authority, together with the relevant duties.

Table 5 - *OBS from AE 22895*

Resource and Responsibility	***WorkingDays***	***Activity***
		Workpackage 1 Management
KK- leader	*10*	*Project Manag.*
KK- leader	*5*	*Information management*
KK- leader	*10*	*Control and Reporting*
		Workpackage 2 Specification
KK- leader; *ZZ,* *FF,* *TU*	*5* *2* *1* *1*	*Funct. Spec.*
KK- leader *TU*	*5* *5*	*GATE ARRAY Spec.*
KK- leader *ZZ* *TU*	*30* *30* *10*	*Technical Verif.*
		Workpackage 3 Training
TU - leader *AK* *BJ*	*3* *2* *2*	*VHDL*
TU- leader *AK* *BJ*	*33* *30* *30*	*B-Scan*
TU- leader *AK* *BJ*	*10* *7* *7*	*Synthesis*
JTAG- leader *AK* *BJ*	*2* *2* *2*	*B-Scan*
		Workpackage 4 Design
TU- leader *AK* *BJ*	*5* *5* *5*	*Synthesis G.A.*
TU- leader *AK*	*10* *15*	*Simulation*

BJ	15	

Etceteras…………

3.3.4.2 Milestones and Deliverables

Milestones are important checks on the project's achievements, if checks are ok then the work can go on, otherwise actions to correct a problem have to be implemented.
In the latter case the planning must be updated and rescheduled.

In the example below, milestones are numbered as M1 in the first month, M3 in the third and so on. Deliverables, that is documentation or prototypes, are referred to the Workpackage, task or subtask.

WP	Tsk	STsk	Milestones	Deliverables	Deliverables Description
1	1	1.1.1		D1.1.1	Asics's Requirements
		1.1.2		D1.1.2	Estimated Costs, Sizes, Time, Risks
		1.1.3	M1	D1.1.3	Asics's trade-off, Foundry Selection
		1.1.4	M2	D1.1.4	Asics's Specifications
		1.1.5	M2	D1.1.5	Project Workplan
1	2	1.2.1		D1.2.1	Description of the Best Practice procedures installed
		1.2.2	M1 through M12	D1.2.2. (1 to 12)	Progress review reports
2	2.1		M5	D2.1	Behavioural Description of ASIC and simulation results
	2.2		M7	D2.1	Gate level Description and simulation results
	2.3		M8	D2.3	Test vectors description and results
	2.4		M7	D2.4	Implementation of digital Asics in PLD
	2.5		M8	D2.5	Layout description and simulation results
	2.6			D2.6	ASIC final Database to foundry
3			M10	D3	Packaged Asics's prototypes
4	4.1		M4	D4.1	(Bread)board Design
	4.2		M5		
	4.3		M8 or M9	D4.3	Final (bread)board and PLD or/and ASIC test results
5	5.1		M12	D5.1	Board level test results
	5.2		M12	D5.2	System level test results

3.3.5 ASIC trade off or Feasibility Study

Having gathered all the information detailed in the preceding sections (3.3.2.1 to 3.3.2.8), and proving the technical and operational feasibility of the project, with the necessary rationales, the project manager has now simply to prepare and submit to the top management a summary expenses' table that highlights the economics of the possible undertaking.
A table like the following would be ideal:

Cost evaluation of ASIC …….

Production Volume……… Project……………..

Costs type	Description	Amount

Development

1. Specs' definition		
2. Functional Schematic		
3. Functional Simulation		
4. Net list		
5. Circuit simulation		
6. Layout		
7. Testing		
8. NRM		
9. Amortisation		
Total development cost		**A**

Yearly Amortisation for development - **B-**	A/3 or A/5
Development cost for each prototype -**C**-	B/n prototypes

Production

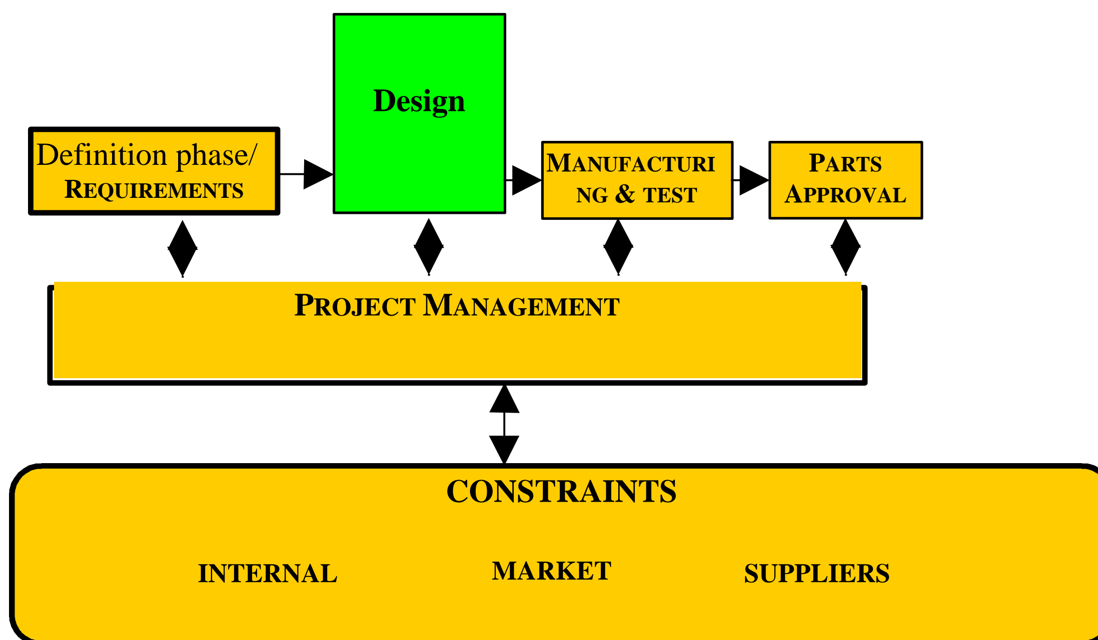
1. Unit cost		
2. Production assistance (x device)		
3. Shipments and Customs (x device)		
4. Incoming inspection (x device)		
5. Incoming Tests (x device)		
6. Warehouse (x device)		
7. Amortisation left (x device)		
8. Other costs (x device)		
Production unit cost		**D**

Development costs	**A**
Unit production cost	**D**
Total cost per Unit	**D+A/(total devices)**

With this kind of information the feasibility study is really completed and the top management can draw its own conclusion on the opportunity to undertake the development.

3.4 DESIGN

Objectives of this section is to describe, for ASICS managers and designers, the tasks, and their good practices, necessary to undertake a reliable computer-based circuit design and test.



The design phase is the heart of the technical operation, and its objective is to provide an unambiguous description of the ASIC to the silicon foundry. This is done by transforming the device specifications, approved in the preceding workpackage, into a computer-based set of files that describe the ASIC in the agreed way to allow the silicon foundry to undertake the manufacture of the chip.
The people involved in this phase are;

1. the designer(s)- i.e. the individual(s) who use the software tools to accomplish such a transformation.
2. the system engineer, the person validates the performances- i.e. the functionality, timing, electrical parameters, package style and size, of the designed chip.
3. the software provider to provide maintenance and technical support to the designer.
4. the silicon manufacturer, who delivers and has to guarantee the cell libraries and the technology on which the design is based-upon.

Of course, the project manager has to be kept fully aware of the work's proceedings.

The main instruments to create such a description are circuit description tools, such as; schematic entry, HDL (Hardware Description Language) or polygon editors together with verification tools, which consists mainly of circuit simulators.
The complexity of the design phase depends heavily on the company's expertise and agreements with the silicon and CAD tool vendors, and on the ASIC type chosen.

For a purely digital design, carried out using HDL description (see below) at RTL level and using synthesis tools, an accepted rule of thumb is a productivity of 1 K gates per week, including pre-layout simulations. However testability issues (see below), CAD tool versions and design complexity can greatly affect the duration of the design phase. For a "first time developer" of an ASIC it is highly recommendable to rely on experienced subcontractors or the silicon vendor to draw a realistic Workplan.

The designers have the responsibility for this Workpackage, but the project manager, system and test engineers, and possibly the Silicon Vendors, have to act and contribute.

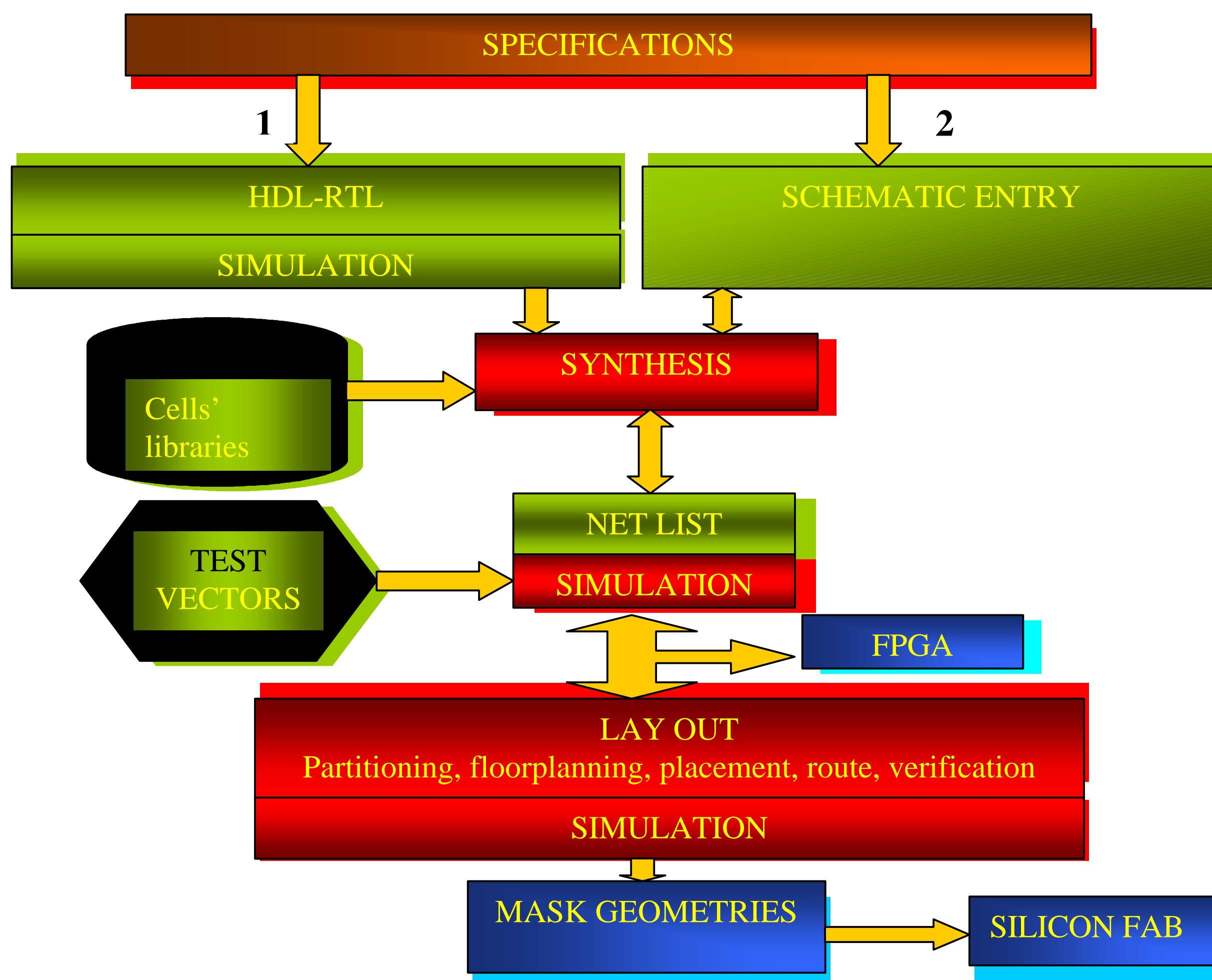
Typical deliverables of this workpackage are the behavioural description, the schematics, test patterns, and the final complete database. A breadboard to test the PLD implementation prior to the silicon vendor's targeting can complement, and provide a higher chance of achieving the deliverables.

In the following a typical design flow for digital CBIC and Semicustom devices is described, these make up the largest part of ASIC market.
Full custom digital, or analogue, and mixed signal devices require a better understanding of the technologies and transistor performance, and of the interactions between the geometries and layout.

CAD tools are mainly used for schematic entry and polygon editor, while simulation is carried out on limited portions of the circuit using SPICE simulators. Placement and routing of analogue designs is today considered an art in itself and requires a lot of experience, as it is done mainly manually.

As explained in the APPENDIX, CBIC and semicustom devices rely upon the availability of cells (simple, such as AND, OR etc. or complex, such as FF, Registers, ALU etc.) which are already tested and certified by the manufacturers. Those cells are used as the circuit building blocks to implement the required functions.
With reference to the following Picture the designer can start its design at two different levels, both supported by current tools:

1- Behavioural description,
2- Gate level design.



Of this phase AE 240 experience has been that " This phase of the AE was severely underestimated largely due to the lack of knowledge in designing a complex ASIC in VHDL. That are two unknowns for the first user, the adoption of a new language to describe a circuit, and its implementation in an ASIC." Furthermore " Each stage in the specification and design process should normally be signed off before proceeding to the next stage. In practice, changes had to be made to the specification as it became apparent that it could not be properly implemented during the design process. The result was that there were a number of design and specification iterations or loops to parts of the ASIC design." For this last consideration, please refer to the relevant chapter in the Appendix.
AE 23295 considers that " the Design Management task is a relevant activity an should be properly manned."

A word of precaution comes from AE 24675: " Of all the project phases, the Synthesis Phase of the project was by far the most demanding and required the most amount of effort."

In summary, before starting the actual chip's design, the following actions/results should have been reached:

- **The right number and talent of personnel is allocated to the Design (managerial result)**
- **Equipments and materials have been foreseen (managerial result)**
- **Realistic goals have been determined (managerial result)**
- **Unambiguous specifications for the ASIC has been agreed upon and fixed (technical and managerial result)**
- **The ASIC type has been determined (technical result)**
- **The Silicon vendor, with the right ASIC type and technology and computer tools, has been chosen and a binding contract has been signed (technical and managerial result)**
- **The test strategy for the parts acceptance has been devised (technical result)**

3.4.1 - Behavioural Description

This approach consists of a functional description, using a hardware description language, of the behaviour of the final chip, and hence a "virtual function chip" is created. As this is just a description of functionality the virtual chip is technology-independent, therefore the design is completely portable as no technological constraints have been added yet. Therefore the main advantage of this technique is that, with such a description a customer can finalise the technology choice, CBIC or PLD and the manufacturer after thorough cost comparison. If necessary the implementation can switch effortlessly from one technology to another.
This stage also includes simulation to be certain that the requested functionality has been achieved.
The description languages used are HDL or VHDL, with the relevant simulators. The most common style used is RTL (Register Transfer Level), and all the most important synthesis tools (see below) support it.
More than 95% of the digital ASIC designs in FUSE has been developed using the behavioural approach.

EXAMPLE: Disadvantages by not using behavioural design
AE 2032 subcontractor was not tooled to design in HDL, therefore the design was captured at gate level. As the chosen technology for prototyping is no more available for production, the Proposer now faces the problem of the complete redesign of the chip and its new prototyping.

If the design has been approached as in par. 3.4.1, then, by using what are called synthesis tools, that "functional design" is transformed, mostly automatically, into a circuit's schematic, or netlist, based on the chosen vendor's cells library.

Synthesis tools offer high reliability and improve efficiency and effectiveness, by optimising the netlist in terms of final area, performance and, consequently, power consumption. In addition they allow implementing DFT (Design for Testability, see below) circuits to improve the testability of the chip, and hence the confidence in a positive result.
For purely digital designs, at this stage Best Practice suggests to target the implementation towards a suitable FPGA.
The FPGA that implements the required functions can be used to test the design in the target environment, and to quickly and inexpensively check and correct possible bugs.
After this FPGA-based check, the design can be retargeted to the chosen silicon vendor.

3.4.2 - Gate level Design

Using the gate level or schematic entry method, the design of a chip is likewise the computer based design of a board, where the physical support is silicon. Instead of components, predefined cells (each with specific function and electrical characteristics, just as a commercial device) are placed and interconnected onto the virtual silicon support.
In this case the design duration takes longer than using the behavioural approach, but, on the other hand one saves the HDL simulation.

When the Gate design entry point has been chosen, the circuit is drawn on the workstation using the cells of the vendor's library to obtain a schematic, in the case of a cell-based design. For a full custom design, the gate level is the only entry point to develop the device, and in both cases, at the end of this phase, the ASIC has a defined manufacturer.
If it is required to switch to a different manufacturer, if the entry point was a behavioural description, there is no need for a complete re-design. However, if the entry point has been at the gate-level, the designer has to redraw the entire schematics, and hence the advantages and disadvantages of the two approaches are evident.

After the schematic has been drawn, functional and timing simulation are carried out to assess the overall performance of the still "virtual" chip. In order to do this a test strategy, and the test patterns (or test vectors or test routines) have to be devised.

3.4.3 Test : Design verification

The test strategy is essential for good practice because through it the compliance of the prototype chip to the electrical (parametric and functional) and environmental requirements are assessed. Therefore the test strategy to be used is essential to the result, and the best solution relies upon the adoption of the following techniques:
1- Stuck-At-Fault ***Testing and Automatic Test Pattern Generation (DFT and ATPG),***
2- At-Speed ***Functional Test Generation,***
3- Quiescent ***Current Test Generation***,
4- FPGA ***implementation.***

1- **Stuck-At-Fault Testing (SAF)**
Stuck-at-fault testing provides a common approach to structural testing for both combinatorial and sequential circuits. This testing method assumes that a logical fault model corresponds to physical defects in the final chip's structure introduced during manufacture.

A "stuck-at" fault refers to a fault in a circuit logic model where a logic element's input or output is "stuck-at" a logical 1 or 0. This corresponds to many possible defects in a chip that all cause a short between a signal and power or ground.
We can presently analyse the "good" circuit model versus the "stuck-at" circuit model for circuits of great complexity. Unfortunate1y, generating tests to accomplish *this* analysis proves difficult unless a circuit has been designed with some type of sequential circuit partitioning.

When a designer follows proper design partitioning techniques, many vendor tools provide automatic test vector generation or ATPG for SAFs. This automatic technique produces signals at input pins that both drive circuit nodes to 1's and 0's and propagate the results to output pins. In the language of stuck-at fault testing, a test set that produces the desired values at a node is said to have “controllability" of that node and a test set that propagates the test result to an output pin is said to provide "observability" to that node. ATPG tools, in conjunction with proper design techniques, can create test sets that give controllability and observability to most of a circuit.

A measure called “fault coverage" determines a fault test set quality. This measure comes from the ratio of the number of circuit nodes controlled and observed by a test set to the total number of nodes in a circuit. Scan design, a commonly available design technique, supports ATPG scan design.

Scan design builds all sequential circuit elements (latches, flip-flops, etc.) into one or more large serial shift registers. These shift registers clock the tests generated for combinatorial circuit elements into place and reads the results, while they simultaneously test the sequential elements.

Design for Testability (DFT) techniques consist therefore in designing and implementing on the chip additional circuitry which allows full controllability and observability of the most part of the nodes of the circuit. Such additional circuit does not interfere with the normal functionality of the device in the normal use, and are known as Scan path, Boundary Scan, Scan/Set, Random access Scan System, BILBO, Linear feedback shift register, JTAG, LSSD etc. As this is not a discussion on DFT, a full explanation of the how's and why's is left to the reader to research in the relevant sources. It must be added, however, that most of the synthesis tools allow the automatic generation of a few of such circuits.

2- **At-Speed Functional Test Generation**

Designers create functional tests to verify a design's functions. If sufficiently comprehensive, these functional tests can serve another purpose. Functional tests, when run at the ASIC's clock speeds or faster, can detect defects that even a very comprehensive stuck-at test set cannot.

To create a thorough ASIC functional test, first test all functional blocks of the ASIC, including all significant data values. While an exhaustive functional test (testing all states, including those caused by differing data values) is not possible, a comprehensive functional test will exercise all desired functional states and all data values that correspond to limits (dynamic ranges) and structural activity (look-ahead, carry, etc.).

3- **Quiescent Current Test Generation**

Measuring device quiescent current after logic activity (after one or more logical states have changed) provides another productive testing form, also known as $\mathbf{I_{DDQ}}$ testing. When repeated several times for different states, this testing can detect many defects that other testing forms cannot. These are the defects that cause an anomalous current because the logical state and the state created

by the defect cause a voltage conflict.

1_{DDQ} test vectors provide a high "toggle coverage." Toggling refers to the test's ability to cause circuit element inputs to transition from a logical 1 to a logical 0 and vice versa. Toggle coverage expresses the ratio of the number of inputs toggled to the total number of inputs in a circuit for a particular test set. Recent published data from a number of companies show that defect levels may drop as much as two orders of magnitude when combining 1_{DDQ} testing with conventional stuck-at fault techniques.

AE 240 testifies, about the chip's test and verification: " The test harness is the ultimate verification between the first user and sub-contractors that specifies correct operation of the design. A proper test harness therefore simplifies the interface between the sub-contractors and reduces the chance of a disagreement over the correct operation of the device. This was not considered properly until the AE began and the first user got into serious discussions with the sub-contractors."
AE 24348 has added a BIST (built-in-self-test) section to its Mixed CBIC ASIC to improve the test pattern fault coverage.

4- **FPGA (or PLD) implementation**

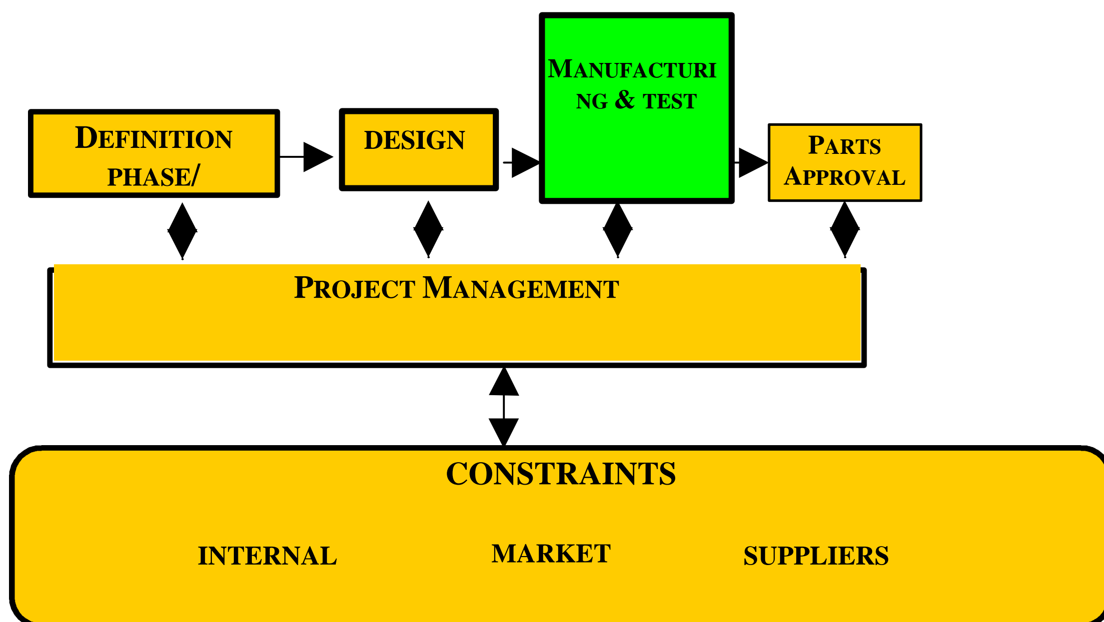
Whenever possible use a behavioural description approach, and a quite inexpensive check should be done by implementing the "virtual" chip in a FPGA. Of course such an approach should have been chosen from the beginning, in order to minimise efforts.
The possibility to get a "pre-run" of the ASIC in a FPGA increases the confidence level of the ASIC's final result and allows the designer to correct design bugs before committing to a silicon vendor. However this should be carefully planned from the beginning of the project, in order not to waste time instead of saving it.

***AE 240**, a very successful ASIC development, got into troubles when trying to implement an FPGA emulation because it is a general good practice, but leaving out of consideration the design complexity. They say: " The time spent in trying to squeeze the design into an FPGA was largely wasted. It became apparent that a software front end connected to the VHDL simulator would give faster results. The number of changes that would be made to the design during the verification phase runs into hundreds. Given that a synthesis, place and route of an FPGA take 4 hours, that makes it painfully clear that it would have taken many more months to verify the design. Instead, the FPGA emulator was abandoned in favour of a software interface to the VHDL simulator that enabled the VHDL model to accept bitmaps as incoming video and output bitmaps as the output video. The time taken to write the front end software was far less than the time it would have taken to do a handful of FPGA design iterations…………… It is very important not to sacrifice rigorous verification through simulation in favour of FPGA emulation."*
*On the other hand **AE 23295** relays the following message: " It is interesting to notice that by means of the FPGA verification a relevant design flaw was identified that would have reduced by half the usable baud-rate of the ASIC Serial Bus interface. It resulted that the problem had escaped to the CAE simulation because it was related with an asynchronous stimuli application, difficult to simulate in a VHDL environment."*

3.4.4 Layout
The layout operation consists in the placement and routing of the vendor's cells onto the virtual silicon floor. Such a placement is usually carried out semi-automatically, in the sense that in order to take into account delays due to interconnections or noise generated by blocks, some of the

circuitry might be better manually placed on the floor.
All the operations are heavily supported by software tools which allow a series of verifications such as; LVS (layout vs. schematics), ERC (electronic rule checker), DRC (design rule checker) etc. These tools are used to highlight hard design errors, such as floating or not connected lines, short circuits, etc.
After the layout verification is done, a new thorough simulation of what is the finished "virtual" chip is performed. If successful the design, in the agreed format, can be released to the silicon vendor.
Lay-out is not required for PLD and FPGA devices.
This phase, according to the vendor's agreements, can be carried out by the vendor itself: if the final post lay-out simulations are not correct a further iteration between the designers and the silicon vendor must be added, adding to the overall time spent.
AE 24348 had the place & route and post lay-out simulations carried out by the silicon vendor: these latter didn't match with the pre-lay-out simulations. The foundry had to correct the BIST section and the company had to update the test patterns.

3.5 MANUFACTURING AND TEST



Manufacturing and test are generally carried out by the manufacturer (remember that the test vectors have to be provided by the customer!), and are therefore the vendor's task according to its own policies and procedures. From the customer's point of view, manufacturing is almost transparent, while it may well be that assistance from it is required by the vendor, in case of marginal results, or failure, of the final vendor's QA test.
Especially for a first user, this phase is not under the customer's direct control and here is a very brief explanation of a manufacturing and testing flow, with the advice that especially for the prototyping phase, some variations are possible. For further information see Appendix I.
The manufacturing process consists of three main phases:

- Masks fabrication, where the necessary set of Masks are fabricated, according to the outputs of the design phase, i.e. the design database.
- Wafer processing, during which each one of the masks of the set is used to define on the wafers a specific pattern (e.g. the pattern of the active areas, the pattern of field oxide for isolation, the

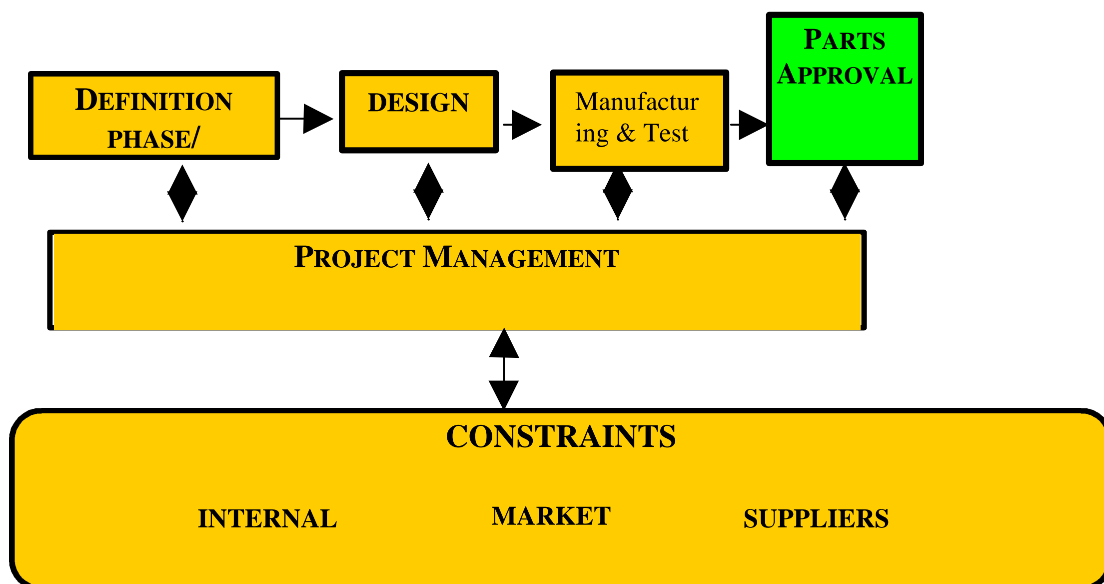
thin oxide's one for gates and capacitors, the polysilicon's, the metals' etc.). At some points during the whole operation, according to the manufacturer's policies, some technological test is performed to insure that alignment of each mask to the previous' is within the limits (TCI, Technology Conformance Inspection), that thickness is correct (PM, Parametric Monitor), basic transistors and capacitors perform within the process capabilities (TCV, Technology Characterisation Vehicles and SEC, Standard Evaluation Circuit) etc..

- Assembly, during which the wafers are sawn into the N chips implemented on each of them. The bare ASIC dice are then glued either into the metal frame (in the case of a plastic packages) or on the conductive cavity bottom of a ceramic package. Each dice pad is then connected, through various wire soldering techniques, to the frame posts (for the plastic package) or to the ceramic package posts. If the package is plastic, then the frame (usually it consists of a continuous strip of frames) is put into a mould, where plastic is hot injected. When it cools, the strip of frames is cut into individual packaged devices and the metal leads jutting out from the package are properly bent, becoming the package pins. If the package is ceramic, after wire soldering, either a metal lid is welded on the cavity, or a ceramic cover is glass-fritted on top of the holder, sealing the device.

Usually a relaxed electrical test is performed on all the dice of each wafer before sawing it, and a thorough one on each of the finished package devices (final test).

The duration of this manufacturing and test phase varies widely according to the technology and the silicon manufacturer (and relevant contract). Usually the array-based devices require anything between four to six weeks, while a CBIC takes between two to four months, for prototyping a number of devices of maximum 10 units.

3.6 PART'S APPROVAL



This task aims to ensure that the manufactured parts comply with the specifications and that the ASIC works properly within the system. The items to check are the quality (manufacturing) and the reliability (duration of the specified performance) of the device and its compliance with the user's

requirements.
As discussed earlier, the ASIC development manager has to understand and control all these aspects, in fact Q&R are the vendor's responsibility, while the compliance with the initial requirements is the sole responsibility of the designers and user.
For Q&R it is "only" necessary to check the QA criteria of the vendor and be assured that these not only conform to the customer's expectancy, but also they have been applied during the fabrication

The test ensures that the device passes Q&R, that the device passes the electrical and functional tests on the Automatic Test Equipment (with the stimuli sequence devised by the designer) in an ideal environment, but the device is yet to be proven in the target environment.
If a PLD has been tested before committing to the silicon manufacturer, then the risk of failure is minimised, if not then before accepting the devices, a thorough test investigation either on breadboard or in the final system must be carried out. As the development of a breadboard takes less time than the manufacturing of an entire system, this approach is usually chosen. The breadboard will allow the elimination of factors that come from the final system, that can affect the performance of the device adversely, but that have nothing to do with the device's characteristic performance.
Such breadboard design and manufacture should be an integral part of the Workplan and should be ready from the moment the devices are delivered. The test of this board can take from a couple of weeks to a couple of months, according to the complexity of the ASIC.

APPENDIX to the FUSE HANDBOOK

ON BEST PRACTICE
IN
ASIC DEVELOPMENT

16/03/99

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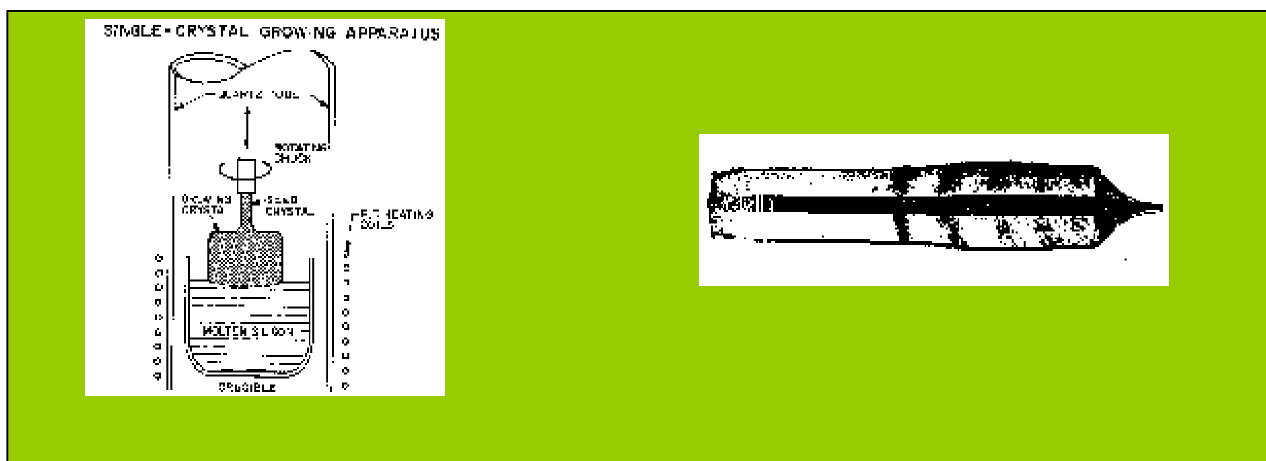
1- Integrated Circuits (IC's) Technologies

1.1- SILICON CRYSTAL GROWING AND WAFERS FABRICATION.

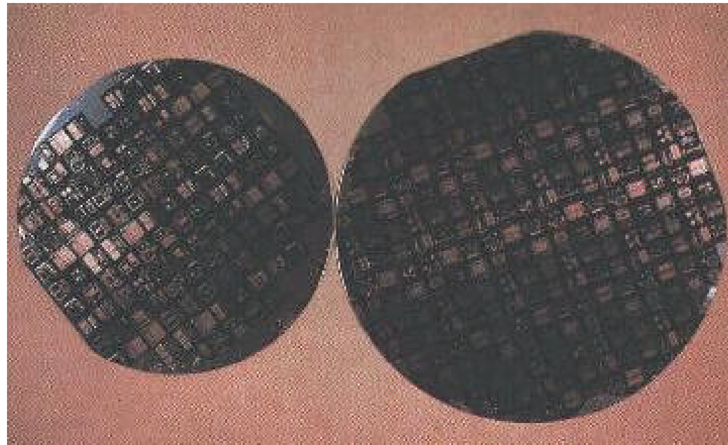
An IC is implemented on a substrate, made of a thin (200 µ or less) silicon wafer. Such wafers are cut from elongated mono-crystals (0.7 metre or more long, and with a diameter of up to 30 cm), which are grown from the molten silicon state onto a seed crystal that establishes and ensures the orientation of the whole silicon. To retain the crystal orientation, a flat reference is ground on one side, and it is maintained along the steps that follows. Also some "dopants" are usually added to the molten silicon to ensure the proper electrical characteristics.
Wafers are cut ("sliced") from the single crystal, by diamond faced saws, perpendicularly to the growth axis. The rough wafers are then polished, by various means, to a mirror finish on one face.
The raw starting material for growing the long mono-crystals is common sand, which has obviously been extensively purified. Below is the crystal growing apparatus together with the grown mono-crystal, on which the reference face has been ground.
Companies other than the device manufacturers (which are improperly called silicon foundries) grow the silicon and prepare the wafers. Wafers, according to the dopants and crystal orientation, are sold according to their diameters, which can reach up to 8 inches. The cost of a bare wafer ranges from a hundred to few hundreds dollars.



1.2- WAFERS PROCESSING

The wafers are then bought, usually in very large numbers by the silicon foundries (the device manufacturers) and processed with their own technologies, to obtain from a single wafer, hundreds of identical electronic ("semiconductor") devices.
The silicon foundries perform three kinds of operations, on the polished wafer surfaces, to reach that goal.
One kind of operation consists in changing the surface electrical characteristics by such means as thermal oxidation, thin films deposition, epitaxial growth, thermal diffusion and ionic implantation.
The second kind of operation consists in defining the areas where the previous techniques must be effective: the typical operations for that are the lithographic processes such as masking and etching of areas.
The third type consists in the fine tuning of the needed final performances by means of annealing and gettering operations while performing the previous operations.

The combination of these various techniques and technological chemistry defines first the process technology, then the implemented device. More than half a hundred of elementary operations are needed to complete a set (lot) of wafers. Below are some finished wafers.

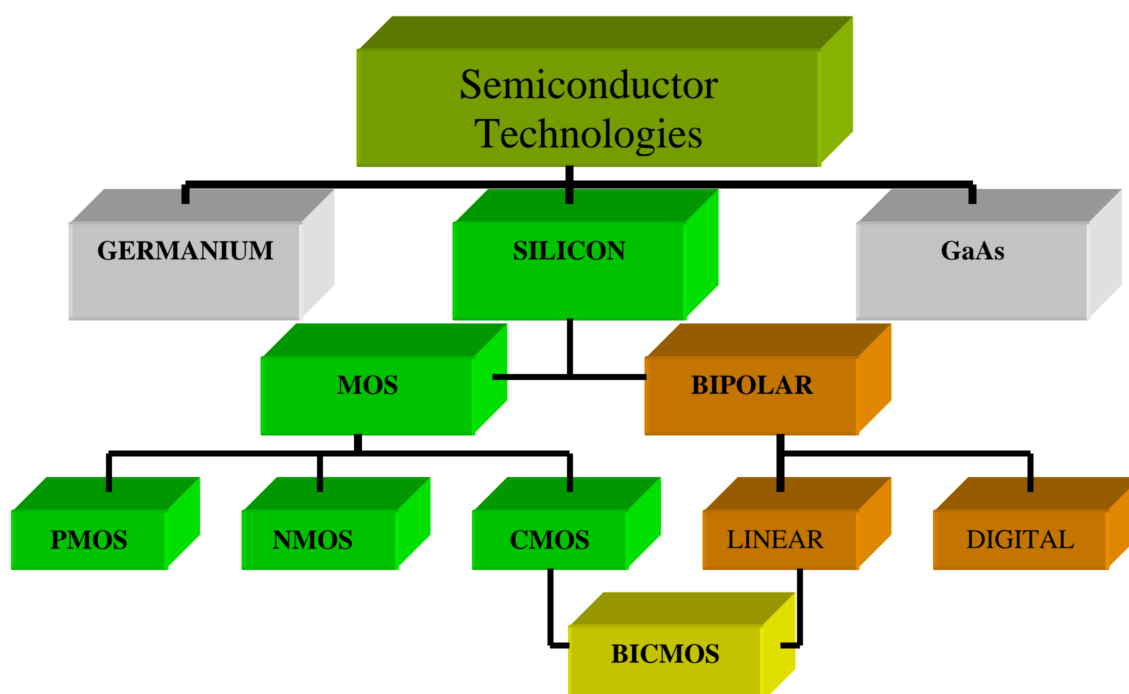


Once a wafer is finished, the circuits on it are individually tested (defectives are marked) and then the wafer is sawn: from a single wafer hundreds of circuits can be obtained. The good dies are then assembled in packages, either hermetic (ceramic, chip carriers etc…) or non hermetic (plastic), after having bonded them to the treated substrate (for hermetic packages) or a holding frame (for plastic) and after having wired the die's pads to the package pins.

At this point is mandatory to understand the following chapter.

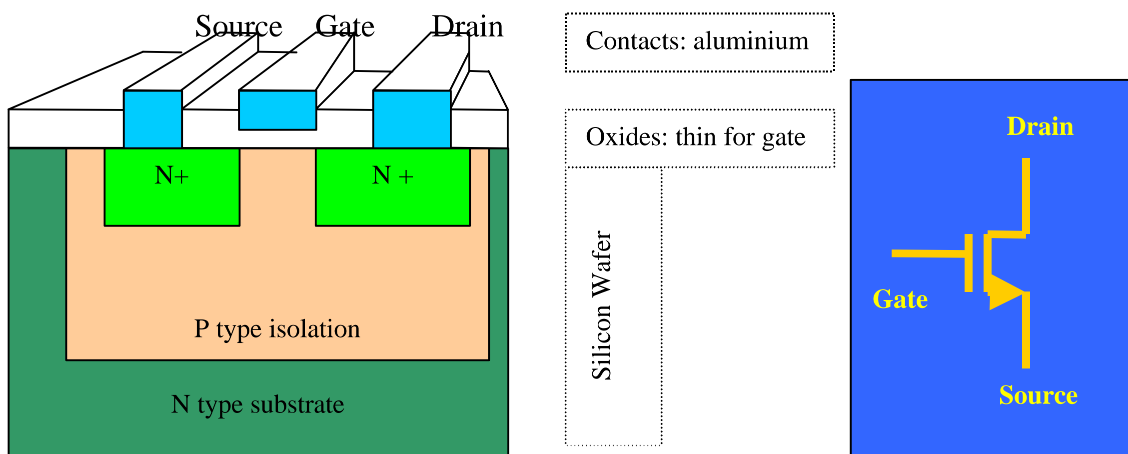
1.2.1- PROCESS TECHNOLOGIES

The combination of the processing techniques, makes up the technology. For completeness the following picture includes process technologies for Germanium and GaAs (Gallium Arsenide): however, these, will not be discussed.



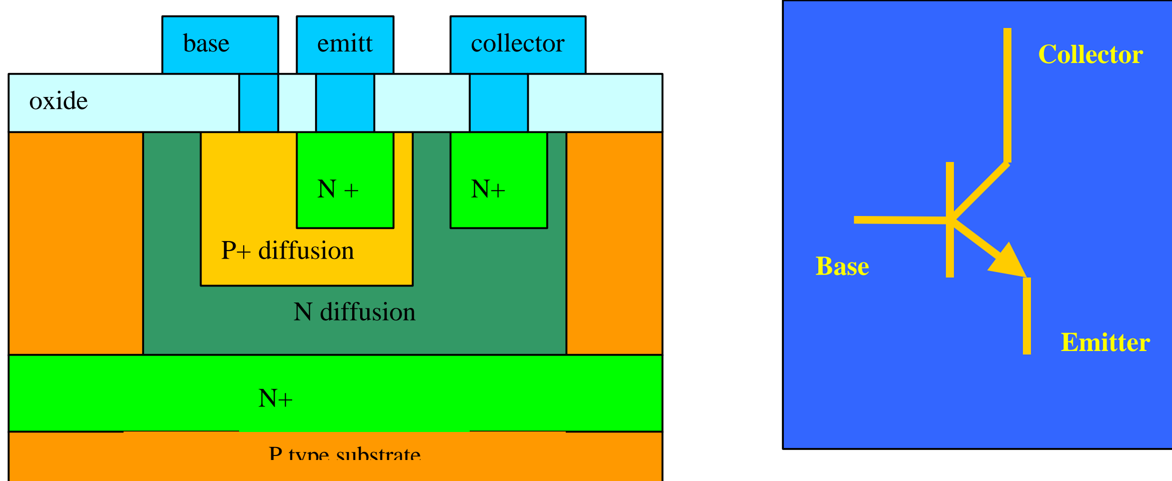
The primary element is silicon, which is divided into two main process technologies: MOS (Metal Oxide Semiconductor) and Bipolar (based on positively and negatively doped areas). These technologies are differentiated by the implementation of the basic active electronic element, i.e. the transistor.

MOS (N-MOS) Transistor: cross section



In this transistor the source and drain make direct contact, through the aluminium strips, to the diffusion underneath (N+ doped, hence the name NMOS), while the gate is separated from the surface by a thin oxide layer. The electrical field generated by the gate modulates the current from the source to drain.
The MOS technology is characterised by the spacing between the source and drain junction, i.e. what is defined the Gate Length, that influences the transistor performance. Today the available technologies range from 1µ to less than 0,35 µ. gate length.

Bipolar NPN transistor: cross section



The bipolar transistor has three terminals that make direct contact with the diffusion layers, i.e. the current in the base modulates the current from emitter to collector. As there is a current flow into the base, in principle bipolar technology is more power hungry than MOS technology, but it can reach higher switching performance.

The size of the diffusion and their reciprocal distances influence heavily the performances of the transistors: for small signal transistors and minimum power driving capability the overall occupied area can be less than one sqµ.

Below each of the main MOS and Bipolar branches, there are dozens of technology variations for manufacturing semiconductor devices, and belong to the six main categories highlighted. At an even further level of detail, each of these technologies varies slightly between individual manufacturers. The degree of similarities becomes critical when alternate sources are required for a custom design.
The processing technologies, such as the different variations for processing MOS devices, all have certain advantages for a specific application, which is usually related to cost and performance.

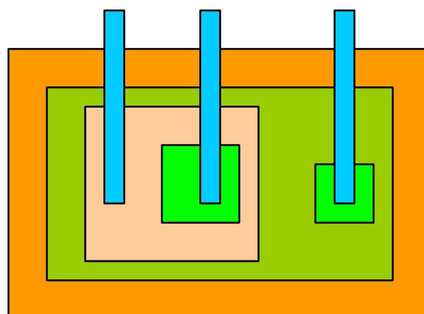
The cost of a processed wafer is, in principle, dependent only on the used processing technology and not on the particular devices implemented on it. For the most popular technologies, e.g. CMOS 0,8 µ , a finished wafer can cost up to 2.000 US$.

A bipolar process can require from 6 to 15 masks operations, a CMOS from 10 to 18, and a BiCMOS from 16 to 26. Of course, between each of the masks operations, the wafers are subjected to all the other physical and chemical operations, described in the previous section, to locally change the electrical characteristics.

1.2.2- HOW ARE THEN DEVICES DESIGNED AND IMPLEMENTED ON SILICON WAFERS?

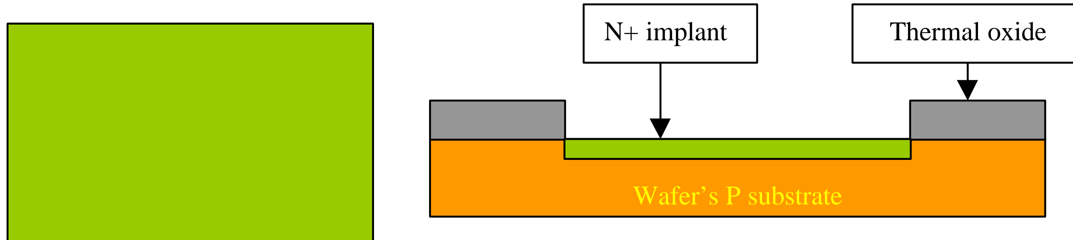
In general, to design a device the device manufacturers need only the appropriate Computer Aided Design (CAD) software tools and a very clear specification of the performance of the technology.
The manufacturer will know exactly how the electrical characteristics of, for example a diffusion layer versus different doping and its concentration, versus its depth or its size. Such technological information, "technology files" are linked with the software.
The software, usually commercial although some device manufacturers have designed software packages of their own and are still in use, allows the designer to capture the circuit. It associates the specific pieces of technology to the various parts of the design captured, runs different kinds of simulations to check the performance, and generates the masks that have to be used to implement it on the wafer.
Each of the masks will allow one specific physical/ chemical operation on the wafer's surface to be performed, such as the doping of certain active areas or the growing of oxide insulation layers, etc.

Below is a very simple example, referenced to the bipolar transistor depicted in section 1.2.2.
At the end of the design, the output from the designer is something like the following, together with the simulation data.

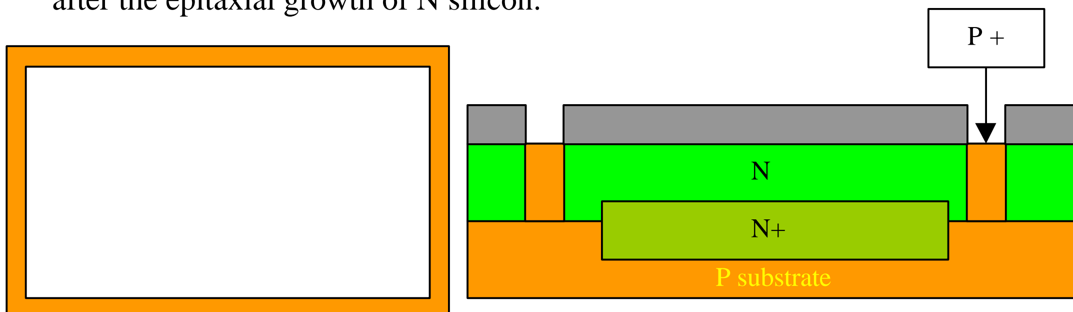


The software package understands and translates that figure in terms of a succession of technological steps, whose order is given by the masks, and shown in a simplified way below.

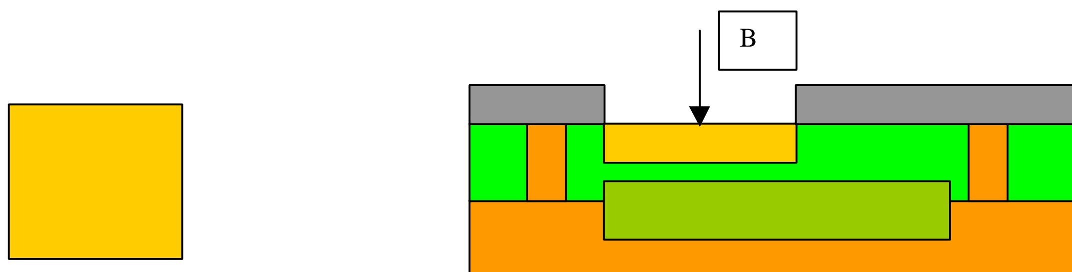
1- the first mask is defined on a chromium plate as a rectangular hole where to implant the N+ buried layer:



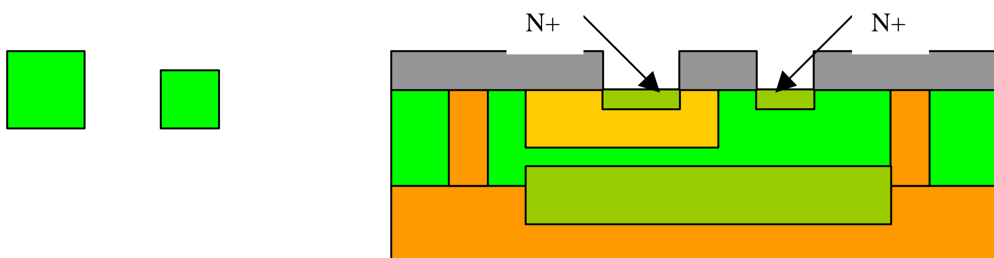
1- The second mask, on a second plate, defines the isolation area, where P+ has to be diffused, after the epitaxial growth of N silicon:



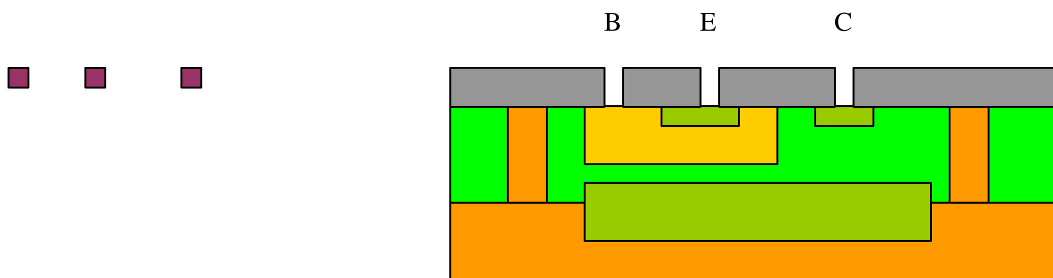
2- The third mask defines the base, to be diffused in P+



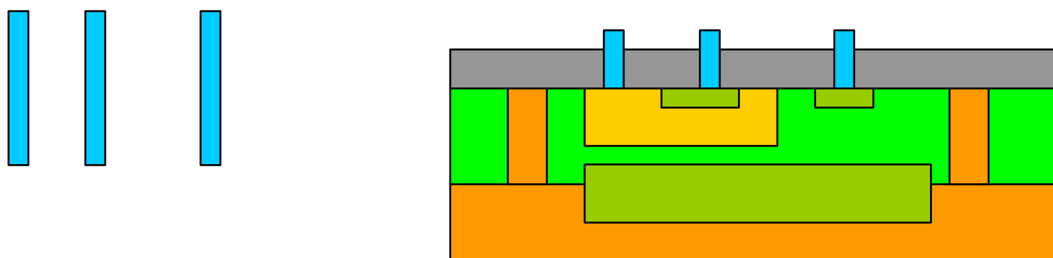
4- The fourth defines the N+ diffusions for emitter and collector



3- The fifth defines the contacts to the diffusions



6- The sixth allows the conductors definition



Each mask, due to the very sophisticated technology needed, is very expensive (around a thousand dollars) ; it carries references to align exactly one to another. They are usually made of optical glass plates covered with chromium.
If the wafer is devoted to the fabrication of that single transistor, the above patterns are replicated (by a photographic step and repeat process) on the plate, which has the dimensions of the wafer to be used.
The process has been schematised, but it can be seen how complicated it is.
Wafers processing, not mentioning the design of new circuits, is quite expensive; that explain why silicon foundries have, and love, to manufacture and sell millions of identical devices.

1.3 - INTEGRATION

When silicon foundries implement simple devices onto a wafer other than single transistors or diodes, i.e. more complex circuits where resistors, capacitors, inductors, transistors and diodes are interconnected on the chip, this operation is called integrated circuit fabrication. Again , due to the small dimensions of the basic elements, still hundreds of identical complex devices find room onto a single wafer.
A few definitions:

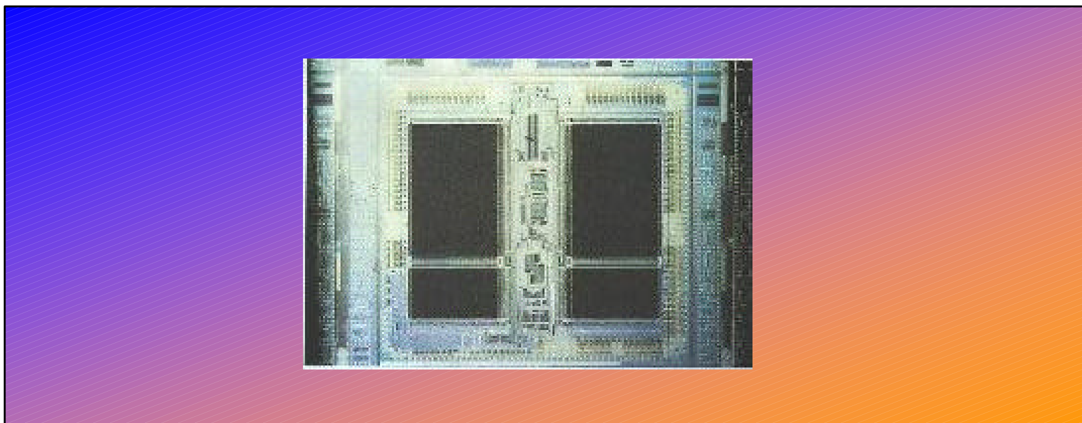
- **Integrated Circuits (IC's)**: Devices that implement, on silicon or other semiconductor materials, passive and active components interconnected to perform complex functions to be packaged with the proper number of pins (from less than ten to some hundreds). Usually the functions to be implemented are:

analogue -such as signals amplifying and conditioning, rectifying, controlling, regulating, etc.
logic (digital) - such as digital additions, comparison, counting, dividing, gating, latching, etc.-
mixed- such as analogue/digital and digital/analogue converters, line drivers, memories, sample & hold amplifiers, sense amplifiers, up to and including microprocessors/microcontrollers and their peripherals.

Integrated circuits can be manufactured as:

- **Standard Components**: Discrete and IC's Devices manufactured in large volumes by silicon foundries, to perform standard functions, and to be used by any customers as building blocks in their design. Those devices are found and sold through retailers and representatives world-wide.
- **Custom Components**: Integrated circuits that perform functions either not attainable through the use of standard IC's, or uneconomical (because of the total price, size, power absorption or other) to be implemented in this way. The silicon foundries (as for a standard IC) manufacture such devices according to the customer specifications and to the foundries' available technologies, for the unique use of that customer. These custom devices are called Application Specific IC's **(ASIC)** .

The picture below is an example of the integration of a complex device.



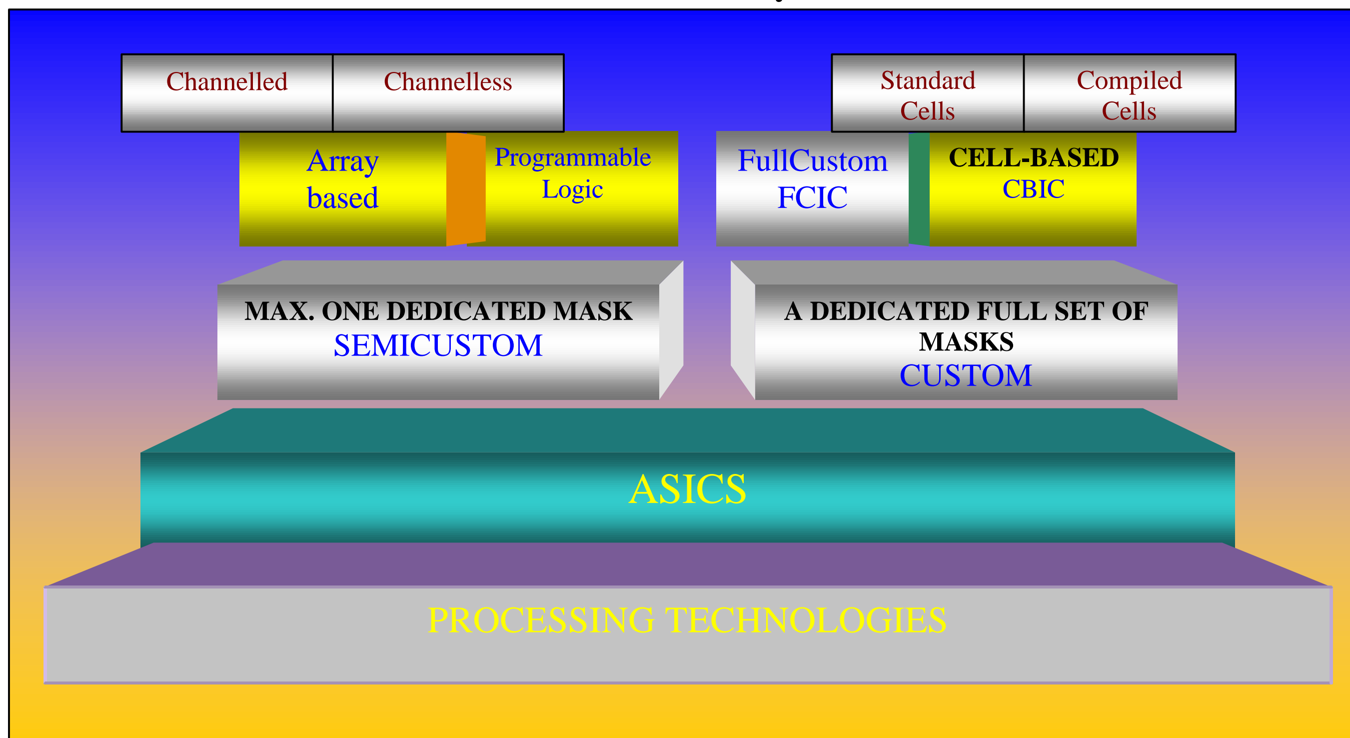
2- ASICS

ASICS are integrated circuits suitable for the use of just one customer, but this does not prevent that user in trying to develop a circuit, which can accommodate for others' users requirements, but that can be only a secondary objective.
The ASICS fabrication technologies are the same as those used by the silicon manufacturer, while the design methodologies are, in general, somewhat different.
In general, the design of an ASIC does not require in-depth knowledge of the technologies' and in addition, the wafer silicon surface is sometimes already pre-processed or, at least the user is provided with a dependable and reliable set of virtual functions, whose manufacturability is guaranteed by the manufacturers.
This is true except for full custom design, which is done exactly in the same way as the silicon manufacturer. It is clear, therefore, that different types of ASICS exist and they vary depending on the availability of pre-processed wafers, on the functions cells available and on the design approach.

2.1 WHICH ARE THE ASIC TYPES AVAILABLE?

The following table is a widely used representation that mixes the two fundamental ingredients that make up an ASIC: the silicon preparation and the methodology used to design the actual circuit on it.

The usual ASIC family tree



The **custom** branch is so defined because, the monolithic circuits can be customised from scratch to satisfy specific users' needs, and therefore a **dedicated, complete mask set** must be used for each different customer.
In the **semi-custom** branch only the interconnections of the **pre-diffused array** of transistors or cells are to be defined by the user, and therefore the masks that need to be developed for each customer are limited to the few necessary for the interconnection (metalisation) layers. As an extreme case of semi-custom devices, programmable logic devices do not need any customer specific process to define the interconnection during the manufacturing stage, since the interconnection can be directly "programmed" by the users through the development of a specific

As an example, when using the custom approach the chip' silicon surface is like an empty drawing board, leaving the designer free to position and interconnect transistors and cells, resistors and capacitors in the best way to reach the minimum occupied area with the maximum performance. When using the semi-custom approach, the designer has a drawing board (the silicon base wafers) which is already filled with a predefined cell (that has various functions) array and the designer has to chose which cells to use and define the interconnections between them.
This first step is defined by the silicon manufacturers, who either prepare the silicon with pre-diffused cells (arrays and PLDs) or they let the customers use the silicon surface as a blank board on which to design the circuit that, later on, will be diffused.

In the following, the ASIC types are defined by the design methodology that will be used to describe the virtual chip.

2.1.1 CUSTOM BRANCH

As it has been discussed in the previous section, the custom branch of the ASIC family is characterised by the fact that the silicon wafer has to be processed fully.

- **FCIC** (Full Custom Integrated Circuit): is a custom ASIC where the customer designs the cells' layout and their connections, mainly by means of handicraft work, so as to fully optimise some of their main characteristic (i.e. speed, area, consumption and linearity). Such circuits, being full custom, by definition can be designed to fit any need and do not require any validated library; however flexibility is paid in terms of development time. This is because the design is done at resistor/capacitor/transistor level, and the final result relies heavily on the designer's own skills.
  An FCIC design has to be undertaken exactly as the silicon foundries design their own standard circuits.

- **CBIC** (Cell Based Integrated Circuit): is a custom ASIC that uses libraries of software standard cells that have already been defined, designed and characterised by the silicon vendor. These cells can have different complexity, can be freely used and interconnected to build up the final circuit, but cannot be modified by the customer (otherwise it would be an FCIC). ICs that are designed by means of silicon compilers are included in this category (compiled cells design); all the others are standard cells based devices.

2.1.2 SEMI-CUSTOM BRANCH

The semi-custom family is based upon pre-processed wafers and therefore a certain number of pre-defined cells, however simple their function, are implemented on the silicon ready to be connected by the customer, according to their requirements.
Therefore the semi-custom branch is equivalent to the CBIC of the custom branch, the difference being that the latter uses software cells, while the former uses physical, silicon-implemented cells.
However, semi-customs and CBIC, from the design point of view, are cells-based devices.

2.1.3 ARRAY BASED

The array based chips come as channelled or channelless, the difference being in the availability of pre-defined "channels" where the metal interconnections must run. The channelless types are therefore more suited where the design has critical interconnections length where inductive/capacitance coupling of lines has to be avoided; this at the expense of a bit more complicate step in the design.

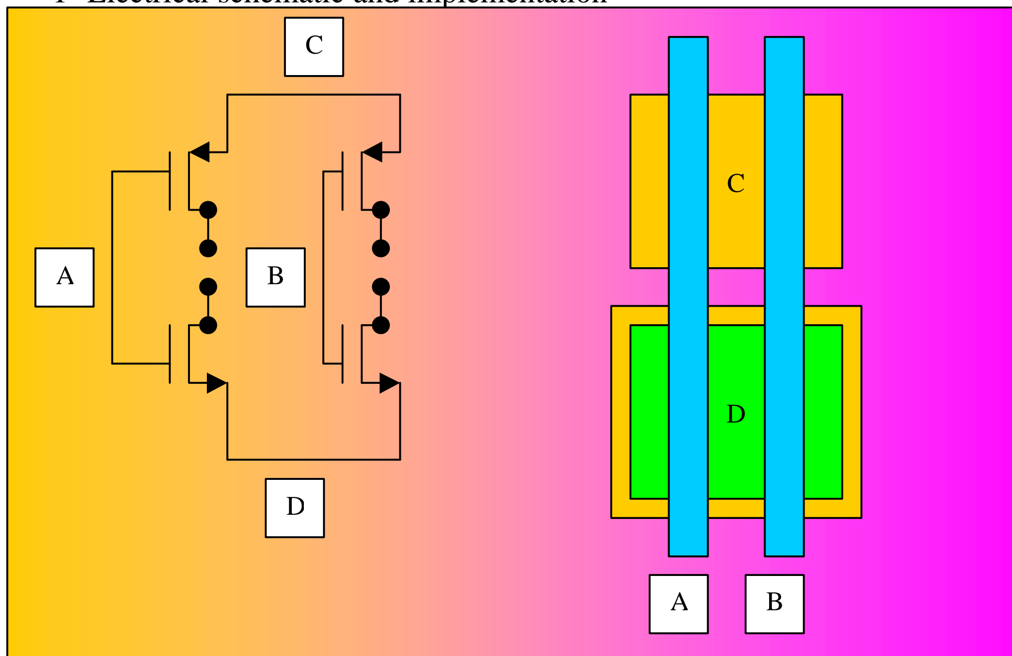
- **G.A.** (Gate Array) is a semi-custom ASIC, which is customised by the vendor, using one or more metal layers to create electrical connections between a pre-diffused array of similar basic cells, in accordance with the user's requirements. G.A.'s are digital devices where the implemented cells are based on simple elements, such a CMOS pair, which cannot be chosen or modified by the customer. G.A.'s can seldom make full use of the gates available, mainly because of the relatively limited routing capabilities. A particular GA manufacturing process that should be mentioned, due to its fast turnaround time, is based on laser technology that

"writes" on the last metalisation layer to personalise the chip. For those reasons G.A.'s are cheaper and faster to prototype, as only one operation (the interconnections deposition or "writing") is required to customise them, but silicon real estate is not optimised and the possibility of analogue elements is strongly reduced.

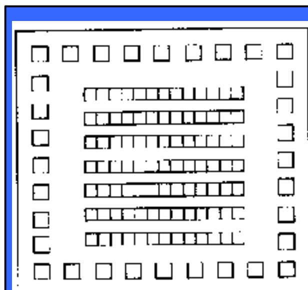
- **Linear Arrays**, which are the analogue version of G.A.'s, are mainly based on bipolar transistors and passive cells, like resistors and small capacitors, that can be tied together to perform the function of several linear ICs. These arrays are offered both in CMOS and bipolar technologies, being the latter more popular. Anyway their diffusion into the market is limited, mainly due to design difficulties, relating to the fact that analogue world often requires an individual functions' customisation that cannot be obtained with a limited set of predefined transistors and passive components. The elementary cell of a linear array comprises *npn* and *pnp* transistors, with different dimensions and some resistors, all of them unconnected. Diodes and capacitors are obtained by using the existing transistors in a different configuration.

CMOS p well Gate Array basic Cell

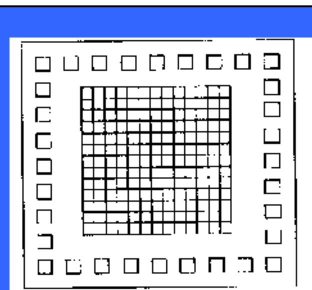
1- Electrical schematic and implementation



2- Channelled GA



3- Channelless GA

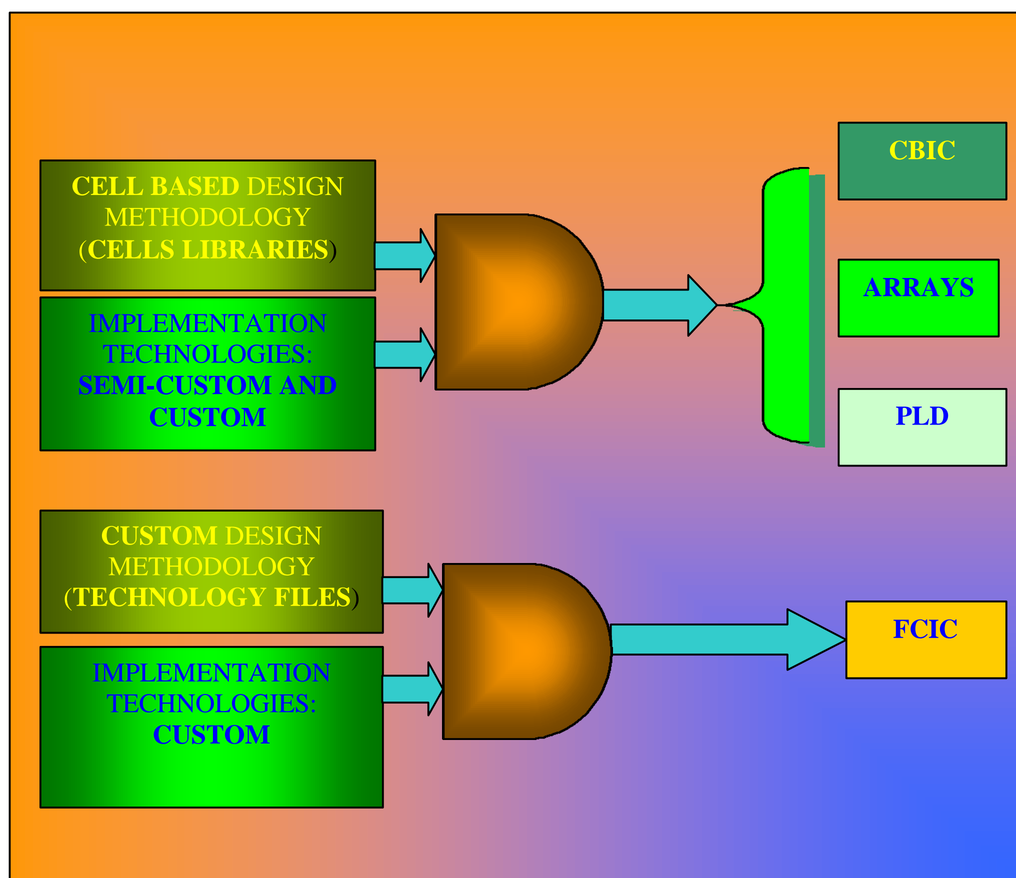


In figure 2 and 3 the small squares at the centre ("core") of the chips contain a string of the cells of figure 1- from few tens to many tens each-; the channels dedicated to the housing of the interconnections are clearly visible in fig. 2.

2.1.4 PROGRAMMABLE LOGIC

- **PL** (Programmable Logic) is a semi-custom ASIC that is customised directly by the customer after its fabrication. These devices can be programmed after manufacturing by means of switches (fuses to be electrically blown or laser cut connections, or static memory cells), which can appropriately tie a system of predefined connections with a pre-diffused array of cells. Although PL are definitely an ASIC Type, they won't be discussed here, as they are discussed in the relevant "FPGA training Material" handbook.

Therefore, the true ASICS tree can therefore be represented like this:



2.2 DESIGN METHODOLOGIES

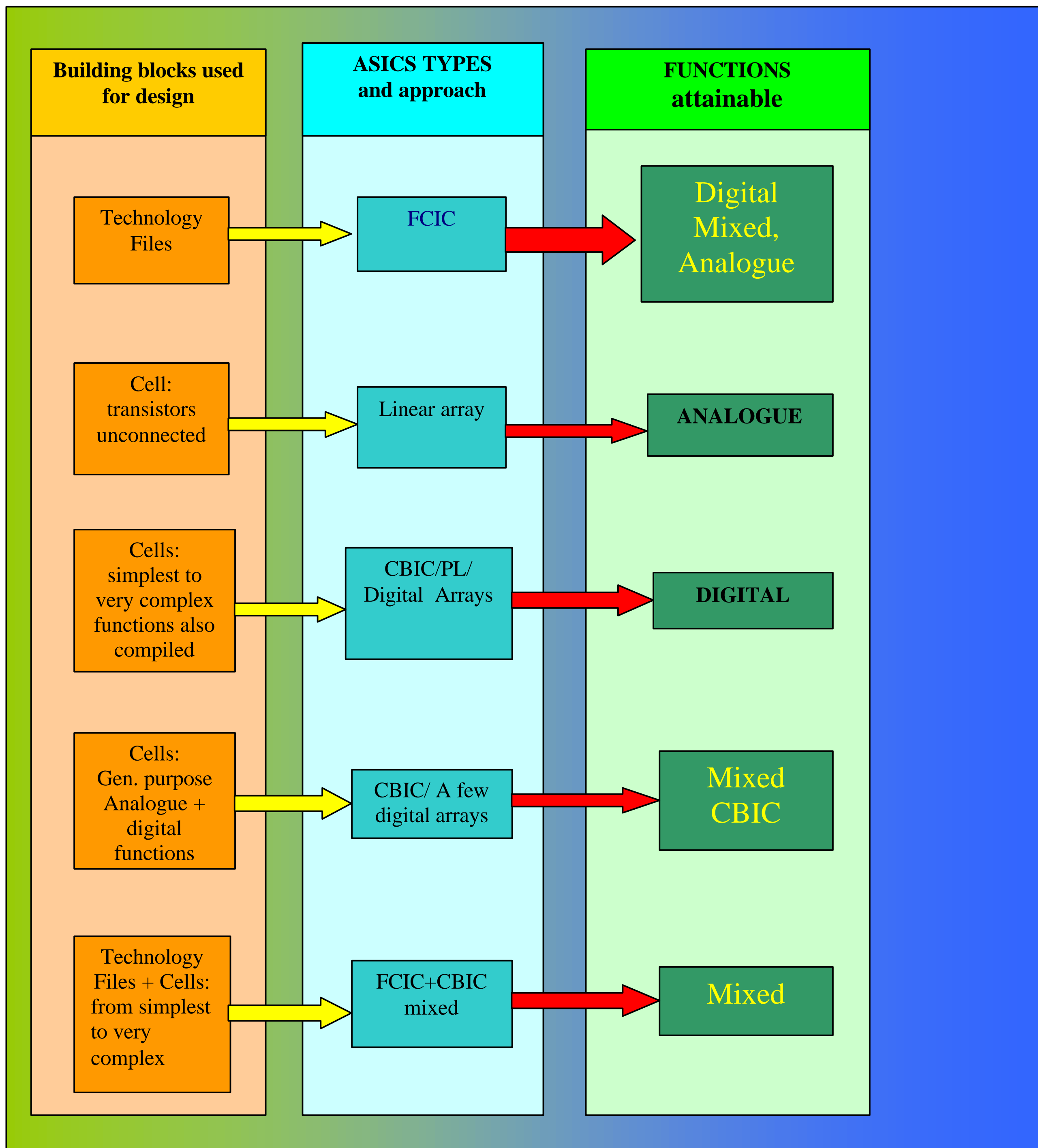
The methodology used to design ASICS is based upon commercial software tools, that can run on Workstation or Personal computers, which enable any Users to design a " virtual" device, simulate its operation, and correct the design, if necessary, prior to its implementation. The current software tools are linked to **Libraries of Cells** or **Technology Files.** The former are made available by the Silicon foundries and consist of **tested elementary functions**, such as gates, buffers, flip-flops, registers, A/D and D/A converters etc. These can be combined together to perform the desired function. The latter, still made available by the silicon foundries, allow the user to design its own transistor or function, when the needed electrical characteristics are not found in the existing libraries, allowing the development of a full custom circuit.

An FCIC (full custom IC) will exploit mainly the technology files to design, at transistors level, the circuit, whose overall functions can be analogue, digital or mixed.
All the other ASICS use mainly the cells libraries to perform the job, and, in general, this method is targeted to design digital functions circuits.

2.2.1 HOW ARE THEN MIXED ASICS DESIGNED?

Mixed circuits are designed either as full custom devices or cell based devices, or the combination of the two.
The full custom approach is easy to understand: the analogue and the digital parts are designed from scratch using the technology files to make each transistor of the complete device.
The cell based approach can attain the title of mixed signal ASIC by virtue of the fact that, in the available libraries, beside a large quantity of different digital tested cells, there are also a few general purpose tested analogue cells provided. **However, these circuits are to be assimilated to digital CBIC devices during design and fabrication.**
The combined approach can still result in a mixed ASIC by virtue of the fact that the digital part is designed with a standard cell approach, while the analogue is designed with a full custom method.
This is the case when the time and economical constraints do not allow for a full custom approach and/or when the analogue cells available in the silicon foundry library do not meet the design's requirements.

Therefore, the world of ASICS, seen from the point of view of the functions attainable from each ASIC family, appears as the following:

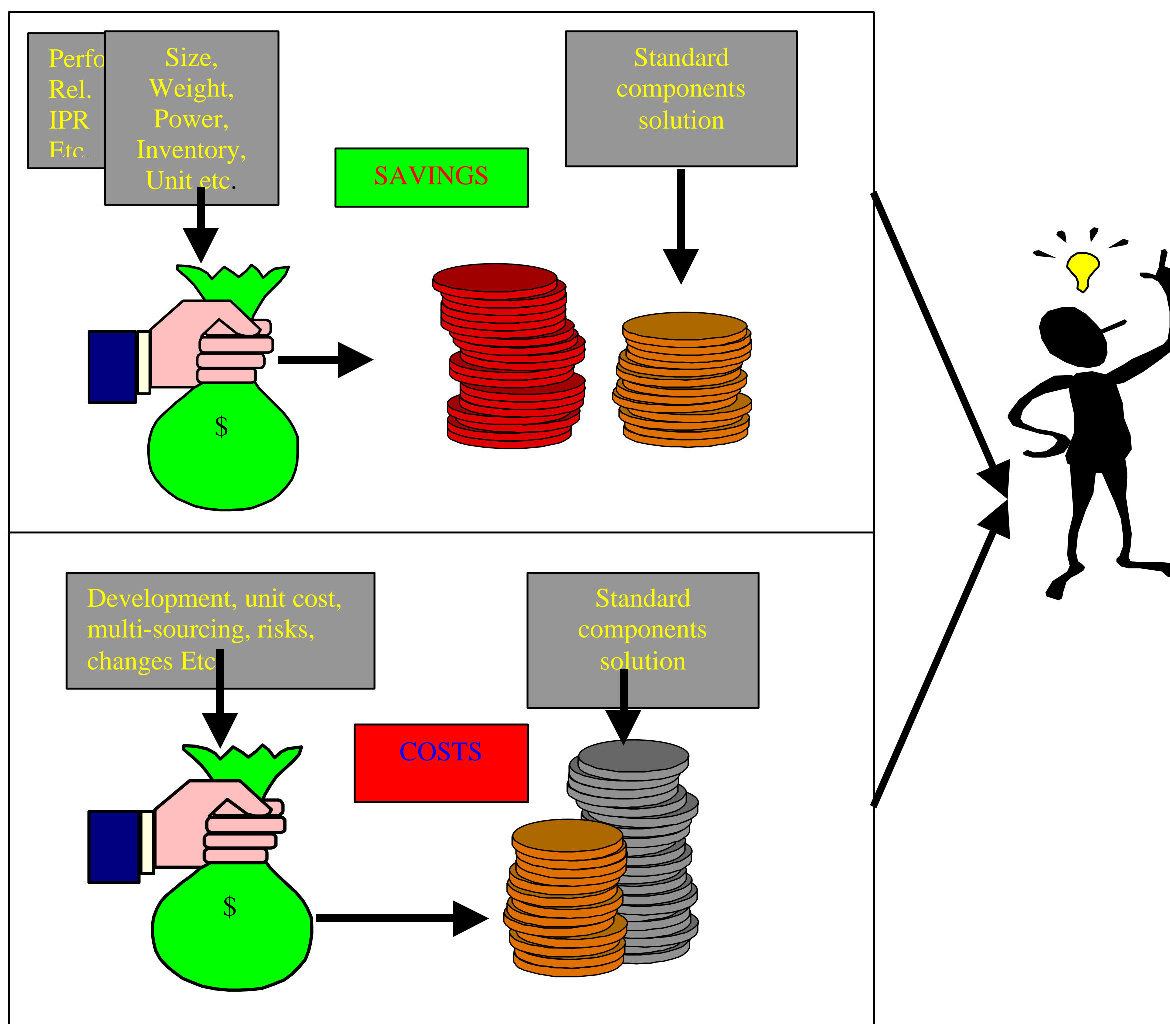


2.3- WHEN SHOULD AN ASIC DEVELOPMENT BE CONSIDERED VERSUS A STANDARD COMPONENTS SOLUTION?

When the financial savings coming from the possible decrease of areas, volumes, weights power requirements, inventory, and unit costs plus the financial increase from the improved performance, reliability, competitive advantage and the intellectual property rights are comparable or higher than the equivalent implementation with standard devices.

2.4- WHEN CAN AN ASIC DEVELOPMENT BE UNDERTAKEN?

The development of an ASIC is justified when the financial costs of the ASIC prototype development (design, manufacture, test) plus the unit costs, plus the quantification of risks, the multi-sourcing difficulties, and the difficulty to change the design at the last minute are comparable or less than the equivalent standard solution.



2.5- USEFUL HINTS

The following gives a few general tables to enable a user to extract the various parameters that have to be taken into consideration when considering an ASIC development.

2.5.1- ASICS TECHNOLOGIES COMPARISONS

Parameter	CMOS	BiCMOS	Bipolar	GaAs
Speed	Med-High	Med-High	High	High
Power	Low	Low-Med	High	Med
Noise immunity	Low-Med	High	High	High
Latch-up immunity	Low-Med	Med	High	Immune
Production costs	Low	Med-High	Med-High	High
Integration	High	High	Low-Med	Low
Fan-out	Low-Med	High	High	Low
Process complexity	Low	High	Med	Low
Sources availability	High	Low-Med	Med	Low

Process Complexity	CMOS	BiCMOS	Bipolar	GaAs
Masks number	13-18	16-26	10-15	11-13
Critical masks/steps	5	6-7	5	3
Process steps	>63	>73	>65	>45
Substrate costs	1	1	1	X 4
Wafers diameter	Form 4" to 8"	4" and 6"	4"	4" and 6"

Silicon capability	CMOS	BiCMOS	Bipolar
Integration density	Very high	High	Med
Power dissipation	Low	Med	High
Clock rate.digital	Less than 200 MHz	Less than 400 MHz	Less than 1GHz
Analogue bandwidth	Less than 40 MHz	Less than 400 MHz	Less than 1GHz
Noise	50-100 $nV/Hz^{1/2}$	Less than 5 $nV/Hz^{1/2}$	>1 $nV/Hz^{1/2}$
Supply voltage	3-12 V	3-40 V	3-80V
Driving capability	Low	High	Very high

2.5.2 ASICS COSTS

	Customs		Semicustom	
Parameter	Full Custom	Cell Based	Gate array	PL
NRM	Highest	High	Medium	Lowest
Design Time	Highest	Medium	Medium	Lowest
Redesign flexibility	Lowest	Low	Low-med	Highest
Production Unit Costs	Lowest	Low	Medium	Highest
PCB costs	Lowest	Low	Low	Medium High
Density	Highest	High	Medium	Low
Second sourcing Diff.	Highest	Medium	Low-med	Lowest
Masks costs (in NRM)	High	High	Low-med	None
Iteration Costs	Highest	High	Medium	Lowest
Layout Flexibility/Effic.	Highest	Med-high	Low-med	Lowest
I/O flexibility	Highest	Med-high	Low-med	Lowest

2.5.3 PARAMETERS AFFECTING THE COSTS FOR PROTOTYPING AND PRODUCTION

1- Die area or size of the chip. The smaller the size, the lower the price.

This is due to the defect density of a process, as, statistically, each process has a determined and fixed number of defects on the wafer's surface. A larger area chip has a higher probability to be affected by a defect.

2- Chosen process. The fewer the process steps, the lower the price.
The finer the technologies' dimensions, the higher the price.
The older the technology, the riskier the undertaking.

3- Packages. The fewer the pins, the lower the price
A plastic package is always cheaper than the equivalent ceramic.
However, when the die size is small but requires many pins it is necessary to use packages with larger-than-necessary cavities to accommodate for the exceeding pins (Pad limited). Conversely, on other occasions and when the chip core is large and needs few pins, use the package with a large cavity and leave the pins unused (Core limited).

4- Quality and Reliability. The more complex the chip the more expensive it is.
The higher the Q&R levels, the higher is the price.

5- Prototyping methods. Single tooling is the most expensive while Multi Project Wafer is the cheapest. The first approach describes the case when one wafer run is dedicated to a single customer, while the second approach applies when many customers have their designs copied together on the wafer. This choice should be made when the volumes for production are determined enough.

6- Production manufacturing methods. For high volumes (> 10.000 devices per year) the single tooling approach is more convenient whether in terms of unit price or in terms of general services by the manufacturer. For low volumes MPW should be preferred. It is not convenient to prototype in MPW and manufacture in single tooling, as masks have to be redrawn and, sometimes, also the prototyping has to be repeated.

2.6- DESIGN FOR TEST (DFT)

Objective:

To present concepts to designers for making a circuit economically and thoroughly testable.

Design for test (DFT) facilitates economical device testing. Therefore, specific design approaches have evolved to make devices more readily testable.

All DFT approaches entail making trade-offs. For instance, many approaches require extra chip area or gates. Some techniques require additional device fabrication steps. The essential trade-off in DFT work occurs between the test circuitry costs, and test development and execution costs.

In this guide we focus on stuck-at fault testing. "Stuck-at" refers to a condition where a defect causes a circuit node to become "stuck" at a logical one or logical zero. A wide segment of the VLSI industry has adopted this testing approach because it can effectively create tests for large,

modem VLSI designs with moderate present-day workstation computing power. Many tools have been marketed that support both the automatic generation of stuck-at fault test circuitry and the automatic generation of stuck-at fault tests (often called "stuck-at fault vectors"). These methods reduce the engineering time required for test generation.

In addition to stuck-at fault tests, designers must develop tests to show that the device's functions and parametric performances match the functional requirements of the device.

Stuck-at fault tests help to show that a design's logic circuit is accurately represented in every manufactured part, and that a manufacturing defect has not caused a distortion in a particular part's logic structure. CAD tools can usually automatically generate stuck-at fault tests. The tools generate these tests through a basic analysis of a design's structure, regardless of the functions the structure is meant to deliver. This narrow focus means stuck-at fault tests have little ability to test for intended function and performance;

For example, stuck-at fault tests can ensure that a counter has eight registers electrically wired according to the schematic. However, they have no ability to test that the original schematic properly described a circuit that would propagate an overflow when its count reached 64K. Tests to accomplish this are called functional tests and, at present, CAD tools cannot automatically generate them.

ASIC DFT has evolved around two major ASIC areas, I/O tests and internal tests. I/O tests involve an ASIC device's input and output pins. Internal tests focus on the device's core logic.

2.6.1- I/O TEST

I/O DFT techniques involve injecting signals into a device through its pins. Some techniques, such as that described in the IEEE standard 1149.1, call for a pin set added to provide this function. This small pin set forms a "test bus" that tests many devices in a board or system with a very little interconnect overhead.

Many I/O tests are based on a technique known as "scan design." Scan design uses latches or flip-flops configured into a serial shift-register chain to pass test signals around a device and pass responses back to the outside world for analysis.

SCAN DESIGN

"The goal of scan design is to achieve total or near total controllability and observability in sequential circuits."

Scan design aims to achieve total or near total controllability and observability in sequential circuits. In this approach engineers design the ASIC flip-flops, latches, or both, to operate either in parallel (normal) mode or serial (test) mode. In the normal or system mode, the flip-flops and latches are configured for parallel operation. In test mode, the flip-flops and latches are loaded (controlled) by serially clocking in the desired data. In a similar fashion, engineers observe the data present in the flip-flops, latches, or both, by clocking out their contents m the serial test mode.

The basic element in scan design is a multiplexer placed ahead of each flip-flop, which is controlled for normal or test operation

The multiplexer switches data between a scan in test signal and data, representing normal or system information. A select control line controls the switching. On the first scan design cell, the serial input connects to the primary input pin (Scan in). On intermediate cells, the serial input comes from the previous cell's output (Out signal). On the last cell, the output (Out N) connects to the primary output pin (Scan out signal). Selecting the test or serial mode creates a complete serial shift path from input pin to output pin.

BOUNDARY SCAN DESIGN

Boundary scan design extends the scan design idea to a board (system) or an ASIC level. This technique solves problems resulting from the combined effects of rising test equipment costs and difficulties in dealing with surface-mount technology. This technique places a boundary scan cell next to each component pin. Combined with scan design, as described above, boundary scan cells allow engineers to control and observe signals between chips. Besides their connections to the package pins and the internal chip logic, the boundary-scan cells have other terminals through which they can be connected to each other, forming a shift-register path around the periphery of the ASIC.

During normal operation, data passes between pins and internal chip logic as if the boundary-scan cells were not there. When put into the test mode, however, the test program directs data to pass along the shift register path. By loading data into the boundary-scan cells, the boundary-scan cells can inhibit data flow to or from the I/O pins, so that engineers can test either the internal logic or the external chip-to-chip connections.
The access to these component pins provides unique advantages to the test engineer. Using a shift path, arbitrary values can be loaded into the flip-flops and data can be extracted from those *flip-flops.* This enormously simplifies the pattern generation required to create tests for the ASIC logic.

To access the boundary-scan cells requires additional I/O pins on the ASIC. To communicate with the boundary-scan cells requires some additional logic on the ASIC. A procedure is also required for device testing. These requirements led to an IEEE standard: ANSI/IEEE Standard 1149.1 IEEE Standard Test Access Port and Boundary-Scan Architecture. This standard defines the I/O pins, control logic, and test tools required for boundary-scan testing *6f* the ASIC device. The standard gives details on expansion of the tool set for particular chip design. It also defines a method for communicating test instructions and data from an external processor to the ASIC.

Boundary scan benefits and penalties

The decision whether to use B-Scan usually involve economics. Designers often hesitate to use B-scan due to the additional silicon involved. In many cases it may appear that the penalties outweigh the benefits for an ASIC. However, considering an analysis spanning all assembly levels and all test phases during the system's life, the benefits will usually outweigh the penalties.

Benefits

The benefits provided by boundary-scan include the following:

- lower test generation costs
- reduced test time
- reduced time to market
- simpler and less costly testers
- compatibility with tester interfaces

- high-density packaging devices accommodation
- easy field support and maintenance.

Penalties

The penalties incurred in using boundary-scan include the following:

- extra silicon due to boundary scan circuitry (between 5% and 10%)
- added pins
- additional design effort
- degradation in performance due to gate delays through the additional circuitry
- increased power consumption

2.6.2- INTERNAL TESTS

Internal tests involve ASIC device internal core logic testing. We will discuss five approaches for this testing: level-sensitive scan design (LSSD), scan path, scan/set logic, random-access scan, and self test with BILBO. These design practices all use a circuit's inherent sequential logic to partition a circuit into easily testable combinatorial logic blocks. They accomplish this by interconnecting the flip-flops and latches into one or more serial shift registers through which engineers can inject tests and observe results.

LEVEL SENSITIVE SCAN DESIGN (LSSD)

LSSD is IBM's discipline for structural DFT ability, which addresses the problems associated with implementing the scan design. This design practice augments the scan design concept by making the scan cells level sensitive. In a level-sensitive system, the steady-state response to input changes is independent of circuit and wire delays within the system.

LSSD imposes constraints on circuit excitation, particularly in handling clocked circuitry. Using this technique provides a circuit immune to most anomalies in the clock's AC characteristics.

SCAN PATH

Nec introduced Scan path in 1975. This technique has the same objectives and uses clocks as LSSD, however, instead of being level sensitive, scan path is edge sensitive.
the scan path. At any other time, clock 2 and its output will be blocked.

SCAN/SET LOGIC

Scan /set logic, set forth by Sperry Univac uses principles similar to LSSD and scan path. Scan set logic, unlike scan path and LSSD, uses shift registers independent of all system data paths and latches.

Upon loading the N bits of the shift registers chain, a shifting process can occur, and the data can be scanned out through the Scan Output pin. This system also supports a set mode. In this mode, the Scan Input signal funnels data into the N bit serial shift register via the Scan Input signal and then appropriate clocking logic loads this data into the ASIC core system latches as required.

These internal tests aim to partition sequential networks into combinatorial networks for ease in testing. For the scan/set technique, the test pattern must set all latches in order to transform each partition under test to a combinatorial network.

This technique allows the scan function to occur during normal system operation: that is, the N bit serial shift register sampling pulse can occur while system clocks drive the ASIC sequential core logic. This allows diagnosing the sequential machine without degrading system performance.

RANDOM-ACCESS SCAN

Random-access scan, put forth by Fujitsu, provides another technique for internal ASIC testing. This technique also reduces the test generation to combinatorial tests and combinatorial fault simulation. Unlike other techniques, random-access scan does not employ shift registers. Instead it implements an addressing scheme that can uniquely select each latch. The addressing mode resembles that used for random Access Memories, and hence its name. This technique, which requires three-four gates per storage element (compared with the two latches for the other scan approaches), provides observability of any point in the combinatorial network. Extra pins are needed (from six to twenty) , according to the modalities for the addressing approach.

BILBO SELF TEST

The Built-In Logic Observation technique uses Scan path, LSSD and signature analysis to self-test a circuit, where the signature analysis, or pseudo-random pattern, is obtained through the implementation of linear- feedback shift registers. Signature analysis is most useful to test data bus structures, such as microprocessors and microcontrollers.

BILBO technique may reduce the number of test patterns, with respect to the other techniques, by a factor of 100, but it requires more silicon area, as it needs about two EX-OR's per latch, and that slows down the data path.

3- PROJECTS MANAGEMENT

3.1- GENERAL

All the documents produced for and during the Project should be named, either with mnemonic codes, or other, and referenced to a particular WP. The front page should bear those items, together with the issuing date, the author's name and signature, the names and signatures of the verification and approving persons, the kind of circulation allowed and which is the current revision.
When revisions are performed, then the second page should contain a table where the variations to the original document are reported, which pages have then been substituted, at which date, in order to give a history of the documents' evolution. The document itself can have adjoining pages with different dates and different revisions as this procedure allows to highlight, print and distribute variations.
All of the pages of the documents should be numbered (possibly as Page n of N), and bear the documents' name, revision # and date.

Any serial development process, such as an ASIC development (but the same considerations hold when complementary, time-parallel activities, are necessary) , has each step (Workpackage or Task starting when the previous step's outputs are fixed. Therefore great care in fixing the rules governing the quality of the interface between each step is mandatory to avoid misunderstanding and waste of time.
Milestones. methodology rule, to avoid such misunderstandings, is making a formal milestone meeting the responsibility to accept the results from the finished workpackage or task, and to transfer them to the next one. In case of parallel activities, that the results of the complementary Workpackages or tasks match with the expected requirement. These results have to be released in the form of hard evidence (a piece of hardware, documentation) and the milestone meeting's attendees should include people from the finished Workpackage and from the one to be undertaken.

3.2- REVIEWS

The review, to be held in between the start and end of each task, and milestones meetings has the objectives to assess these main issues :

Status of the activity vs. the expected (from the Workplan) schedule,
Status of the activity vs. the expected technical results ,
Status of the documentation,
Causes of concern,
The information is archived after having been agreed upon by all attendees in an appropriate meeting, this should list the results of the above items and any actions to be taken, by whom and when.

If the definition phase is completed carefully, then the review or milestone should run smoothly, expect for a few minor adjustments to the documents (specs) and time-scales are allowed, provided that such changes can be absorbed by the overall plan.

3.3- DEFINITION OF WORKPACKAGE, TASK, SUBTASK:

A Workpackage is defined as a set of activities carried out, usually by a homogenous (in terms of competence and tools) group of people and whose output can be considered a finished stand-alone result. Each of the activities that make up a Workpackage are called tasks, whose results represent a semi-finished product, which, summed-up with the results from other tasks of the same Workpackage, make the finished Workpackage result. Sometimes, in order to control sensitive tasks, it is advisable to break them down into subtasks. Any Workpackage end corresponds to a

milestone of the project (also some tasks, due to the importance of the relevant activity, can end with a milestone). At this point a milestone meeting should be held to assess the progress of the work with respect to the original scheduling, and to retune, if necessary time scales and documentation.

3.4- PLANNING: TOOLS AND METHODS

Planning in theory is a simple matter, but doing it properly i.e. to make it effective, is totally a different matter. It is easy to plan in an approximate way, but the risks associated with this are very high and out of any control. Therefore, as ASICs are costly, it is mandatory to plan as accurate as possible.

Planning is an iterative process: first a coarse view of activities and requirements and results, possibly a first adjustment, then an accurate analysis of each of the foreseen activities (for requirements and results), then back to the overall picture for reassessment and retuning. The use of appropriate techniques can avoid double or triple iterations with respect to the previous description, allowing for a saving in both time and resources. Below is a brief description of the main techniques available to achieve a good and credible plan in a short time.

Planning is based upon the adoption of one of the following techniques:

GANNT, or bar diagram,
PERT,
GERT.

GANNT or bar diagram is the simplest one, as it represents the flow of activities along a time scale. It is the favoured methods for SME's as it does not require a specific skill and it is easily understandable. Its name comes from the name of the engineer who refined it into an actual form.

PERT (Program Evaluation and Review Techniques) is suitable for complex Projects, therefore it is a probabilistic representation, based upon a net of arcs, which represent the activities, and nodes which represent the start and end of the activities. The main assumptions of this method are:

Duration and costs of the activities are independent variables,
A " Critical Path" is a sequence of activities that reach an expected result in the least time,
Critical paths have a Gaussian Distribution,
Critical paths are determined on the basis of an average duration, while non-critical paths, although exhibiting a higher variance, are not used to evaluate the time required for the project completion.

PERT is seldom used for innovation projects, as it is too deterministic and it does not allow flexibility or alternate solutions.

GERT (Graphical Evaluation and Review Techniques), is a PERT modification, where the net is aleatory, with nodes which represent logic operations, and probabilistic arcs with aleatory parameters representing activities and requirements, such as duration and costs.
The innovation of the method consists in the fact that nodes exhibit a receiving part and a transmitting one, where the receiving part can perform the simple boolean operations AND and OR. AND means that the node is activated only when ALL the activities entering in it are completed; OR means that the node is activated when any one of the activities connected there is finished.
The transmitting part of the node can be either deterministic, i.e. the activities that depart from it can start only when the node conditions are met, or probabilistic, i.e. each departing activity has a predetermined probability to start AFTER the node conditions are met.

This method is useful for very complex projects, including innovation projects, but oversized for most Asics's developments.

Therefore the simple GANNT method is, at first glance, the most useful for Asics's development projects and all what follows is based on it.

GANNT is built by splitting the project into hierarchical structures regarding ACTIVITIES, RESULTS or PRODUCTS (down to the elementary ones). This is more complicate to say than to do and, in fact, it consists in a matrix where activities are reported in the rows, and the expected results are allocated at the intersections with the columns, which represent time. Therefore every intersection is characterised by the couple " Activity/Result" that represents the minimum indivisible parts of the project.

Such project structure decomposition is named PBS (Project Breakdown Structure) or, at all practical effects equivalent, WBS (Work Breakdown Structure). The result is that the project is completely and minutely described, level by level, allowing the necessary planning and control of the project itself.
Projects elements, characterised by the measurable quantity " Obtained Result/ Finished Product", and by the resources needed to accomplish it, together with the time and costs allocated, and by the responsible (organisation or individual) for delivering it, is called PP (Project Package) or WP (Work Package).
The organisations participating to the project, including all and any externals (suppliers, researchers etc.) are organised hierarchically into the OBS (Organisation Breakdown Structure).
OBS and WBS can be, in turn, described in a " Responsibility Matrix", where, in the rows, Workpackages are indicated, and, in the columns, the organisation or individuals.

Therefore, using appropriately WBS and OBS, the whole project can be planned and fully controlled, and the same methodology can be used to compute the overall budget of the project and its expenditures flow.

3.5- PROCESS ANALYSIS.

GANNT, WBS and WP's are based upon the minute description of each and any elementary activity, in order to understand the needs, costs and times, and monitoring methods. A good method is to dissect such activities, from now on called Tasks (with a upper-case T), by the process analysis method, that can be performed in many equivalent ways, from the descriptive form to the pure graphical one. The final result has to be the same, i.e. the complete visibility of any issue concerning the Task.
Two pieces of information are needed to perform correctly a process analysis: the output result or product needed at the end of an activity and the inputs available. At this point, the problem is as simple, or as complicated, as drawing a line connecting two points. There is an infinite number of curves that can satisfy such requirements, but only few, and very often just one, can satisfy the given boundary conditions.
The duty of the project manager and his team is to find the best curve between input and output that satisfies the constraints.

The Overall Process Analysis Table of the Definition Phase Workpackage might look like this :

Definition Phase	
Objectives	Definition of Technical Requirements, Verification of Technical and economic feasibility, Estimation of costs, timings and risks
Inputs	System technical Spec.'s, (Functions, performances, complexity, reliability, size and weight, etc.), System expected costs, System expected time-to-market, Architectural and/or electrical schematics, Silicon foundries Technologies, Prices (NRE and Volume production) and delivery times, interfacing characteristics, EDA tools available and their compatibility with Silicon foundries, or EDA tools providers, with prices and delivery times, and interfacing characteristics, Available resources (manpower, instrumentation and financial) and needed experience.
Outputs	**Requirements' Document** containing the Identification of Functions of ASIC and System, the ASIC Specifications, Estimation of its costs, size, features etc., Estimation of development time and manpower, Subcontractors choices, all the rationales for justifying the undertaking of the Project. Scheduling or Workplan of the Project, containing a Description of the various Tasks in which the project can be broken down, the identification of checkpoints and alternate steps (if necessary), a Project Time schedule (highlighting the critical points, indicating alternate routes), an overall Costs and Manpower estimate, the various partners and their roles, the Set of Checklists to be filled in to facilitate the follow-up and control.
Who Participates and how to the definition phase	Technical Project Manager- Leader- 15 days, XY- Asics designer- advisor- 30 days WZ- System Engineer- advisor- 20 days XZ- Mktg. Manager- 2 days YW- Production floor Engineer-2 days XW- Silicon Foundry Representative- 3 days etc....
Who checks and how the Project	Technical Project Manager- fills-in the checklists at the foreseen timings, calls a meeting every Monday morning and when requested, The tasks leaders fill-in the relevant checklists of their tasks.
Other Aspects to be considered	The ASIC specification must be signed by the ASIC Designer, accepted by the System Manager, approved by the Project Manager. The leaders of each task have to provide the proper summary tables, before signing the overall Workplan.

Of course this is an example but the methodology to be used is the same.

3.6- MONITORING

It is a duty of the technical, or project, manager to implement a series of initiatives to control and measure the ongoing project. This is achieved through scheduled and unscheduled meetings, whose aims are the "objective" measurements of the following parameters:

I. Execution times,
II. Resources (quality and quantity of manpower and instrumentation) used,
III. Costs incurred,
IV. Quality of the elementary results/products achieved,
V. Expenditures flow.

Any one of those checks might be unsatisfactory, therefore countermeasures should be put in place to retarget to the initial objectives. As usual, it is always better to foresee and be prepared than to be caught off-guard, therefore assessment/management of risks has to be performed in advance.

Clearly, from the to-be-controlled issues described above, a meeting should be held whenever a result, small or important, is expected to be achieved. Because a result is usually associated to a milestone, those meetings are called milestones meetings. But again, in order to see in advance, also review meetings, to be called before the end of any task, should be foreseen. Of course these are most useful where the task is important in terms of duration. In general we can say that one review meeting per month is considered a Good Practice, and, of course, such meetings will assess all the tasks and Workpackages of the whole project.

4- ASICS in FUSE at a glance

ANALOGUE

AE NUMBER	APPLICATIONS	FOUNDRY	ENTRY TYPE	TYPE	TECHNOLOGY	SECTOR
233	OFFICE MACHINERY	ASIC		ARRAY	BIPOLAR	EDP
249	TELECOM	MAXIM		ARRAY		TELECOM
1009	TELECOM	TIMET		ARRAY	BIPOLAR	TELECOM
1953	TELECOM	ALENIA		FCIC	GaAs	TELECOM
2192	BIOMEDICAL	?		ARRAY		INDUSTRIAL
22907	ELECTRONIC HOUSE PRODUCTS	SLA		ARRAY	BIPOLAR	CONSUMER
23020	AUDIOVISUAL CONSUMER	AMS		CBIC	CMOS	CONSUMER
23208	BIOMEDICAL	AMS		FCIC	CMOS	INDUSTRIAL
23567	ELECTRICAL ENGINEERING	ZETEX		ARRAY	BIPOLAR	INDUSTRIAL
23596	TELECOM	SLA		ARRAY	BIPOLAR	TELECOM
24653	ELECTRONIC ENGINEERING	GMMT(?)			GaAs	INDUSTRIAL
25815	AUDIOVISUAL CONSUMER	ZETEX		ARRAY	BIPOLAR	CONSUMER
25832	AUTOMATION	HMT(?)		?		INDUSTRIAL
25842	ELECTRICAL ENGINEERING	ZETEX		ARRAY	BIPOLAR	INDUSTRIAL
25906	TELECOM	AMS	MPW	FCIC	CMOS	TELECOM
26535	ELECTRICAL ENGINEERING	ST		FCIC	CMOS	INDUSTRIAL

DIGITAL

AE NUMBER	APPLICATIONS	FOUNDRY	ENTRY TYPE	TYPE .	Technology ALL CMOS	S
166	BIOMEDICAL	CHIPEXPRESS		G.A.	CMOSLOW VOLTAGE	I
186	ELECTRICAL ENGINEERING	ATMEL	MPW	CBIC	CMOSLOW VOLTAGE	I
189	AUDIOVISUAL CONSUMER	XILINX		FPGA	CMOS	C
197	ELECTRICAL & OPTICAL	SAMES		FCIC	CMOS	I
201	ELECTRICAL ENGINEERING	ALTERA		FPGA	CMOS	I
202	INDUSTRIAL PROCESS CONTR.	THESYS		FPGA+G.A.	CMOS	I
205	ELECTRICAL ENGINEERING	?		CBIC	CMOS	I
211	TELECOM	TEMIC		?	CMOS	T
235	TELECOM	?		FPGA+CBIC	CMOS	T
239	ELECTRICAL & OPTICAL	ALTERA	MPW	CPLD	CMOS	I
240	ELECTRICAL ENGINEERING	CHIPEXPRESS		G.A.	CMOS	I
358	TELECOM	?		FPGA+?	CMOS	T
516	ELECTRICAL ENGINEERING	AMS		CBIC	CMOS	I
1005	OFFICE MACHINERY	TEMIC		CBIC	CMOS	EDP
1009	TELECOM	ZMD		?	CMOS	T
1213	BIOMEDICAL	AMS	MPW	CBIC	CMOSLOW VOLTAGE	I
1221	OFFICE MACHINERY	EKA		CBIC	CMOS	EDP
1224	TELECOM	?	MPW	CBIC	CMOS	T
1226	TELECOM	AMS	MPW	CBIC	CMOS	T
2010	TELECOM	ACTEL+AMD	MPW	FPGA+CBIC	CMOS	T
2045	ELECTRICAL & OPTICAL	TEXAS		G.A.	CMOSLOW VOLTAGE	I
2071	INDUSTRIAL PROCESS CONTR.	THESYS		G.A.	CMOSLOW VOLTAGE	I
2075	AUDIOVISUAL CONSUMER	?		CBIC	CMOS	C
2119	ELECTRICAL ENGINEERING	XFAB		CBIC	CMOSLOW VOLTAGE	I
2127	OFFICE MACHINERY	PLESSEY		CBIC	CMOSLOW VOLTAGE	EDP
2179	BIOMEDICAL	ATMEL		CBIC	CMOS	I
2218	ELECTRICAL ENGINEERING	ATMEL	MPW	CBIC	CMOSLOW VOLTAGE	I
2219	INDUSTRIAL PROCESS CONTR.	NEC		G.A.	CMOS	I
2227	INDUSTRIAL PROCESS CONTR.	ALTERA		FPGA	CMOS	I

2250	ELECTRONIC COMPONENTS	MSC?		FPGA+CBIC	CMOS	I
22842	RUBBER AND PLASTIC	?		FPGA+CBIC	CMOSLOW VOLTAGE	I
22895	ELECTRICAL & OPTICAL	JAMI+ALTERA		FPGA+G.A.	CMOS	I
22898	OFFICE MACHINERY	THESYS		CBIC	CMOS	EDP
22930	TELECOM	ORBIT+XILINX		FPGA+CBIC	CMOS	T
23279	OFFICE MACHINERY	?		FPGA	CMOS	EDP
23295	INDUSTRIAL PROCESS CONTR.	?	MPW	FPGA+G.A.	CMOS	I
23587	OFFICE MACHINERY	AMS		CBIC	CMOS	EDP
23627	TELECOM	ATMEL		CBIC	CMOS	T
23637	METAL PRODUCTS	QGATE	MPW	G.A.	CMOS	I
23717	ELECTRICAL & OPTICAL	AMS	MPW	FPGA+CBIC	CMOS	I
23764	ELECTRICAL ENGINEERING	XILINX		FPGA	CMOS	I
24594	TELECOM	?	MPW	CBIC	CMOS	T
24675	ELECTRICAL ENGINEERING	ATMEL		CBIC	CMOS	I
26552	ELECTRICAL & OPTICAL	?	MPW	FPGA+?	CMOS	I
26858	AUDIOVISUAL CONSUMER	ACTEL+?		FPGA+ G.A.	CMOS	C
27759	ELECTRONIC COMPONENTS	?	MPW	CBIC	CMOS	I
27870	INDUSTRIAL PROCESS CONTR.	IMS		G.A.	CMOS	I
29402	SEA TRANSPORTATION	SAMSUNG	MPW	CBIC	CMOS	TRA
29415	TELECOM	?		CBIC	CMOS	T

MIXED

AE NUMBER	APPLICATIONS	FOUNDRY	ENTRY TYPE	TYPE	TECHNOLOGY	S
111	PROCESS CONTROL	?			CMOS	I
124	METAL PRODUCTS	MIETEC	MPW		CMOSLOW VOLTAGE	I
145	ELECTRICAL AND OPTICAL	SEMEFAB			CMOS	I
155	TELECOM	?	MPW		BiCMOS	T
198	ELECTRICAL ENGINEERING	?		CBIC	CMOS	I
238	ELECTRONIC SUBSYSTEMS	ATMEL	MPW	CBIC-	CMOS	I
368	ELECTRICAL AND OPTICAL	µE	MPW		CMOS	I
371	ELECTRICAL AND OPTICAL	MCE		CBIC-	CMOS	I
504	AGRICULTURE	?		ARRAY		I
1003	PROCESS CONTROL	THESYS		?		I
1007	PROCESS CONTROL	MIETEC	MPW		CMOS	I
1008	OFFICE MACHINERY	AMS	MPW	CBIC-	CMOSLOW VOLTAGE	EDP
1016	MEDICAL	?			CMOSLOW VOLTAGE	I
1024	ELECTRONIC SUBSYSTEMS	AMS			CMOS	I
1029	MEDICAL	?			BiCMOS	I
1812	ELECRTONIC SUBSYSTEMS	THESYS			CMOS	I
2020	MEDICAL	MCE		CBIC-	CMOS	I
2032	ELECTRICAL AND OPTICAL	ATMEL		CBIC	CMOS	I
2050	ELECTRICAL AND OPTICAL	?			CMOS	I
2052	ELECTRICAL AND OPTICAL	?	MPW		CMOS	I
2078	ELECTRONIC SUBSYSTEMS	?			CMOS	I
2091	PROCESS CONTROL	MELEXIS	MPW		CMOS	I
2107	ELECTRICAL AND OPTICAL	ALFA			BIPOLAR	I
2123	ELECTRICAL AND OPTICAL	AMS	MPW		CMOS	I
2148	MEDICAL	AMS	MPW		CMOS	I
2204	TELECOM	ATMEL	MPW	CBIC-	CMOSLOW VOLTAGE	T
2224	ENERGY PROD.& DISTR.	AMS	MPW		CMOS	I
2228	ELECTRICAL AND OPTICAL	?			CMOS	I
2251	ELECTRONIC SUBSYSTEMS	?		CBIC-	CMOS	I
22873	ELECTRICAL AND OPTICAL	AMS	MPW	CBIC-	CMOS	I
22918	ELECTRICAL ENGINEERING	THESYS		CBIC	CMOS	I
22949	MEDICAL	AMS	MPW		CMOSLOW VOLTAGE	I
22990	ELECTRONIC SUBSYSTEMS	AMS	MPW		CMOS	I
23068	MEDICAL	AMS			CMOSLOW VOLTAGE	I
23086	ELECTRICAL AND OPTICAL	?	MPW		CMOS	I
23130	PROCESS CONTROL	THESYS		CBIC-	CMOS	I

23169	ELECTRICAL AND OPTICAL	ATMEL		CBIC-	CMOS	I
23275	ELECTRICAL AND OPTICAL	AMS	MPW		CMOS	I
23298	ELECTRICAL AND OPTICAL	AMS			CMOS	I
23328	ELECTRONIC SUBSYSTEMS	AMS	MPW	CBIC-	CMOS	I
23333	TELECOM	AMS	MPW		BiCMOS	T
23380	ELECTRICAL AND OPTICAL	IMS		ARRAY	CMOS	I
23445	ELECTRONIC ENGINEERING	?			CMOS	I
23454	PROCESS CONTROL	AMS	MPW	CBIC-	CMOS	I
23588	ELECTRICAL AND OPTICAL	?	MPW		CMOS	I
23597	ELECTRICAL AND OPTICAL	AMS	MPW	FCIC-	CMOS	I
23628	ELECTRICAL ENGINEERING	AMS		CBIC	CMOS	I
23630	ELECTRICAL AND OPTICAL	THESYS			CMOS	I
23636	PROCESS CONTROL	MIETEC	MPW		CMOS	I
24348	TELECOM	AT&T		CBIC-	CMOS	T
24558	SOFTWARE CONSULTANCY	ATMEL			CMOS	EDP
24571	MEDICAL	?			BiCMOS	I
24606	TELECOM	AMS	MPW		CMOS	T
24613	TELECOM	AMS	MPW	CBIC-	CMOS	T
24651	PROCESS CONTROL	AMS		CBIC-	CMOS	I
24656	ELECTRICAL AND OPTICAL	AMS	MPW	CBIC-	CMOS	I
24677	ELECTRONIC SUBSYSTEMS	AMS	MPW	CBIC-	CMOSLOW VOLTAGE	I
24732	ELECTRICAL AND OPTICAL	ATMEL	MPW	CBIC-	CMOS	I
24734	MEDICAL	AMS		CBIC-	CMOS	I
24744	PROCESS CONTROL	IMS		FCIC-	CMOS	I
24755	METAL PRODUCTS	ST		FCIC	MOSFET	I
24809	PROCESS CONTROL	AMS	MPW		CMOS	I
25747	ELECTRICAL AND OPTICAL	AMS			CMOS	I
25828	ELECTRONIC SUBSYSTEMS	?		CBIC-	CMOS	I
25829	ELECTRONIC ENGINEERING	AMS			CMOS	I
25866	PROCESS CONTROL	AMS	MPW		CMOS	I
25870	PROCESS CONTROL	?			CMOS	I
25956	TELECOM	MAXIM		ARRAY	BIPOLAR	I
25969	ELECTRICAL ENGINEERING	AMS	MPW	CBIC	CMOS	I
25970	MEDICAL	MIETEC	MPW	CBIC-	CMOS	I
26033	MEDICAL	AMS		CBIC-	CMOS	I
26130	ELECTRICAL AND OPTICAL	THESYS			BiCMOS	I
26704	ELECTRONIC SUBSYSTEMS	AMS		CBIC-	CMOS	I
27061	TELECOM	AMS	MPW		CMOS	T
27771	ELECTRICAL AND OPTICAL	AMS	MPW		CMOS	I
29373	PULP AND PAPER	AMS	MPW	CBIC-	CMOSLOW VOLTAGE	I