AE 27410

WIRELESS BIKE REAR DERAILLEUR SYSTEM

*Mixed signal ASIC technology results in innovative new product.*
Established in 1890, MAVIC designs, manufactures and markets high quality equipment and accessories for high value mountain and road racing bikes including rims, wheels, hub with cartridge bearings and the electronic derailleur. Products are distributed to end users via a network of sales distributors world-wide. The company employs 300 people, and has sales turnover of 35 M Euros.

The majority of MAVIC’s product range was based on the design, development and production of bicycle mechanical components. In 1993, MAVIC introduced the “ZAP MAVIC SYSTEM” (ZMS), an electronically controlled derailleur, which enabled push button instigation of up or down gear shifting on bicycles. This micro-controller based product was developed by subcontractors, and this was MAVIC’s first electronic experience.

The ZMS product was a market success, but was withdrawn from the market by the company in 1995 because of reliability problems associated with the wired solution. The strong market response indicated that a product which provided a method of communications which overcame the reliability problems associated with the wiring would be a major economic success.

This market opportunity led MAVIC to develop a mixed signal ASIC device to implement a bi-directional, wire-less, digital communication link between the rear derailleur and a controller on the handle bar to overcome these reliability problems. These two units are set approximately 1.2 m apart on the bicycle, and form part of an overall system including brake levers with an embedded gear switch and a front wheel wireless speed sensor. The system uses 3 printed circuit boards (PCBs) Each PCB contains two IC components:

1. A specific micro-controller with the signal processing software of the wireless transmission and the specific control functions for the device it controls.
2. The mixed signal ASIC which is controlled by the micro-controller.

Each circuit is in standby mode most of the time to minimise consumption, switches periodically to detection mode to check whether incoming messages are being sent and, if so, switches to full receiving mode.

The improved system provides the cyclist with several benefits including:
- Quick gear shift operation.
- Short assembly time, based on ease of mounting of the system components.
- Speed indication on system display.
- Compatibility with all cycle frame sizes.
- User feedback via visual presentation of gear position on the control and display module’s LCD display.

The mixed signal ASIC development was completed within 12 months. The ASIC development costs were 138 k Euros.

Based on the total system development costs which included a significant industrialisation cost, payback period is estimated to be less than 10 months and ROI in 2001 will be 350%.

Based on mixed signal ASIC development costs alone, these figures become respectively less than 1 month and 3500%.

**Keywords**

- Mixed signal ASIC
- Wireless communication
- Bicycle accessories
- Bicycle components
- RF control
- Gear changing device for racing bicycles

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1. Company name and address

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01990 SAINT TRIVIER
FRANCE
Tel: 04 74 55 80 55
Fax: 04 74 55 80 58

2. Company size

- 1997 turnover : 35 M Euros.
- Number of employees: 300.
- Number of engineers involved in electronic systems : 2

MAVIC is owned (100%) by the French winter sports group SALOMON, being part of the newly formed group ADIDAS-SALOMON, the second sports articles group in the world.

3. Company business description

Established in 1890, MAVIC designs, manufactures and markets high quality equipments and accessories for high value mountain and road racing bikes including rims, wheels, hub with cartridge bearings and Electronic derailleur.

The company good reputation is also based on the support it provides to major racing teams in France, including Tour de France teams. MAVIC equips 26 professional teams around the world and, in 1989, Greg LEMOND who was "Tout MAVIC" equipped, won the Tour de France and the World Championship.

Industrial Sectors: Prodcom Code 34-35 (Transport equipment)

4. Company markets and competitive position at the start of the AE

The MAVIC customers are end users who spend a great deal of their leisure time bicycling. They are ready to invest into high quality / high performance components that fulfil both their need and pride.

Products are distributed to end users via a network of bicycles distributors world-wide.

The market is price segmented. Because of the product’s high performances, quality and design, they are found on road bikes at retail prices above 800 Euros and mountain bikes at retail prices above 500 Euros. The target for the improved product is road racing bikes of retail prices above 1500 Euros

The world-wide bike market is estimated at 30 millions bicycles / year, of which 3.5 % are road racing bikes, i.e. 1.0 million bicycles / year. Within this sector the market opportunity is for sales to the:

- first equipment market: for the first year, the FU product will be used on bikes above 2000 Euros which represents 1/10 of road racing bikes. Thus this market is estimated at 100 000 bicycles / year.

- Refurbishing market: bearing in mind that such end-users are estimated to replace important components such as rear derailleur and its associated commands once every 5 years, it can be easily inferred that this market is estimated at 100 000 bicycles / year.

Furthermore, the bike market trend being slightly upward and innovations pushing up the high end of it, these figures should increase by 2 to 5 % per year.
The main MAVIC contenders on the derailleur market are Shimano and Campagnolo (Italy). Shimano designs its components in Japan and manufactures them in Asia. Its main high level mechanical derailleur systems are: Dura-Ace, Ultegra and 105. Shimano market share on road bike is about 50 %, and 80 to 90 % on mountain bike. Campagnolo (Italy), with overall sales about 10 % of Shimano’s, offers competing systems with its mechanical derailleur Record, Chorus and Athena versions. Campagnolo’s market share on road bike is about 50 %.

All the competitors systems are mechanically activated and work on the basis of a cable being pulled incrementally through levers implemented in brake levers. High end cable systems are sold (retail price) between 400 and 700 Euros.

<table>
<thead>
<tr>
<th>MAVIC Turn Over 97 (kEuros)</th>
<th>MAVIC Turn Over 98 (kEuros)</th>
<th>MAVIC Market share</th>
<th>Shimano Market share</th>
<th>Campagnolo Market share</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rims and Wheels</td>
<td>35000</td>
<td>51500</td>
<td>50 %</td>
<td>0 %</td>
</tr>
<tr>
<td>Meca derailleur</td>
<td>0</td>
<td>0</td>
<td>50 %</td>
<td>50 %</td>
</tr>
</tbody>
</table>

Table 1: Market shares

None of these two competitors design electronic nor wireless derailleur, which offer competitive advantages in terms of ergonomics, aesthetics, display facilities, and ease of installation.

This provided a major market opportunity to produce a highly innovative product.

In a first attempt, MAVIC developed and launched in 1994 the “ZAP MAVIC SYSTEM” (ZMS) which met instantaneous success and MAVIC obtained a 5% market share of the highest product range. In 1995, reliability problems led MAVIC to take ZMS out of the market and no sale was achieved during the two following years.

Regular inquiries from professional teams, users, retailers, and competition, about the future of the MAVIC electronic derailleur underlined the market strong demand for a ZMS successor.

5. Product to be improved and its industrial sectors

The ZMS consisted of an electronic control unit connected to the rear derailleur by a wire harness. The controllers (or Zap) fitted to the handles enabled the cyclist to generate up / down gear shift. The system is illustrated in Figure 1 below.

Fig 1: Schematic of the ZMS electronic derailleur
For gear shifting, the control switch closure induces the micro-controller to activate a solenoid that pushes a pin into a threaded drive rod that is connected to the guide pulley of the rear derailleur. The rotating pulley turns the drive rod, which mechanically moves the derailleur back and forth making up and down gear shift. When the desired gear is obtained, the micro-controller turns off the solenoid power and the drive pin is withdrawn.

The prized features of the device were:
- its unique user friendliness,
- its light weight,
- its shifting speed.

The functional specification were as follows:
- Number of switching units: 2
- Connection between controller and rear derailleur: 4 wires
- Maximum number of gears: 8
- Indication of gear position: None
- Switching unit feedback None
- Gear shift possible orders: 1 by 1 (All by prolonged contact on switch)
- Temperature Range: -10 + 60° C
- Water proof: Rain + high pressure cleaning device
- Shock / vibration: For road racing conditions
- UV / solvent: Resistant

The improvements required for the system include:
- Improved reliability, by:
  - Removing the wire harness which was fragile, difficult to install, cumbersome to maintain and had limited compatibility with various bike frame sizes.
  - Removing the electronic connectors which were prone to water ingress.
  - Improving the electronics design to stand the current peaks drawn by the solenoid.

The projected benefits to be delivered from the application experiment included:
- Wireless links.
- Ergonomic (thanks to the easy access and handling of switches).
- Lighter weight due to removal of cables and sheaths and replacement of mechanical shifter by integrated electronics.
- Easy to install (no cable, rear derailleur easier tuning).
- Easy to maintain (thanks to information provided by the electronics).
- Aesthetics (derailleur and electronic blocks are being designed as a whole, no cable running along the frame)
- Competitive retail price.
- Fashion effect development driven by innovation and design.

The detailed improvement are defined in the following section.
6. Description of the product improvements

6.1. The new MAVIC electronic derailleur system
This MAVIC wireless derailleur system, the MEKTRONIC, comprises of:
1. two-way wireless digital communication links:
   1.1. between Control Board on the handle bar and the 1.2 m distant rear derailleur,
   1.2. between the wireless front wheel speed sensor and the Computer Board.
2. 2 brake levers assemblies which carry gear shift buttons.

This system configuration is illustrated in the following illustration:

The improved system contains three modules: control board, rear derailleur and speed sensor contain each a Specific Electronic Circuit (SEC) carrying on PCB the necessary components for communication link: micro-controller, ASIC, transmission and receiving hardware (matching network antennas and filters).

The micro-controller is different in each SEC to meet cost optimisation requirements, the microcontroller performs the signal processing functions for the wireless transmission link and the necessary functions required for the control of the specific device it is connected to.

The mixed signal ASIC, the target of this application experiment, is the same for each SEC.

The improvements between the ZMS and the wireless derailleur are illustrated in the following parameters comparison table:
<table>
<thead>
<tr>
<th>Functionalities</th>
<th>ZMS</th>
<th>New wireless derailleur</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of switching units</td>
<td>2</td>
<td>up to 3</td>
</tr>
<tr>
<td>Connection between controller and rear derailleur</td>
<td>4 wires</td>
<td>wireless</td>
</tr>
<tr>
<td>Maximum number of gears</td>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td>Gear shift possible orders</td>
<td>1 by 1</td>
<td>1 by 1 by prolonged contact on switch</td>
</tr>
<tr>
<td>Indication of gear position</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Switching unit feedback</td>
<td>No</td>
<td>Snapping feeling and noise</td>
</tr>
<tr>
<td>Number of shifts</td>
<td>50000</td>
<td>200000</td>
</tr>
<tr>
<td>Battery</td>
<td>6V / 180 mAh</td>
<td>3V / 180 mAh</td>
</tr>
<tr>
<td>Battery expected life</td>
<td>6 months</td>
<td>24 months</td>
</tr>
<tr>
<td>Battery warning</td>
<td>None</td>
<td>Yes</td>
</tr>
<tr>
<td>System display unit</td>
<td>None</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Environment**

<table>
<thead>
<tr>
<th>Electromagnetic compatibility</th>
<th>No</th>
<th>Yes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature domain</td>
<td>- 10 + 60° C</td>
<td>- 10 + 60° C</td>
</tr>
<tr>
<td>Water exposure</td>
<td>rain + high pressure cleaning device</td>
<td>rain + high pressure cleaning device</td>
</tr>
<tr>
<td>Shock / vibration</td>
<td>Road racing conditions</td>
<td>Road racing conditions</td>
</tr>
<tr>
<td>UV / solvent</td>
<td>Resistant</td>
<td>Resistant</td>
</tr>
<tr>
<td>Prevention of water ingress</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Fitting on bicycle frame**

<table>
<thead>
<tr>
<th>Assembly time</th>
<th>30’</th>
<th>5’</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compatibility with the majority of bike frames / bar systems</td>
<td>weak</td>
<td>complete</td>
</tr>
</tbody>
</table>

**Consumer**

**Advantage**

- user friendly
- weight
- swift gear shifting

**Drawbacks**

- lack of compatibility with frame types and sizes
- mounting (wire harness)
- water proof (wire harness, Electronic connector)
- battery short life time
- price

- user friendly (improvement of controller feeling and LCD display)
- weight
- swift gear shifting
- easy mounting and maintenance
- compatible with all frame types and sizes
- competitive price
- none perceivable
In addition the introduction of the new system design based on the mixed signal ASIC introduces the following additional improvements:

- Electronics has been redesigned to withstand current peaks.
- New solenoids have been developed to draw 4 times less energy.
- Overall cost of the improved product compared to the original system is cut by 30% to 50% (depending on product range) due to wiring harness and connectors deletion and installation cost reduction.
- Retail price compatible with the market defined target (bike retail price of 1500 Euros or more).
- Furthermore, the total weight of the Electronic derailleur is less than that of the corresponding systems from the competitors’ top range like DURA-ACE and ULTEGRA.

6.1. Functional specifications of the total system

General characteristics:
- Portable devices, battery operated. Current consumption optimised to guarantee batteries life greater than 2 years.
- Minimum size to be integrated on components designed for road racing bicycles hence light, small and aesthetic.
- Bi-directional wireless links.
- Robustness to electromagnetic perturbations i.e. high rejection of interference (both internal and external) to make the link as reliable as possible.

Current consumption optimisation strategy
- Each SEC will be in standby mode most of the time to minimise consumption.
- It will switch periodically to detection mode to check whether incoming messages are being sent.
- If so, then it will switch to full receiving mode.

The SEC will have 2 transmitter operation modes to deal with «normal environment» and «racing environment» respectively. In the racing environment where current consumption can be higher because the batteries can be changed more often, the use of higher current levels improves the electromagnetic compatibility level in an environment where a lot of radio transmissions may exist.

IC components co-operation
The short link between ASIC and micro-controller will enable data exchange (in/out) and component configuration (central frequency, emitted power, emission-reception mode, standby or detector mode).
All messages being digital, a serial link with a shift register will enable data transfer with corresponding micro-controller. A high order input filter in the receiver protects the transmission from electromagnetic pollution.
- Messages will be sent and received at various frequencies.
- Power emission level will be selected by software.

Operating cycles
A micro-controller will set “its” ASIC in 4 modes: Standby, Detector, Receiver, Transmitter.
- Messages should be as short as possible to prevent message collisions but the data rate will be limited by the micro-controller speed and by the maximum acceptable bandwidth (the higher the bandwidth, the weaker the electromagnetic robustness).
- The clock is fed to the ASIC so that it can be turned off by the micro-controller when it is not required: this will strongly reduce the ASIC internal consumption in standby mode.
• The message detection will be carried out in two phases:
  − After the derailleur ASIC wake up, this latter will repeat (standby / detector mode) cycles where the detector mode timing is dictated by the minimum number of instructions required by the micro-controller to detect the presence of a message while taking into account current consumption & threshold accuracy requirements.
  − If a message is detected, the ASIC switches to the receiving mode where the signal will be amplified, filtered and demodulated. The required time to switch from detector to receiver mode is linked to the phased lock loop (PLL) stabilisation time which will be confirmed.


6.2.1. Functional block diagram of the ASIC

![Functional Block Diagram of the ASIC](image)

6.2.2. Technical specifications

• Data rate: > 1000 bits/s.
• Band width: < 15 kHz
• Central frequency: < 150 kHz
• Power emission: minimum 5 different levels (up to 100 mA in the antenna)
• Bit error rate: better than $10^{-4}$
• Maximum acceptable consumption (to be optimised for 4 modes)
  − Stand-by: <1.5 µA
  − Detector mode: <400 µA
  − Receiving mode: <800 µA in the (-10, + 60°C) range
  − Transmitter mode up to 50 mA in the (-10, + 60°C) range
7. Choices and rationale for the selected technologies, tools and methodologies

7.1. Choice of wireless communication concept:
Infrared and optical technologies were discarded due to the screen effect of the cyclist’s legs. Ultrasonic means were rejected due to insufficient bit rate.

The frequency selection: the range was chosen below 150 kHz and the central frequency was to be selected by software.

In this spectrum, the number of powerful emitting stations is very small and they are well known (International list of frequencies purchased from the International Union of Telecommunications). Furthermore, in this frequency range, most systems work on the induction principle which is regulated by the ST 300.330. Maximum magnetic field level is limited to 72 dB \( \mu \text{A/m} \) at 10 m which strongly lower the risk of interference with the system.

The frequency is set by the micro-controller. It must be fixed for the commercial version of wireless derailleur and adjustable from one system to another by mean of a Phase Locked Loop (PLL).

Bit Error Rate (BER) which is fundamental for the reliability of the system, is mainly imposed by the signal / noise ratio at the receiver input which, itself, depends on receiver filtering, demodulator noise rejection and demodulator jitters.

Data rate and receiver bandwidth (BW) selection is a trade off between message duration and electromagnetic noise rejection which is influenced by the filter type and bandwidth. The following compromise was settled at: - Data rate >1000 bit/s - BW = ± 7.5 kHz

7.2. Choice of mixed signal ASIC

The product is based on RF mixed mode ASIC technology. The SACMOS (TSMC / Philips technology), 2 microns device technology was selected and implemented. This provided a good compromise between product technical constraints (consumption, low voltage, existing library), cost of development and masks, cost per produced unit, and reliability (well proven technology, many users world wide). Furthermore, due to its large base of customers, the foundry and XEMICS/CSEM are committed to provide this technology for 10 more years.

The initial packaging was SMD (SO 24). This will be replaced by COB when sufficient volume is reached. Circuit layout has been finalised. Overall circuit surface is close to 14 mm².

Alternative microelectronic technologies were considered but rejected for this application experiment:

Purely digital implementations, such as FPGA or CPLD, technologies were incapable of performing the analogue transmission mode for the selected RF transmission link. In addition, these devices were considered too costly.

Micro-controller technology, although utilised to perform the programmable control functions for the improved system, could obviously not incorporate the digital transmission requirements for the system, and therefore an additional ASIC component was required.

Discrete device solutions were rejected on the basis of the severe size limitations imposed in this application. Discrete components, even when used as SMT components, occupied to much space to provide an economic and practical solution.
7.3. Choice of Complete System

It comprises 3 PCB boards (wireless controller speed sensor and rear derailleur) each carrying the necessary components for communication link: ASIC, micro-controller (different on each board for cost optimisation); transmission and receiving hardware (matching network antennas and filters.)

Mixed technology package for each board: CMS for ASIC, micro-controller, resistors and coupling capacitors.

Standard technologies for quartz, antenna, power supply capacitors for solenoids current peaks, reed switch for speed sensor, battery contacts.

7.4. Methods and tools

Simulation was used to demonstrate ASIC functionality by mean of methods which have been agreed between MAVIC and the development subcontractors (XEMICS/CSEM, and CREATIVE EURECOM).

ASIC production testing: 100 % of the first production run had their main functionalities (consumption, bandwidth and noise rejection, threshold level,...) electronically tested. In serial production, XEMICS / CSEM quality department will control 5 % products per batch.

Required qualification and environmental tests (MIL-STD 883). They have been performed (temperature cycles, damp heat, thermal shock, vibrations, solvents resistance, solder ability,...). The ASIC was developed by mean of standard CAD tools (VHDL, Synopsys and Quicksim) and produced by PHILIPS using its well proven tooling and tests facilities. Standard electronics tools and tests equipment were used elsewhere.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

MAVIC main activity was development and production of bicycle mechanical components. Subcontracting ZMS derailleur electronics was the first electronic experience of MAVIC which had no competency in ASIC and standard electronic design and development as well. To acquire these competencies for the FU product development, MAVIC hired two engineers:

Michel KUBACSI as project director of the AE project.
- 5 years as an R&D engineer on electronic measurement systems in oil logging.
- 6 years as an R&D manager on electronic control systems in the appliance industry.
- 3 years as an R&D director on electronic measurement systems on fluids in the industry.

The success of the FUSE project has been instrumental in Mr KUBACSI being promoted to General Managing Director of MAVIC.

Bruno MONTAGNON as Electronic Chief Designer in the AE project.
- 2 years as a maintenance engineer in the aeronautic industry
- 10 years as an electronic engineer in the appliance industry
9. Work plan and rationale

The work plan for the application experiment is shown in the following table. This workplan was closely adhered to during the application experiment because of an immovable end date set by the need to display the prototype at a trade fair. Close technical and project management of the ASIC development process ensured all project milestones were accomplished on time.

<table>
<thead>
<tr>
<th>WP1 technical management</th>
<th>Month</th>
<th>1</th>
<th>2</th>
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<tbody>
<tr>
<td>11 - Experiment planning</td>
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<td>12 - Article for FUSE news letter</td>
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<td>15 - Design Planning assistance (Subcontr. 1)</td>
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</table>

**WP2 Training**

| 21 - Initial training on technical management ASIC design and testing rules |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 22 - ASIC development through project follow-up |   |   |   |   |   |   |   |   |   |   |   |   |   |

**WP3 Specifications**

| 31 - Functional requirements  |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 32 - Environmental requirements | |   |   |   |   |   |   |   |   |   |   |   |   |
| 33 - Agreement on ASIC specs  | |   |   |   |   |   |   |   |   |   |   |   |   |
| 34 - Preliminary ASIC specs (Subcontr. 1) | | | | | | | | | | | | |
| 35 - System simulations (Subcontr. 1) | | | | | | | | | | | | |
| 36 - Final ASIC specs (Subcontr. 1) | | | | | | | | | | | | |
| 37 - Agreement on final ASIC specs (Subcontr. 2) | | | | | | | | | | | | |

**WP4 Design**

| 41 - External circuit design |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 42 - ASIC Final circuit design (Subcontr. 1) | | | | | | | | | | | | |
| 43 - ASIC circuit layout (Subcontr. 1) | | | | | | | | | | | | |

**WP5 Evaluation**

| 51 - Lab testing of circuit behaviour - report | | | | | | | | | | | | |
| 52 - Field testing of circuit behaviour - report | | | | | | | | | | | | |
| 53 - ASIC prototypes production (Subcontr. 1) | | | | | | | | | | | | |
| 54 – ASIC qualification - report (Subcontr. 1) | | | | | | | | | | | | |
| 55 – ASIC tests sequences (Subcontr. 1) | | | | | | | | | | | | |
| 55 - Evaluation of ASIC performances – report (Subcontr. 2) | | | | | | | | | | | | |

**WP 1 - TECHNICAL MANAGEMENT**

The objective of this task was to manage:

- the ASIC development in time and cost and ensure its unit costs control, as a dedicated component of the wireless derailleur system,

It was mandatory for MAVIC to show the end product at the September 98 bike show. Otherwise a business loss of nearly 3.5 millions Euros had to be foreseen. Furthermore, a risk analysis of the project showed that the technology was feasible (confirmed after the agreement on specs) but that the timing was very uncertain. Hence, the stress was put on obtaining ASIC pilot run (so called “rush lots”) delivery as soon as possible.
the co-operation between MAVIC and its two subcontractors,
the follow up co-operation with the TTN.

Technical management detailed actions included the set-up of a detailed planning including full design phase, layout and prototype manufacturing. Ensure program technical management.

**WP 2 - TRAINING**

- **Informal training:**
  Specifications discussion and writing gave to MAVIC a realistic picture of SACMOS technology in terms of performances (consumption, accuracy, tolerances). The company acquired practical knowledge about:
  - Costs comparison of a packaged and dye version.
  - Costs / quantities
  - Analysis of functions costs to establish the specifications.
  - Test organisation and equipment to minimise the time required for functional control.
  - Test optimisation by full functional characterisation correlated with simple and fast measurements made on the circuit.

- **Formal training**
  It was provided by subcontractor 1: XEMICS in NEUCHATEL Switzerland.
  - Basic principles and tools of integrated circuits, trends and choices.
    - Presentation of low-power CMOS integrated circuits.
    - passive devices implementation,
    - elementary building blocks and voltage references.
    - Technological trends and their consequences in terms of fab and process constraints.
    - Digital / analogue circuits development project organisation and structure.
    - Scope, costs and mastering of CAD tools: VHDL, Autologic or Synopsys, Quicksim or Flextest, Place & Route, Lpex for the digital and VHDL, ELDO, ICgraph, Electronical Route Check, Lpex for the analogue.
  - Foundry (IC producer) – relationship and quality control
    Various constraints linked to IC production start / quality control / production flow.
    - Circuits are characterised through specific tests during the initial evaluation (engineering batch).
    - Experience makes statistical control of process (SACMOS 2.0) and packaging (SOP 20) sufficient.
    - Circuits functionality are tested at 100 %.
    - Engineering batch takes less than 6 weeks in a rush procedure.
    - Engineering batch is limited to 6 or 12 wafers.

- **Conclusion**
  A good background in electronic technology and industry was mandatory.
  MAVIC acquired sufficient knowledge of specific constraints at various stages of an ASIC development: basic technology, development tools, design checks, ASIC costs parameters and foundry delays and process control.
  MAVIC learned the fundamentals of strategic choices in ASIC domain: type of technology, future of technology, backup solutions, multiple supply.
  Furthermore, Training by subcontractor enabled more open and effective relationship.
**WP 3 - SPECIFICATIONS**

The ASIC specifications were to be optimised according to functional requirements and environmental constraints. This phase has been completed according to plan (one month after project started) and specifications have been agreed upon.

- **First user**
  Had the responsibility to establish the detailed functional and environmental requirements of the ASIC in terms of:
  - Electromagnetic interference.
  - Magnetic field measurements and induced voltages.
  - Power consumption.
  - Micro-controller / ASIC interface.
  - Hardware environment (supply voltage, crystal, etc.).

Furthermore, the FU controlled with subcontractor 1 & 2 that the electronic and functional specifications of the ASIC offered the best economical / functional / quality trade-offs for the application.

- **Subcontractor 1**
  Proposed electronic specifications of the ASIC based on the technologies it mastered and could provide:
  - Bit error rate tests.
  - Circuit schematics.
  - Receiver (filter + demodulator) response.
  - Response time (Phased Locked Loop and Pick Detector Level).
  - Preliminary specifications as (circuit + internal specifications).
  - Current consumption with respect to possible schematics.

- **Subcontractor 2**
  Checked that the ASIC specifications could be met with the type of RF architectures compatible with the application.
  - Architecture comparisons.
  - Bandwidth / data rate.
  - Viable transmitter architectures.

**WP 4 – DESIGN**

The main objective of this work package was detail design of electronic circuit and checking it by simulation.

Analogue blocks layout was carried out and then connected to the digital part of the circuit and to the I/O pads. All drawing rules and electronic functionality were checked. The design and layout work were interlocked to minimise development time.

To shorten this stage as much as possible, XEMICS called up important resources. MAVIC, on its side, spent more time than expected updating the mock-ups, to obtain a close representation of the ASIC.

WP4 finished 2 weeks before schedule and costs were as budgeted.

- **First user role:**
  - Detail design of external circuits.
  - Interfacing these circuits with the ASIC (quartz or clock, micro-controller, emitting/receiving antenna, de-coupling capacitors, printed circuit layout,...)
  - Full circuit functional checking through the evaluation of a mock-up circuit of the ASIC.
- Determination of voltage thresholds and filtering requirements.
- Study of various antennas characteristics.
- Micro-controller Interfacing: data exchanges / configuration.
- Study of timing requirements.

**Subcontractor 1**
Performed the layout and detailed ASIC design; applied simulation / drawing rules and functionality reviews to control that specifications were met at 100%.
- Transmitter power transistor.
- S/N levels at the demodulator input for various BER
- Amplifiers specifications (noise rejection / gain / distortion)
- Consumption.
- Tolerances on threshold levels.
- Common mode rejection.
- Harmonics rejection.
- Determination of acceptable set-up times.
- Final ASIC specifications.

**Subcontractor 2**
Reviewed the various circuit implementations and simulations to check that the RF functionality are met.
- Antenna driving circuit and simulations.
- Antenna matching receiver architecture.
- Specifications on output power transmitter.
- Check on overall receiver architecture (gain / noise factor / IP3...)
- Preliminary estimates on jitters

**WP 5 - EVALUATION**
Main objective: laboratory and field evaluations of the ASIC prototype samples to check the end-product specifications meeting.

**First user role:**
Functional and evaluation tests of the ASIC in the end-product environment.
- Electromagnetic compatibility tests.
- Tests on bike in various environmental conditions (electromagnetic, temperature, vibrations).
- Tests with professional riders
- Endurance and environmental lab tests (humidity, salt mist, T° cycling, ...).
- Specifications for circuit testing.

For the ASIC evaluation, two types of printed boards were developed: one following the RF rules of implementation (which requires grounded planes / symmetrical printed lines) and one close to the envisaged final implementation which takes into account the surface constraints. This enabled ASIC behaviour checking depending on printed board characteristics. MAVIC implemented the circuits on both types of printed boards to compare the circuit behaviour. No significant difference were seen at this stage.

A lot of work was done on the network matching ASIC to the antenna characteristics.
The ASIC were bonded on the derailleur and computer printed circuits for evaluation purpose.
Lab evaluation:
- Initial results were poor due to problems linked to:
  - Insufficient ASIC / antenna impedance matching.
  - Noise on the PDL (detector) input; found to be induced by the clock oscillator implementation and waveform which had to be smoothed out.
  - Communication patterns which were too short to be correctly received by the derailleur.
These problems were solved through experimentally by software adjustments.
- Communication between computer / derailleur was found to work correctly up to a 2 m distance. The interference tests combined with field mapping confirmed the sensitivity of the receiver part of the ASIC.
- The radiated energy coupling with the derailleur subsystem met the requirements but was improved by slanting the derailleur antenna.
- Rejection tests have been carried out between 10 kHz and 250 kHz. Excellent rejection (up to 80/100 dB) was demonstrated for emissions out of the bandwidth, apart from the $H^{(3)}$ and $H^{(5)}$ harmonics. Close to these frequencies, rejection satisfied specifications.

Field evaluation started in parallel as follows:
- 7 bikes were fitted with the circuits and ridden regularly. No significant transmission problem were found, even in hostile environment (TGV, power lines...).
- 4 systems ran on an automatic bench which induced gear shift every 6 seconds. 250000 shifts were reached without incident.
- 9 bikes were equipped with the FU system to be exposed at the September bicycle fair. They performed up to 10000 shifts a day without major problem.
- Energy consumption tests were carried out on the life-time testing bench. The expected number of shifts (80000 for a 3V cr2032 button battery) were found conform to calculation.
- Bikes equipped with prototype FU systems were given to 3 professional riders of the CREDIT AGRICOLE team for test in actual racing conditions: initial feedback was good, main comments concerning ergonomic, number of shifters (3 in parallel), total weight and revolutionary character of this technology.
- Environment tests were successfully carried out (Temperature cycling / vibrations / shocks / humidity).
- Speed sensor circuit optimisation has now started to finish the evaluation of the complete system.

**Subcontractor 1**
Produced masks and a first ASIC run; provided prototype samples; qualified circuit (ASIC specifications) and developed the test sequences.
- Test of 10 ceramic and 10 plastic circuits which were sent to MAVIC for evaluation.
- Limited characterisation of one of the circuit which showed that all specifications were met but third harmonic rejection (where measurement have shown a 2dB rejection for a spec at 3dB).
- Initial tests which showed that they met the specifications at 2.6 V and at room temperature.
- Successful initial testing of main functionalities of these circuits.

**Subcontractor 2:**
Provided independent evaluation of the ASIC performances.
The resources utilised in the completion of the mixed signal ASIC design are defined in the following table:

<table>
<thead>
<tr>
<th></th>
<th>Efforts in person x days</th>
<th>Costs (k Euros)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Planned</td>
<td>Achieved</td>
</tr>
<tr>
<td><strong>FU</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WP1: Technical Management</td>
<td>15</td>
<td>16</td>
</tr>
<tr>
<td>WP2: Training</td>
<td>14</td>
<td>15</td>
</tr>
<tr>
<td>WP3: Specification</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>WP4: Design</td>
<td>30</td>
<td>32</td>
</tr>
<tr>
<td>WP5: Evaluation</td>
<td>35</td>
<td>38</td>
</tr>
<tr>
<td>Other (travel &amp;subs)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Subtotal</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Subcontractor 1</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Training costs</td>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>Design assistance</td>
<td>110</td>
<td>133</td>
</tr>
<tr>
<td>Production costs by foundry</td>
<td>30</td>
<td>36</td>
</tr>
<tr>
<td>samples evaluation</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Subtotal</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Subcontractor 2</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design and evaluation assistance</td>
<td>25</td>
<td>12</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Planned and Actual Resource Requirements for the Application Experiment**

Whilst the application experiment completed on schedule, the total actual cost exceeded budget by 9.5% due to:

- Underestimation of functional complexity and of sensitivity to interference which increased time spent in mock-ups building and circuit implementation and adaptation.
- Decision to replace prototype phase as such by a first batch of ASIC manufactured with production masks. This risk was motivated by time to market constraint and associated need to deliver a large number of ASIC as quickly as possible.
- Underestimation of feasibility study phase.

The major risks identified at the outset of the application experiment were the achievement of the RF bit error performance requirements and the delivery of the ASIC define within the timescales. The system design and specification phase addressed the communications mechanisms using design modelling, theoretical performance analyses, and by the co-operation of the two subcontractors during the specification phase. The establishment of an agreed time plan for the application experiment coupled with strong project management activity ensured that the time scale risks were minimised. The time scales were also assisted by the decision to move directly to production masks, thereby replacing the ASIC prototype phase by a first batch of ASIC manufactured with production masks.
10. Subcontractor information

MAVIC needed to obtain competencies on RF communication and ASIC development and conducted a survey to find companies which:

1. are specialists in low voltage, low consumption CMOS integrated devices,
2. are highly competent in mixed mode ASIC design,
3. demonstrate a real know-how in RF signal architecture,
4. meet the tough economical constraints associated with consumer products,
5. have the necessary human resources to develop an ASIC in less than 12 months.

Three European potential partners were identified and preliminary discussions were conducted (technology potential and limits, existing circuits fulfilling some of the MAVIC demands, performances and costs of silicon technology). The two following subcontractors were selected:

10.1. Subcontractor n° 1, XEMICS/CSEM

The Centre Suisse d'Electronique et de Microtechnique was recognised as a world expert in low voltage, low consumption, CMOS mixed mode design having a good experience in RF architecture. Furthermore, its close location was an advantage for training and project meetings.

XEMICS/CSEM role was ASIC development up to working samples.

10.2. Subcontractor n°2, CREATIVE EURECOM

CREATIVE EURECOM was recognised as a world expert in radio frequency communication systems.

CREATIVE EURECOM role was radio frequency circuits development and control, impedance matching with antenna, communication software implemented in the micro-controllers.

10.3. Main contractual point

The contract which was signed with each subcontractor included confidentiality and intellectual property right clauses. The arrangements entered into ensured MAVIC had exclusivity of use of the application experiment ASIC device, and was the owner of the ASIC masks which were put on loan to the foundry.

11. Barriers perceived by the company in the first use of the AE technology

11.1. Lack of technical know-how

When developing a consumer-product, a systematic search for product optimisation has to be made. Trade-offs between technical and economical issues have to be reached at every step of development.

Having no background in ASIC technology presents problems:

1. Difficulty in assessing the proposals made by the ASIC designers:
   - is their technology the best for my application ?
   - is there a discrepancy between the claimed performances and the reality ?
   - is the solution truly optimised ?
   - are the development cost and price per unit fair ?
   - what are the possible tolerances on product characteristics ?…

2. Tendency to delay the development in its initial steps:
   - In feasibility study, choices of concepts remain questionable which pushes to look for various alternatives.
   - Preliminary specifications and architectures have to be thoroughly reviewed with ASIC designers for ASIC technology possibilities and limitations. Fast evolution of this technology induces specifications modifications which demand more simulations and laboratory tests.
3. Confidentiality (industrial property) and commercial reasons prevent from co-operating with ASIC designers too early in the project.

4. Lack of know-how leads to repeat 2 or 3 times some tasks.

11.2. Apprehension feeling
Lack of past experience in ASIC development tends to make people feel uneasy about ASIC development, performances and quality achievement and control. But no cultural barriers were present nor expressed by the FU.

11.3. ASIC modern testing ignorance
The functional tests of a circuit are very important to ensure full compliance with specifications. It was difficult to estimate the full capability of modern testers, the tests conditions (sampling, life testing) and their costs.

Thorough understanding of tests optimisation to fit an application is mandatory to choose the best compromise between low cost and over specification.

11.4. High risk investment
Mixed mode ASIC development cost varies for from 100 kEuros to 500 kEuros depending on circuit architecture, existing libraries and technology (the thinner the mask definition, the higher the cost). Without past experience, it is difficult to assess clearly development costs and the expected ROI which leads to poor risk evaluation.

12. Steps taken to overcome the barriers and arrive at an improved product

12.1. Lack of technical know-how
This barrier was overcome by selecting as subcontractors recognised world experts who, under MAVIC control, were put in charge of:
- Training and assistance.
- Overview on the various technologies available and the corresponding advantages and drawbacks.
- Choice of best technologies suited for the types of architectures fitting MAVIC present and future needs.
- Various concepts choice and evaluation toward thorough product optimisation at the feasibility study step.
- Design, development and evaluation, to be successful from the very first AE product delivery in performances and price per unit.

The training described in § 12.3, gave MAVIC some insight on the specific problems linked to ASIC development.

Furthermore, AE project follow-up brought profitable experience to MAVIC.

12.2. Apprehension feeling
Training on the various checks made during project development to ensure performance, quality and testability.

12.3. ASIC modern testing ignorance
Training to understand the means behind such fundamental steps as simulations (system, blocks and circuits), environmental and limit conditions tests, adaptation of circuits already available in library, new circuit design and layout.

Training on the possibilities offered by the modern testers and the test requirements to be taken into account early in the design phase.
12.4. **High risk investment**

The positive assessment of the original proposal by the European Commission experts was instrumental in convincing the management of the potential benefits of this innovation.

To evaluate the risk, MAVIC sent a request for proposal based on preliminary quite accurate functional ASIC specifications, to 3 different companies (selected by subcontractor 2) who developed ASIC in the past. The answers produced an estimation of development cost (at ± 30 %) and of ASIC price per unit.

Assessment of the ASIC development investment was achieved through follow-up development and price per unit permanent cost control.

13. **Knowledge acquired**

MAVIC anticipated the development of the following knowledge and capabilities during the application experiment:
- How to manage and control an ASIC development program to success.
- The technical knowledge and capabilities required of ASIC designers.
- The ability to produce clear and unambiguous ASIC functional specifications.
- ASIC development process requirements, lead time and dispersion avoidance.
- ASIC evaluation methods, and the ability to undertake the functional proving of the device’s performance.
- ASIC project management, and the ability to monitor target costs throughout the application experiment.

MAVIC successfully developed all of these skills, and at the end of the application experiment were confident in their ability to manage ASIC product developments.

14. **Lessons learned**

The company has learned that:

1. A strong electronic background is mandatory for undertaking a project of this complexity. This is mandatory because it is essential to be able to establish clear specifications for electronic circuits of the system, communication protocol and the overall system architecture.

2. Competent electronic engineers belonging to the company are mandatory. This allows these individuals to choose and assess subcontractors, and to co-operate closely with them in the feasibility study and preliminary specifications writing phases.

3. As far as project management is concerned, some crucial aspects have been highlighted:
- Constant project follow-up is required to avoid misunderstandings.
- A thorough understanding of the technical specifications of the product (and hence of its environment) is fundamental for success.
- At design stage, a meticulous awareness is crucial to review all the characteristics of design choices made by ASIC designer.
- Ability to evaluate the application in house is very important to ensure good qualification.
- Testing requirements must be written very early in the project to be taken into account in the design phase.

4. Some care should also be exercised in accepting initial evaluation results where complex RF ASIC devices are concerned. The company experienced product behavioural discrepancies between “state of the art” implementation boards used by the ASIC designers to test the ASIC and the implementation in the actual system due to space constraints. This could lead to big problems to be solved in the evaluation phase.
5. It is important to monitor development costs and production target cost per unit throughout the development process. These costs must always be clearly defined and maintained under control along the project follow-up meetings.

15. **Results, industrialisation and replication**

The MAVIC electronic derailleur system is operational and has met the specifications for the improved product. The performance of the improved system has been thoroughly tested during the evaluation phase of the application experiment.

The full production ASIC masks were developed as part of the application experiment. These masks belong to MAVIC. The typical tooling costs to be accommodated for the production of a full mask set and the expenditure required to obtain a first production batch of fully tested component is approximately 34 K Euro.

The hardware architecture around the ASIC and the software have been developed by MAVIC and improved through the various industrialisation steps. The skills acquired are further improved by additional testing being made on the end product.

The ASIC industrialisation process has already been proven through an engineering batch of 5000 circuits that were used to manufacture the pilot and pre-production end product at the end of 98. However, to get the ASIC ready for production, an additional 3 months effort was required to finalise the qualification and the industrialisation.

A production contract was signed by MAVIC and subcontractor 1 which is put in charge of supervising the ASIC production by the founder. This contract defines AE ASIC property, exclusivity, ordering process, delivery process, second source access if the technology in use is given up, production program actualisation and control processes (quality requirements, cost per unit, quantities, batches delivery dates) etc.

The components will be manufactured in Europe (France and Switzerland mainly), and the final assembly will take place in Serrières de Chautagne (Savoie, France).

This AE and the corresponding developed ASIC are ideal for wireless 1.5 / 2 m. communication links between portable devices thanks to the very low consumption level achieved. No other replication opportunities for the application of this technology has been identified by the company for bicycles, but other control applications are being explored.
16. Economic impact and improvement in competitive position

MAVIC’s objective is to take 5 to 10% of the OEM market and 15% to 20% of the after sales market within 3 years.

This sales growth will be achieved because the improved system provides the following benefits:
- Quick gear shift operation.
- Short assembly time, based on ease of mounting of the system components.
- Speed indication on system display.
- Compatibility with all cycle frame sizes.
- User feedback via visual presentation of gear position on the control and display module’s LCD display.

The sales projections for the improved product are identified in the following table (relative to projected sales levels for 1999):

<table>
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<tr>
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<th></th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Sales / 1999</td>
<td>40%</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>100%</td>
<td>250%</td>
<td>275%</td>
</tr>
</tbody>
</table>

In 1996, the ZMS electronic derailleur marketing was suspended because of the reliability problems with that system, and sales of the product without improvement would have been zero. The market share is expected to be largely increased due to high functionality of the new derailleur which does not have an equivalent (wireless gear shift) in the competitors’ product ranges. Sales profitability levels are the same as those achieved on the original ZMS system.

Based on the total system development costs, payback period estimates are less than 10 months and ROI in 2001 will be 350%. When based on mixed signal ASIC development costs alone, these figures become respectively less than 1 month and 3500%.

17. Summary of best practice and target audience

This AE can benefit to companies with mechanical design experience and a very limited experience in micro-controller systems entering into a complex RF ASIC device design.

Best practice aspects include subcontract and specification definition, and technical management of the project to produce qualified prototypes / pre-production units on time. The strategy for undertaking the design employed by the company gives an useful indicator to other companies in the same position.

The general target audience involves companies in the following sectors:
- Transport equipment, Prodcom code 34-35
- Sport articles, Prodcom code 364
- Machinery, Prodcom code 29
- Appliances for checking testing Prodcom code 33

* * *