

FUSE Demonstrator Document

ASIC full colour LED Display Driver.

*From discrete drivers to highly integrated ASIC for large displays,
including memory and data transfer management.*

***FUSE PROJECT
AE:22 918***

First User: Focon Engineering A/S

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Title

ASIC full colour LED Display Driver.

From discrete drivers to highly integrated ASIC for large displays, including memory and data transfer management.

AE Number

AE 22 918

Abstract

This demonstrator describes the First User Experiment (FUSE) 'Mixed Analogue/Digital ASIC for Graphical Colour LED-Display'. The First User (FU) - Focon Engineering A/S – has its primary business in design and manufacture of information and communication systems for public transportation systems.

The objective of this Application Experiment (AE) has been twofold; the adaptation of ASIC technology in the aspect of design and manufacturing, and an improvement of Focon's standard monochrome displays based on one LED per dot to full graphical multicolour displays. The existing product is based on standard TTLs and discrete components.

Before this experiment, Focon had no experience in ASIC design methodologies and no design equipment for this area. In the area of analogue ASIC design, Focon is now able to specify and control the development process, and in the area of digital ASIC design; Focon is now able to do the design work in-house.

Regarding digital design, Focon is now able to use VHDL as a design tool, thereby enabling us to become independent of existing technologies. Using this technology, we have at the moment – besides the Mixed Analogue/Digital ASIC for Graphical Colour LED Display - designed our first FPGA, the next one is coming up.

Concerning the Mixed Analogue/ Digital ASIC, the experiment was – after a work-around for a bug in the analogue ASIC part - concluded with functional prototypes.

A multicolour demo display with the required improvements was also concluded as planned. At present, we are waiting for the multicolour LED technology to mature over the next years, to improve our opportunities of marketing the new graphic multicolour display towards which the ASIC is directed and thereby to improve our market position.

The duration of this AE has been 16 months and the cost was 160,000 Euro for the design and prototyping plus 40,000 Euro for the industrialisation of the new product.

Due to price of 3-color LED is not declining as expected, a ASIC utilising a 2-colour LED will be introduced to the market to maintain market shares.

The payback period of the 3-colour version is 6 months and for the 2-colour is 12 months of production. The ROI is 800% for the 3-colour version and 259% for the 2-

colour version.

The planned Workplan was delayed by approx. 2 months, basically due to a delay in the design merge at the ASIC subcontractor, and due to the time required to find a workaround for an oscillation problem in the analogue part of the ASIC.

Keywords

Mixed signal ASIC, current driver, LED, information system, transportation, train, graphical communication, LED Colour display

Signature: 5-03205551155-3-3550-2-35-DK

1. Company name and address



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2. Company size

Focon has 75 employees, of whom 30 are working with R&D. Focon is, in all aspects, a first user of ASIC design methodologies. The 1998 revenue of FOCON is app. 10 MEuro.

A total of 4 developers are involved in this project and these are 2 software developers (Henrik Andersen and Søren Bondesen) and 2 hardware developers (Lars Dalvig and Kim Petersen). Project manager is Kim Petersen. All involved are first users of ASIC's.

3. Company business description

Focon was established in 1987 by Jens Østerlund in 1987. The aim of the company was to design and manufacture visual information systems for railways as well as reservation and information systems for train stations, ferries and busses.

Over the last years, the primary business has been focused on design and manufacture of information and communication systems for public transportation systems. Since 1993 the information systems have been extended from simple textual displays to complete information systems including graphical displays, internal and external PA-systems, crew communication, emergency passenger talkback, audio entertainment, video entertainment and surveillance.

Focon Engineering is known as a quality supplier and innovator of information systems. Introduction of three-colour LED system will re-emphasise this image in the market.

Product development is performed mainly in house. Several product are being customised for each specific project, hence flexibility in finalisation of product is essential to FOCON.

Activities carried out by the company include sales, design, manufacture, service and maintenance on units returned from the end user. Concerning manufacture, most activities are placed with subcontractors. Final assembly, test and quality inspections are carried out at Focon.

4. Company markets and competitive position at the start of AE

Focon is a leading manufacturer of complete railway information systems in Europe.

The railway information system industry is defined as the companies supplying complete railway information systems including graphical displays, internal and external PA-systems, crew communication, emergency passenger talkback, audio entertainment, video entertainment, and surveillance.

In relation to the market of textual, audio and video railway information systems Focon is doing business in Denmark, Sweden, Germany, England, Belgium and Portugal.

The market share is estimated to be 20 - 60%, depending on the countries.

Focon's strength is within railway information system. Essential competitors in different countries are:

England: IGG, JASMIN
Denmark: ScanAcoustic, Modulex, Infocom
Sweden: ScanAcoustic, Modulex, Meisner
Germany: Siemens WKF, Buselectronics, Meisner

These competitors all offer products, which are comparative to Focon's products. None of them manages full graphics or full-coloured LED displays. Focon has a major competitor within our primary business market. We presume that this competitor remains focussing on textual and monochrome display techniques.

Focon is known as a quality supplier and innovator. The image as innovator will be re-emphasised by bringing the 3-colour LED display to the market.

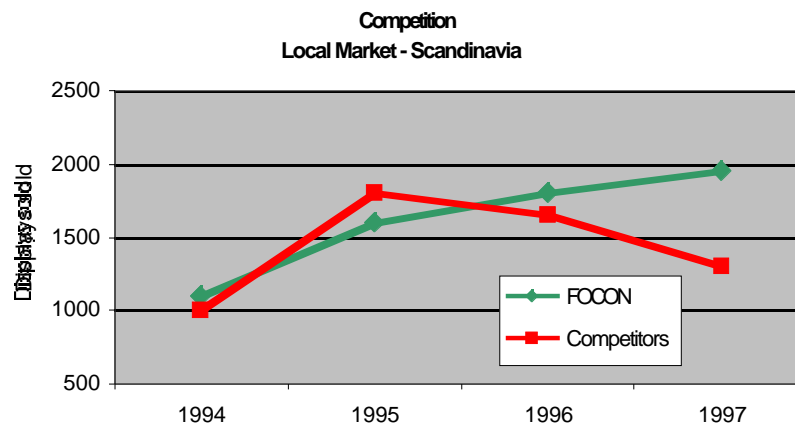
The 1998 revenue of FOCON is approximately 10 MEuro. However, the company had losses in the period 1994-95, due to missing introduction of new product to market.

Focon has 10 years of experience in single LED products, whereas information systems with full coloured LED is a new product area. This new technology will give Focon a technological lead and increase our competitiveness, and help us remain in the market.

The pricing of each type of LEDs is however an important factor to determine the time of introduction to market. The 3-coloured LED is a new product with initial pricing being high and expected lower price over the years. However, the LED manufacturer has found greater profit in improving their market share of 1 and 2-coloured LEDs. This means that the expected decrease in pricing has been delayed. As a result Focon have postponed their introduction of the 3-coloured LED display systems.

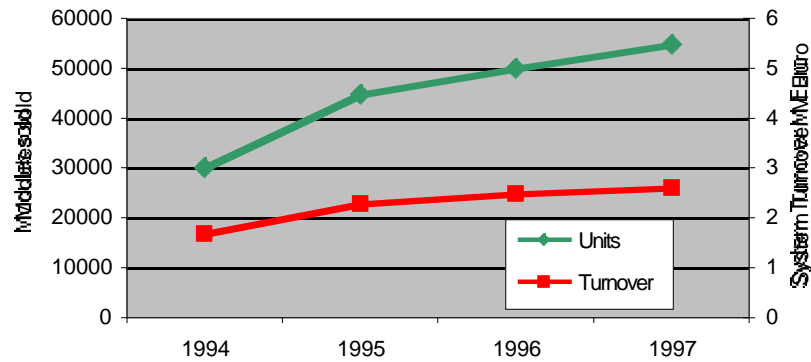
Focon has made a preliminary feasibility study; analysing trends in technologies, components and requirements for large display systems based on LED's. It is obvious that future applications will require full graphical colour displays, whereas today's standard is monochrome displays based on one LED per dot. It is estimated that the market trends in all countries will be towards firstly introduction of full graphics and secondly full-coloured displays. In the past five years the market has technological developed very slow. However, the introduction of high-speed train systems is the driver for innovation of fully integrated information systems, which is requesting added features in displaying the information. FOCON estimates a 10-20 % increase in demand per year in the next 3 years.

The competition within the local market - Scandinavia and Germany - has during the past 4 years developed as shown in the graph. The Focon increase in market share is mainly related to Focon being a supplier of full information and reservation systems rather than displays only.



The total sales of display modules within the past 3 years have developed as shown in the graph below.

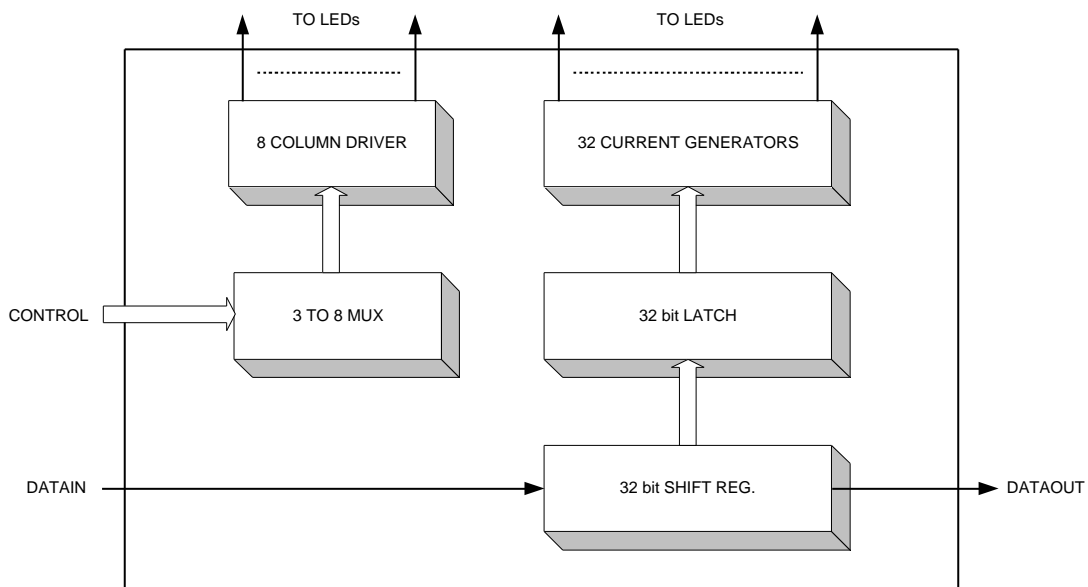
Economic History



The success of Focon is mainly driven by the ability to develop complete customised information and reservation systems to the right price, dimensions, quality and time. The pricing of our products are estimated to be similar to competitor products with same features.

5. Product to be improved and the reason to innovate

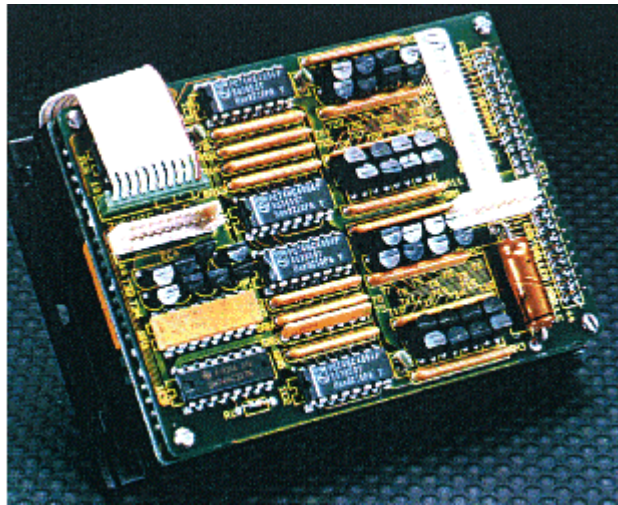
The product to be improved is the existing 16 x 16 dot LED matrix module. This module consists of 32 fixed current generators, a 32 bit latch, a 3 to 8 multiplexer, and some passive components on a PCB. For reference, see the following block diagram:



Functional block diagram of existing monochrome 16 x 16 LED module

The circuit is implemented with discrete components (40 transistors, 6 MSI components, resistors and capacitors). The functionality of the product is to drive a 16 x 16 matrix of LED's, organised electrically as an 8 x 32 matrix. A CPU-based display controller sends data to the module and controls the scanning via control signals. For

reference on the physical appearance, see the following picture:



Picture of existing monochrome 16 x 16 LED module

Within reasonable limits, 16 x 16 LED modules may be cascaded to form the desired display size.

Concerning environmental condition, common temperatures for the LED displays developed at Focon is $-20 \text{ .. } 50^{\circ} \text{ C}$. Due to internal temperature rise – mainly due to power dissipation in LED's and current sources - the LED module must be specified for ambient temperatures of $-20 \text{ .. } 65^{\circ} \text{ C}$.

The innovative driver of the product is primarily to add features within the same space. The limited space per pixel requires higher integration of functionality, thus new technology was to be introduced.

Cost reduction has also been an important driver for this project to remain competitive on the market. It was evaluate that the loss of market share 4 years ago was related to the fact that FOCON didn't comply with added request for full-coloured and animations features. These features required implementation of 2 and 3-coloured LED display modules with request of higher integration per space, thus the only way for FOCON to stay competitive was to development of the new product, which include the technological step to design of mixed ASICs.

6. Description of the product improvements

The goal of the ASIC is to bring Focon in the position of offering full graphical multicolour displays, whereas today's standard is monochrome displays based on one LED per dot. By using the ASIC, we plan to obtain price competitive graphical colour displays controlled by a dedicated graphic controller. The solution is demanded to be smaller in size than the existing product, have more functionality (text based graphical, monochrome multicolour and higher data rate required for animation) as well as reaching superior reliability, and reduction in component count and overall costs. The product requires 3 times more LEDs and drivers with the same space. The total resolution of the display is 4096 colours.

The objective of introducing the 3-colour LED Display was to expand the market of our product in terms of added features and application of the usage to product. A new application of the product is applying full-coloured advertisement videos to the system, hence giving the information provider (final user) access to added income or coverage of expenses of the information system.

Introduction of 3 LEDs technology by means of conventional technology would require 3 times more space on the PCB, which would jeopardise with size requirement of the final product. Also the control of each colour needs separate attention as the efficiency of radiated light versus LED current differs from the range of 5mA of the red LED to 50 mA for the blue LEDs. Programmable current levels are required to have full colour control the display. Thus, integration is necessary to comply with this requirement.

The "intelligent" ASIC is to control an array of 16 x 16 dots, where each dot is made of three LEDs (red, green and blue). Also, to achieve data update rates required for animated graphics, the ASIC must relieve the display controller in performing the scanning scheme of the module.

The total chip size is approximately 30 mm², while the analog part (mainly drivers) covers 5 mm². It was processed using 0.8 μm CMOS technology.



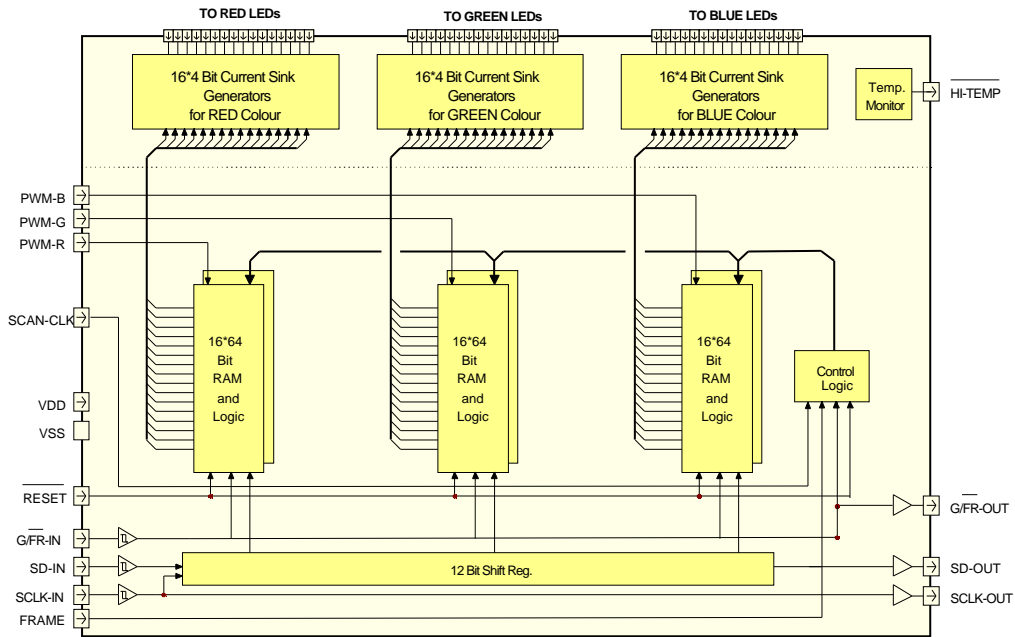
Picture of the developed ASIC

The new and improved product/ASIC contains the following functions:

- 3 x 16 programmable 4 bit current sink generators.
- 84-pin QFP package
- chip size 30mm²
- 2 independent picture frame memories. One picture frame memory is updateable while the other is "shown".
- A PWM input signal, one for each colour.
- 3 current reference inputs, one for each colour.
- High speed serial interface.
- Temperature supervise circuit to control overheat.
- Picture frame input to switch between pictures in the two frame memories

- Complexity: 5.5 K gates logic + 6 x 1024 bit RAM + analogue current generators,

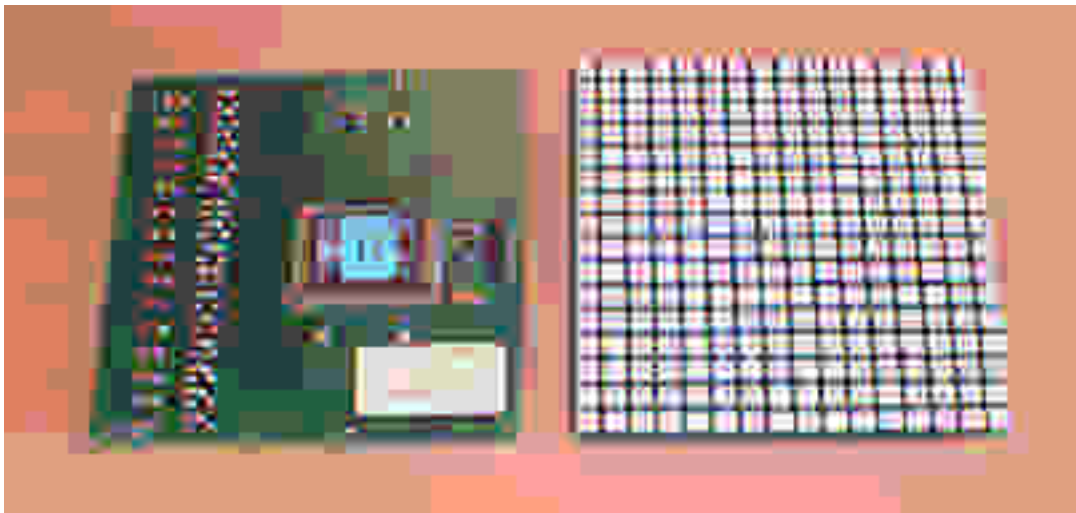
Please also see the simplified functional block diagram below:



Functional block diagram of the developed ASIC

For the construction of a demo display for this specific project, a new graphical colour 16 x 16 dot LED module based on the new ASIC was made.

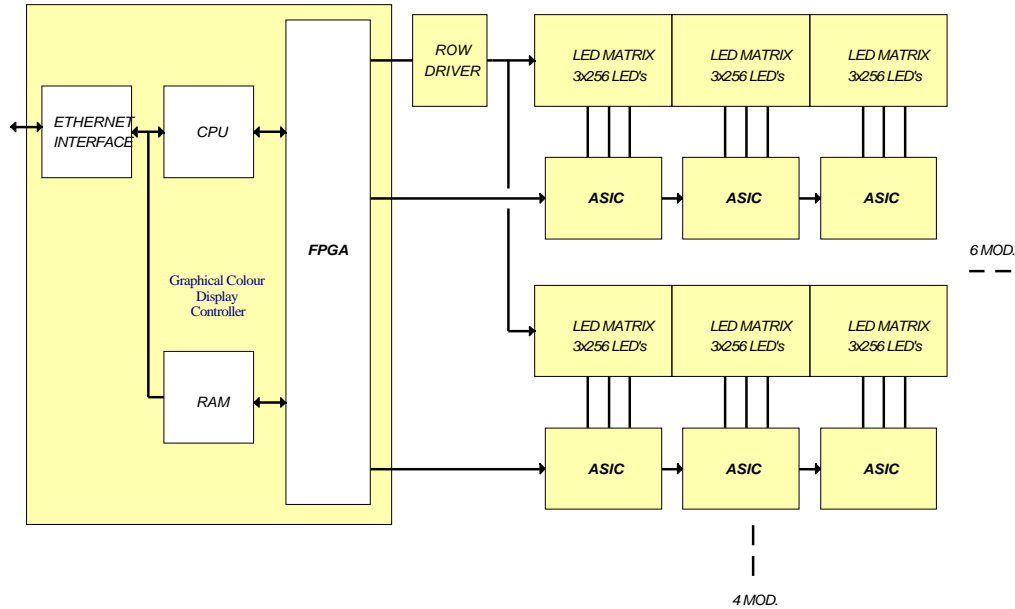
The new circuit is implemented using few discrete components, the ASIC and the 256 3-colour LED's. For reference on the physical appearance, see the following picture:



Picture of developed multicolour 16 x 16 LED module

To construct a graphical colour demo display, 24 of these modules were integrated on

a larger PCB to perform a 96 x 64 dot display. Also integrated was a new developed dedicated graphical controller based on a FPGA and a μ controller. The FPGA supplies as co-processor pattern format, memory-interface, and take care of the serial I/O interfacing for the μ controller. The complexity of the FPGA is approx. 4 K gates. For reference, see the following draft block diagram:



Draft functional block diagram of the developed demo display

For reference on the display physical appearance, see the following picture:



Picture of developed colour demo LED display

7. Choices and rationale for the technologies, tools and methodologies

To enable choice of suitable technology and methodology an analysis was initiated. The development group at FOCON carried this analysis with support from the TTN centre.

Expected Volume:

The expected volume is important to determine as it a tool to predict the financial frame of the design work.

The projected sales within the period 1997 to 2003 were estimated at 120,000 modules per year. It is estimated that each display will consist of 14 modules.

Display technology:

For the display technology Focon has considered the following methodologies:

1. A μ controller combined with some standard analogue components to drive the LED's. This solution is not capable of supporting the required data rate for animations, it will require a large number of component count and thus take up too much space and result in low reliability and high overall cost.
2. A FPGA or GateArray combined with some standard analogue components to drive the LED's. This solution will support the required data rate, but will otherwise have the same disadvantages as for solution 1. Furthermore the sink current of up to 100 mA (simultaneous on up to 16 outputs) was too high for most FPGAs.
3. A mixed signal ASIC with all the functions on one chip. This solution will support the required data rate, take a minimum of component count and space, and result in a good overall cost.

It was concluded that a mixed signal ASIC satisfies our requirements to functionality, as well as will give the best overall solution in respect to component count, space, reliability and cost.

Design tool

We initiated an investigation as to which tools are available, what is the difference between them and their coverage.

Among others, we looked into:

Xilinx, Altera for FPGA designs.

Veribest, Viewlogic, Galileo, Mentor Graphics, Synopsys in relation to ASICs

To be able to make our choice, we set up different criteria:

- Entry possibilities

- Simulation opportunities
- Synthesis possibilities
- Input and output formats (thereby interface to Thesys)
- Support and training course
- Necessary hardware and software platform (workstation/PC, Unix/NT)

By giving priority to the criteria and having the different tools demonstrated we chose ViewLogic consisting of ViewDraw (Schematic entry), Speedwave (VHDL simulator), ViewSynthesis (VHDL gate level) and ViewSim (Gate level simulator). This choice has posed some problem, since Thesys initially did not interface with such tools. However, the final VHDL code was used and converted into Verilog by Thesys.

Design methodologies for the ASIC:

Different methodologies can be used for the design process of an ASIC:

1. Schematic capture using library modules from the selected ASIC vendor
2. HDL (Hardware Description Language) technology independent standard language coding following by synthesis using vendor design kit

Please note that option 2 is only valid for digital design.

In general terms FOCON wanted to place the investment for design tools in PC based tool rather than WS, as it is cheaper. We also wanted to have synthesis capabilities for an FPGA and/or ASIC implementation.

The ASIC to be designed was intended to be a standard cell type with an analogue part and a digital part. Also, for the analogue part some custom cells was to be designed.

As first step, it was decided that the analogue part was to be designed by a subcontractor. The reason for this was the risk combined with the specialised task of analogue ASIC design, and the required investment in expensive design equipment and training.

On this background, Focon was free to choose between doing the 'digital' part via schematic capture and/or HDL.

As one of the intentions with the AE was for Focon to gain knowledge about using VHDL tool, and as the 4 persons allocated to the project have previously been taking a mini-course in VHDL design in preparation for the introduction of this techniques into FPGA design, VHDL was chosen. Further, this choice was supported by the design flow, offered by the evaluated ASIC vendors. Our choice did however pose some problems, since the subcontractor was to implement this support for the first time.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

Focon has developed electronic equipment using standard component on PCBs. Focon is experienced in hardware and software engineering based on the use of μ controllers, and high level programming. The company has already used PCB layout tools and PAL assembly tools, and uses a few PLD's in some products. All production and assembly of PCBs is subcontracted, thus Focon had experience in subcontracting.

Focon is a first user in all aspects of microelectronics and ASIC design. The only background of the persons allocated to this project regarding complex digital design was a purely theoretical and as to size very limited course in VHDL.

Thus, purchase of VHDL design tools as well as training in ASIC design flows, VHDL design and synthesis and the purchased design tools were required.

9. Workplan and rationale

A workplan was set up to control and manage the execution of the project. Rationale of phase splits of the workplan was mainly depended on the technology chosen, the capability at FOCON and interface to subcontractor. The workplan is shown on next page.

Rationale

As the capability of FOCON prior to the AE didn't include digital nor analogue design these capabilities had to be added to the project either as a technology transfer to FOCON or to be performed at subcontractor. Furthermore it has been concluded that a technology step to mixed signal ASIC was too comprehensive for FOCON, thus the most advanced part of the step was decided to be subcontracted. The overall split of tasks was defined as digital design is to be performed at FOCON, while analogue design and manufacture of silicon was to be subcontracted. In the rationale for the subcontractor it was feasible to have the same subcontractor for both the analogue design and the manufacture of silicon.

Risk Analysis

A risk analysis was conducted to focus on potential risk elements. The analysis was focussed on subcontractor performance and price declination of 3-coloured LEDs.

Having an alternative silicon foundry subcontractor was considered important. This consideration was based on the Focon being uncertain on interfacing to silicon foundries.

Pricing of 3-coloured LED modules is vital for the price of the final product. As a decline in price was predicted it was decided that use of 2-coloured LED modules could be possible within the new design. The 2-coloured version is to be produced anyway for application not requiring the full-colour option. It is worth noting that a 2-coloured version utilises 256 colours resulting from combinations of these 2 colours.

Contingency plan

1. During the feasibility study each potential subcontractor was to be evaluated as alternative supplier as well.
2. In case price of 3-coloured LED modules does not decline use 2-coloured LED modules is to be applied in the first product. Design has to be prepared for a 2-coloured LED version

Activity	PERSON	Month																
		Feb 97	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan 98	Feb	Mar	Apr	May	
Technical management	P 2.0 A 2.1																	
WP 1A – Specification	P 3.0 A 3.9																	
Specification, ASIC and display	Focon	P 2.0 A 2.4																
Submission to design house		P 0.8 A 1.2																
Contract with design house		P 0.2 A 0.3																
WP 1B – ASIC Analogue design	P - A -																	
Design of analogue part	Thesys	P - A -																
Analogue design – Tape out		P - A -																
WP 2A – Training & digital design	P 6.0 A 6.0																	
Training VHDL (Thesys)	Focon	P 0.3 A 0.5																
Training Simulation & Synthesis (ViewLogic)		P 0.2 A 0.3																
Design of digital part		P 5.5 A 5.2																
WP 2B – ASIC prototyping	P - A -																	
Merge design and post layout	Thesys	P - A -																
Prototyping of ASIC's		P - A -																
WP 3 – ASIC test & display prototyping	P 4.0 A 3.4																	
Prototype PCBs for the demo display	Focon	P 0.9 A 0.7																
SW for demo display and PC		P 1.0 A 0.7																
Prototype display controller		P 1.4 A 1.2																
Functional test of the ASIC		P 0.4 A 0.5																
Functional test of the demo display		P 0.3 A 0.3																

- **Who did what**
Kim Petersen performed these tasks as project manager except for the cost follow-up, which was performed by the financial manager, Aage Andersen.
- **Responsibilities**
The project manager had the overall general responsibility of the project
- **Knowledge transfer**
Knowledge on management of ASIC design specific in dealing with subcontracting of silicon manufacturing was transferred to the company

Workpackage 1A Specification

Technical specification of functionality and performance of the new ASIC and testing requirement

- **Work done**
Analysis of requirement,
Analysis of feasibility including estimate of final costs and size of chip
Block diagram level specification
VHDL design training
Contract with the design house
- **Who did what**
The project team at FOCON performed these tasks. The subcontractor did support in terms of feasibility and requirement for the silicon manufacture.
- **Responsibilities**
The project manager had the responsibility of this WP
- **Knowledge transfer**
Knowledge on capability of the specific ASIC technology and VHDL design work was transferred to the company. Furthermore, knowledge on subcontracting was transferred

Workpackage 1B Analogue Design

Design of analogue part, Analogue design and tape out

- **Work done**
Design of Analogue part
Analogue design coding
Tape Out
- **Who did what**
The subcontractor performed these tasks.
- **Responsibilities**
The subcontractor had the responsibility of this WP
- **Knowledge transfer**
Knowledge on required input to the subcontractor and how to interpret reports from the subcontractor was transferred to the company.

Workpackage 2A, Training & digital design

Training VHDL, Design of digital part, Simulation & Synthesis

- **Work done**
Training VHDL design of digital part
Design of digital part

Simulation & synthesis

- **Who did what**

The project team at FOCON participated in these tasks. The technical staff at FOCON design the digital part with consultancy from the subcontractor.

- **Responsibilities**

FOCON had the responsibility of this WP

- **Knowledge transfer**

Knowledge on VHDL design work and hands on experiences was transferred to the company.

Workpackage 2B ASIC Prototyping

Merge of designs and prototyping of ASIC's

- **Work done**

Merge of design,

Design check run

Accept of layout

Manufacture of prototypes

- **Who did what**

The subcontractor performed these tasks, except for the acceptance of layout which was performed by the project team at FOCON

- **Responsibilities**

The subcontractor had the responsibility of this WP

- **Problems**

The tools at subcontractor had no interpreter for Verilog files. This interpreter was added by subcontractor. This resulted in a minor delay.

- **Knowledge transfer**

Knowledge on capability of the specific ASIC technology and VHDL design work was transferred to the company. Furthermore, knowledge on subcontracting was transferred

Workpackage 3 ASIC Test and Display Prototyping

Prototype PCB for demo display, SW for the demo display and PC, Prototype display controller, functional test of the ASIC and functional test of the display

- **Work done**

Prototype PCB designed and implemented

Software for the PC and display

Functional test of the ASIC using test bench board

Functional test of the display

- **Who did what**

The project team at FOCON performed these tasks, except for the manufacture of PCB which was subcontracted.

- **Responsibilities**

The project manager had the responsibility of this WP

- **Problems**

The ASIC show a minor error. The current generator was modulated with a 200 kHz sinus. The error was determined to relate to the bandgap reference cell, which a standard Thesys cell. This error wasn't visible in the final

prototype and will be corrected in the next ASIC run.

- **Knowledge transfer**

Knowledge on testing prototype ASICs was transferred to the company.

Furthermore, knowledge on subcontracting was transferred

Scheduled efforts versus actual efforts.

Workpackage	Task Cost	First User effort		Subcontractors cost	
		Planned	Actual	Planned	Actual
Management	8.8 KEuro	22 Persondays	26 Persondays		
Specifications	11.2 KEuro	66 Persondays	86 Persondays		
Design	56.2 KEuro	132 Persondays	132 Persondays	30 KEuro	32 KEuro
Prototyping	66.2 KEuro			40 KEuro	45 KEuro
Evaluation & Test	17.6 KEuro	88 Persondays	75 Persondays		
TOTAL	160 KEuro	308 Persondays	319 Persondays	70 KEuro	77 KEuro

10. Subcontractor information

Subcontractor for Analog design and manufacturing of silicon was necessary to fulfil the project. FOCON selected the following subcontractor:

Subcontractor

Thesys Gesellschaft für Mikroelektronik mbH
 Haarbergstrasse 61, D-99097 Erfurt, Germany
 Peter Madsen, C-88 A/S, Danish representative

Contact persons

Matthias Deike, Sales
 Thomas Liebetrau, Application Engineer
 and respective designer

Size and history

Thesys has approx. 500 employees and a long history as both semiconductor manufacturer and design house.

Business

Design support from head office in Erfurt and other small offices several places in Germany. Production is located at own 6-inch wafer fab in Erfurt.

Service provided

Design support and ASIC manufacturing.

Expertise

Thesys has expertise and experience in design and production of standard ICs and ASIC's. They have experience in the following application areas: industrial, automotive, medical and telecom application.

Rationale for selecting the subcontractor

The subcontractor was chosen on the following basis:

- Geographical placement
- Experienced team and long history as both semiconductor manufacturer and designer
- Good experience in both digital and analogue ASIC design
- Smooth communication on the technical area
- Quick response to technical inquiries
- Best pricing offer

Two other companies were considered as subcontractor. These were DELTA and ES2, since they also offer design and manufacture for mixed signal ASICs. However, when using the selection criteria, Thesys came out top.

Contractual matters and the interface between the subcontractor and FU were defined in a contract agreed upon by both parties. The contract included matters of interface, penalties, IPR and delivery terms. 40% payment was to be prepaid, while the remaining invoice was to be paid at the time of prototype acceptance. Ownership of complete schematics, netlist and simulation results was stated as belonging to Focon. The responsibility of correct implementation of the coded design was laid on the subcontractor, while functionality of the FOCON design work was laid on the FOCON.

PART II

11. Barriers

Prior to the AE, a number of barriers prevented Focon from adopting the ASIC technology to improve the products and thus gain a better market position.

The barriers ranged from adapting ASIC technology, to learning design and verification methodologies as well as technical and financial uncertain factors related to introduction.

Knowledge barriers

The knowledge barriers, which have prevented Focon from introducing the ASIC technology, are:

1. Which functions can with advantage be realised by means of ASIC technology ?
2. Which technical risks are related to the introduction of the technology ?
3. Which ASIC supplier do we choose ?
4. How do we interface to the ASIC supplier and which design functionality's can we make ?
5. How to evaluate risks related to the ASIC technology

Technology barriers

Neither Focon nor any of the R&D staff had experience in ASIC design methodologies and Focon has no design equipment for this area. Thus, a lot of questions have remained unanswered regarding the new technology, technology; some of these are listed below:

1. Which limitations does the technology have ?
2. What are the possibilities concerning design flow ?
3. Which type of development tools do we need to design an ASIC ?
4. What characterises the individual ASIC technologies (Standard Cells, Custom Cell, and Gate Array) and what are their advantages and disadvantages ?

Financial barriers

We have met a number of financial barriers of which the most important are:

1. Lacking background to be able to estimate costs connected to the introduction of the technology
2. The fear for high and unestimated costs in connection with redesigns.

12. Steps taken to overcome the barriers and arrive at an improved product

Prior to the preparation of the FUSE proposal, Focon has made a preliminary feasibility study; analysing trends in technologies, components and requirements for large display systems based on LED's. It was obvious that future applications would require full graphical colour displays, whereas today's standard is monochrome displays based on one LED per dot.

Barriers to overcome during the AE have been focused on transfer of ASIC technology into the company. This included the purchase of design tools and training related to design and manufacturing of the actual ASIC. In addition, Focon planned the work relating to both external processing at the subcontractor (wafer fab) and the internal processes, in order to overcome the barrier associated with planning.

Training

One of the parameters in our choice of design house was their opportunity of offering us a training course.

This course (3 days) went into details with the following:

- The phases of an ASIC design.
- Who takes care of which phases.phases?
- What to pay special attention to in the different phases.
- Which formats are available (which support the design house) to transmit data from Focon to the design house.

As to VHDL design and synthesis we chose a training course from the supplier of selected design tools:

This course (2 days) was directed on Viewlogic Office:

- Digital design flow.
- Behavioural level test
- VHDL Synthesis.
- Synthesis-right VHDL code.
- Gate level test

REF

The TTN also provided support and knowledge transfer in matter of:

- management of ASIC
- project specification
- test specification
- subcontracting of ASIC design
- subcontracting of ASIC production

13. Knowledge and experience acquired

The primary knowledge achieved by Focon has been the adaptation of ASIC technology in aspect of design and manufacturing. To spread both ASIC technology and HDL design processes, a total of 4 developers have been involved in this project. These are 2 software developers (Henrik Andersen and Søren Bondesen) and 2 hardware developers (Lars Dalvig and Kim Petersen).

Key knowledge achieved includes:

- Introduction of VHDL tools (Schematic entry, VHDL simulator, synthesis and gate level simulator)
- Acquiring VHDL tools
- Selection of subcontractor(s)
- Setting up plans for ASIC Projects
- ASIC design flow and VHDL coding/synthesis training related to the personnel in the project group
- To make ASIC requirement specification and to break this up into small function blocks for realisation
- Digital micro-electronic design using VHDL technology independent standard language coding
- Synthesis process using vendor design kit. A most important experience gained here is the coherence between the VHDL coding and the result of the synthesis tool.
- Simulation and verification of VHDL and gate level
- The generation of test vectors for verification during the final design process at the subcontractor as well as for production testing.

Apart from the scheduled knowledge transfer on digital design and ASIC project management, which has been acquired, the project team at FOCON gained deeper knowledge in analogue design than previewed.

Further to the experiences with VHDL and ASIC design we have by means of this project designed the first FPGA in the history of Focon. This has been used in the developed graphics controller. The FPGA supplies as co-processor pattern format, memory-interface, and take care of the serial I/O interfacing for the μ controller.

Also, Focon is for the moment designing another FPGA for an entirely new project. The expected complexity is about 5 K gates.

14. Lessons learned

Part of the experience gained through this project comes, naturally, from the problems we have had with the project.

The purpose of this paragraph is thus to pass on to other FU's what to pay attention to.

Regarding the implementation of the project, we have had 4 persons allocated to the project part time. The advantage to this was, of course, that in this way it was easier to pass on our experience to the R&D department. A disadvantage was that with the relatively short time each participant had for the project it was difficult to acquaint technologically with all the new subjects. This meant that the project co-ordinator had to spend some energy to keep things together. To maintain a grip on the situation, we all had to gain the necessary basic knowledge.

The specification of ASIC lasted longer than expected, thus the lesson learned is that the allocated effort to the task was sufficient, but the task of 'on the job training' in this matter was neglected. As a first user it is essential in advance to detect possible training items.

The choice of design tools and specification of ASIC took longer than expected, as many things had to be harmonised with both parties. Focon's expected investment in design tools and requirements to the ASIC as well as Thesys' requirements to the design interface and their opportunities regarding implementation had to be described. The lesson we have learnt is don't rush the decision, because it is important for future development work.

Regarding design tools, we believe that the decision to use VHDL was right because of the price advantages and the fact that we also in future plan to use this tool for FPGA designs, - an area where VHDL is very widespread. However, the ASIC subcontractor (Thesys) preferred Verilog and that we developed via relatively expensive design tools. We ended up with choosing a VHDL design tool from ViewLogic. Thesys had a similar tool, however for unix, Unix, and as we wanted to maintain our PC environment, we decided that Thesys could do a new ViewLogic NT design kit for Focon.

Except test strategy, the design of the digital part passed without any major surprises. Owing to the two different platforms, the integration of the digital part with Thesys took, however, longer time than planned.

Regarding our choice of ASIC test strategy in the design phase, we decided to make use of Thesys' expertise and knowledge on their Automatic Test Equipment (ATE). As we had some specific requirements to the test of the analogue current sink generators, and as Thesys had an ATE fulfilling these requirements, we agreed that it would not be necessary to build-in an extra test functionality in the ASIC. The test principle was to write specific data to the ASIC and then verify the written data via the analogue current generators. In this way, ASIC logic, RAM and the analogue current sink generators could all be tested based on the ASIC's normal functionality.

By the end of WP 2 when we were to generate test vectors, it proved that the chosen test strategy caused problems concerning the test time. The analogue inputs on Thesys ATE had relatively long settling times, which resulted in a relative long and thereby

costly RAM test time. The optimal solution would have been to include extra test logic in the ASIC design to be able to test the RAM blocks independently from the current sink generators, e.g. by means of digital out clocking of the RAM contents. At the actual time, this solution would have led to even more delay because of the necessary redesign and simulation.

We therefore decided, together with Thesys, to maintain the chosen test strategy. To reduce the test time, Thesys made a test adaptoradapter containing fast Analogue to Digital Converters (ADC), to avoid the slow settling times for the analogue inputs of the test equipment in this way.

We must conclude that the above problems are caused by the fact that Thesys in the first design phase - because of lacking time resources - were not good enough in their technical sparring.

PART III

15. Resulting product, its industrialisation and internal replication

As described REFFORMATVERBINDENa new graphical multicolour 96 x 64 dot display was developed. Additionally a new dedicated graphical controller consisting of an FPGA and a μ controller has been developed and integrated into the product. The LED matrix was realised by 24 modules each having a new 16x16 dot LED module based on the developed ASIC. The resulting display modules consist of one ASIC and either a 3-colour or 2-colour LED-unit. The new circuit is implemented using few standard discrete and integrated components, the ASIC and the required number of LED units.

Also a Windows PC software for downloading bitmap pictures to the display was developed. In the current version, the display may be controlled to show static colour pictures or animated graphics controlled by the host (PC).

The prototypes were electrically tested at FOCON using the developed test board. 69 of 110 units were found acceptable for the prototype display. Regarding the visual aspects, the result is very satisfactory. However, it must be noted that the present PC software cannot handle a data rate corresponding to real time (25 pictures/sec.).

For the 3-layer layer PCB was applied for the prototype. Due to the high currents (200 Amps) implied the ground level turned out to be unstable. Thus it has been decided for the final product to add an 4th layer to the PCB for grounding.

After successful testing of the prototype the following tasks for the industrialisation of the new product have been performed. New ground layer added of PCB to minimise noise. Mechanical redesign to comply with PCB size and thermal considerations. Redesign of test bench to optimise effort of testing and mass production. The total time spent for industrialisation is 4 months.

Problems related to the LED technology has both technological and cost-related nature, which unfortunately are outside the control of Focon.

The technological problem is that the few 3 chip LED's available on the LED market today have common anode. However, the forward voltage for the 3 LED's varies in their respective working area from about 2.0 V (red LED) to about 4.3 V (blue LED). This results in a heavy increase in the power dissipation in the ASIC current generators, a problem which we have solve by inserting zener diodes at the ASIC/LED interface.

The problem of costs is also related to the LED unit. Introduction of the 3 chip LED's has been essentially slower than predicted by manufacturers during our feasibility study. The expected decline in prices has not taken place. At present the price of the applied LED is 0.9 Euro per unit, which complicates the marketing of the product. The LED price is dominated by the needed technology for the blue chip.

This means that the 3 chip LED technology has not matured yet. Two world-wide LED suppliers - Rohm and Sharp - expect that within 1-2 years they will be able to offer integrated modules (e.g. 16 x 16 matrix) with 3 chip RGB LED's. Not until then, will there be any basis for a more widely introduction. For LED modules in general, it will be possible to do custom types regarding pin layout. Also in future, it will thus be possible to develop custom modules regarding separate anodes for the 3 colour groups. Due to the complexity and size of the ASIC it is not feasible to implement the ASIC into a monochrome display system.

For the mean time, whilst the price for the 3 chip LED's is settling, for many applications we have focussed on an adequate alternative, which is a display based on 2-coloured (red and green) chips only. The solution gives an adequate alternative innovation in the display features and a display based on this technology is considerably cheaper and will give a competitive product in the range of enhanced multicoloured display systems. This product was introduced to the market in August 1998.

The 2-coloured LED version has been put into production in 1998. The 3-coloured version is going into production by the end of 1999 for use in the new train system for the coming bridge between Denmark and Sweden.

The industrialisation of the product for both versions has required an additional cost of 40 KEuro.

Furthermore, Focon plans to have a new FPGA for digital design in order to redesign the single LED product in order to improve its integration and production costs.

16. Economic impact and improvement in competitive position

We have seen that the technology (one-colour display) sold today has primarily not been experiencing any basic development for the last 8-10 years, resulting in an increasing demand for a technology leap, e.g. multicolour displays. If Focon will not be able to offer multicolour displays in the near future, we fear that our market share will be decreasing.

Multicolour information systems will increase the geographical market of Focon.

Especially, we have within the last few years received inquiries for multicolour displays from present customers as well as from a number of new customers, e.g. in the Far East, where especially China, Japan and Australia are two very large and very interesting markets.

To improve the level of competition, the projected product is to include full coloured presentation of textual, graphical and animated information. The new display is designed to fulfil the increased request for extended lifetime of up to 30 years.

Economical impact for 3-coloured LED version

At the start of the AE , the financial basis for the project was based on a comparison between the present conventional driver electronics and the new ASIC.

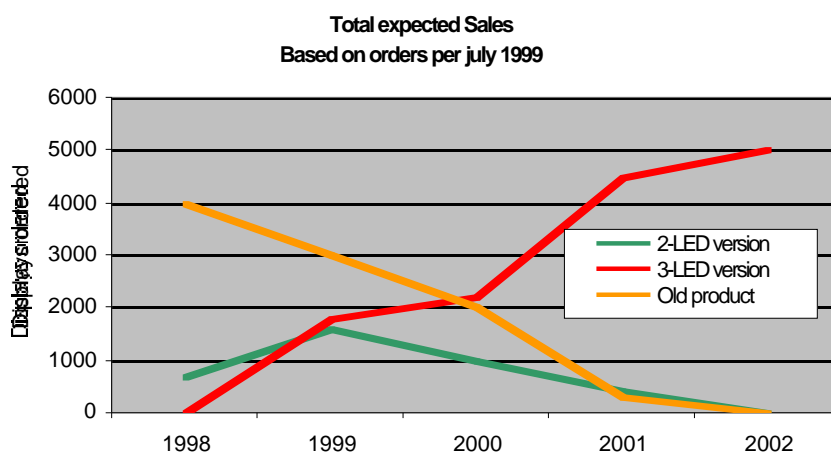
Break-even point for the ASIC based microelectronics with integrated LED matrix vs. conventional electronics LED's was calculated to be at approx. 4,000 modules, where it is estimated that each display will consist of 14 modules. Pricing of the ASIC based LED module including PCB, ASIC, discrete components and LED module is set to 25 Euro per unit. Pricing of discrete module including PCB, discrete components and LED's was 60 Euro per unit. The projected sales within the period 1997 to 2003 were estimated at 120,000 modules per year. This would have increased Focon's profit by approximately 650 KEuro per year. The payback period is expected to be 6-9 months. The ROI is calculated to 800% within 5 years. It's anticipated the next generation of the product will be introduced after 3 years of production.

Economical impact for 2-coloured LED version

During the experiment, the financial basis for the project changed as the development in costs of external components to the ASIC did not behave as predicted. The price of a 3-coloured LED was predicted to decrease with 40-60%. This decrease is now expected to take place in period 1999-2000. A contingency plan for a 2-coloured LED version was established. The additional product is still based on projected ASIC, but with only 2 LED applied per cell. The economical impact is briefly described below:

Break-even point for the ASIC based electronics with integrated LED matrix vs. conventional electronics LED's was calculated to be at approx. 5,000 modules, where it is estimated that each display will consist of 14 modules. Pricing of the ASIC based LED module including PCB, ASIC, discrete components and LED module is set to 20 Euro per unit. Pricing of discrete module including PCB, discrete components and LED's was 60 Euro per unit. The projected sales within the period 1997 to 2000 were estimated at 25,000 modules per year. (This version is only intended as introduction to market) This would have increased Focon's profit by approximately 395 KEuro per year. The ROI of this product is calculated to 250%. The payback period is expected to be 12 months.

The ordered number of modules to be produced is shown the table below



The most beneficial area for the new ASIC is multicolour displays, for which it was also developed.

REFFORMATVERBINDENThe availability and cost of three coloured LED has not - as expected - matured yet. It is expected to take another 1-2 years before better and less expensive solutions are available on the market for the blue LED. Until then the alternative is a display based on two-coloured (red and green) chips. Today, many LED suppliers offers two colour LED modules and Focon intend to produce a product using these units. With the added cost of industrialisation and optimisation of this additional product the total investment was about 200 KEuro.

Focon does not use a specific marketing. Today we have a number of positive references and new projects typically initiated on request of customers.

Despite of the expensive 3-chip LED technology our two major customers have shown high interest in this product. We are at present considering whether to manufacture a prototype display based on the same LED's as the developed demo display, which they will use to investigate the opportunities of the full colour LED display technology.

17. Summary of best practice and target audience

A number of items show its value as best practice during the experiment.

Firstly, the project team building with close contact to the project manager and the production was valuable in term of spreading the knowledge transferred technological as well as managerial.

Secondly, the workplan definition on especially the spilt of design work between the FU and subcontractor was good practice. Estimation of own capability and limitation was very valuable for the success of the experiment. I.e. the most demanding part of the project, the analogue design, was submitted to a subcontractor, while the FU concentrated on the digital part and gained knowledge on the technology.

Thirdly, we found best practice to set-up a risk analysis with its related contingency plan. I.e. what to do in case the designed circuit doesn't function.

The target audience for this experiment will be

- Producers of information systems
- Producers of standard components and LED-based displays
- Companies producing customised products.
- Companies with need of improving project management.
- Small sized companies unfamiliar to Mixed signal ASIC design
- Companies with need of improving functionality technologically and per space
- Companies with technological barriers towards ASIC
- Companies with existing use of subcontractors except for ASIC production