Development of a video scaling ASIC for use in multi-image displays.

FUSE DEMONSTRATOR DOCUMENT

AE 240

Application Experiment (AE) Abstract
This application experiment describes the first use of ASIC technology by an Electronics company. The experiment was performed successfully with a new and innovative gate array ASIC technology from Chip Express.

Beta electronics of Co. Meath, Ireland offers customers a complete design, prototyping and turn-key manufacturing service to industry with manufactured products extending from the farm to the high street business world. Beta has a product development division called Zandar Technologies whose role is to develop and market a suite of video display products for a number of markets in order to diversify Beta's business outside of contract manufacturing.

The AE involved the design of a low cost, gate array ASIC that re-sizes a video image in real time. The component accepts digital video input and produces a very high quality scaled version of the input image using a unique digital video processing algorithm. This forms the core of Zandar’s multi-image display products.

The cost of the AE was 189 kECU, of which 164 kECU was for this application experiment. The duration of the AE was planned at 12 months but actually lasted 16 months. The payback period is expected to be 2 years with a return on investment of 650KECU over a 4 year period.

The objective of the experiment is threefold: 1) To reduce the cost of Zandar’s products so as to enable exploitation of a wider market for low cost systems. 2) To develop the core of the next generation of multi-image display products which will contain greater flexibility, far higher image quality and functionality. These two objectives were to be met through migrating Zandar’s proprietary video image scaling technology, which is FPGA based, to an ASIC of greater complexity. 3) Finally, the strategic goal of acquiring ASIC design expertise has been achieved for the company to successfully enter into other markets with its future generation products.
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2. Company Size
Zandar Technologies is a business unit of Beta Electronics. It has about 500 KECS turnover, which corresponds to roughly 10% of Beta electronics. Beta Electronics comprises 45 employees. 39 of these employees are in the manufacturing services division while 6 employees are with the Zandar Technologies business unit. Most of the microelectronics expertise is located in the Zandar division which has a development team of 5 persons with over 40 years of collective design experience. Their experience is drawn from previous industrial and academic research backgrounds and covers many areas of electronics and information technology. All are qualified to University honours degree or masters level.

3. Company Business Description
Beta electronics was set up in Ashbourne, Co. Meath, Ireland in 1980 as a subsidiary of Warnants Holdings. Warnants is a group of Irish companies whose activities encompass the sale of capital plant and industrial equipment, sheet metal fabrication, electronic manufacturing and the distribution of sports and leisure goods. Today, Beta offers customers a complete design, prototyping and turn-key manufacturing service. The application of Beta's designed and manufactured products extends from the farm to the high street business world. The company has manufacturing capacity that encompasses semi automated and fully automated surface mount assembly lines as well as manual assembly of systems and low volume product runs.

In 1993, Beta set up a product development division called Zandar Technologies. Zandar's initial role was to develop a suite of multi-image display products for the cable television and broadcast industries and to diversify Beta's business outside of contract manufacturing. Beta markets the multi-image display products under the Zandar Technologies brand name in order to provide a unique market presence for its multi-image products.

Zandar Technologies is recognised as a leading supplier of high quality multi-image display products to the CATV and broadcast television industries with customers such as BT, Philips (NL), Nynex(USA), Samsung(USA), PictureTel(USA), Telefonica Sistemas de Satelites (Spain), MTV Europe, Canal+, Canal Satellite Digital(Spain), BBC, Astra Satellite.
Zandar currently sells the Q600 series Video Montage system. This is a 19 inch rack system that can generate a number of fixed multiple window displays for cable television mosaic channels as well as TV broadcast monitoring. More recently, Zandar launched a new series of PCI video cards called the OmniVideo. The series can accept between 2 and 16 video inputs which are displayed as video windows on a single monitor. They are a flexible solution allowing user resizing of windows and overlapping video windows similar to the functionality of windows on a computer display except that each window can contain live video. Most recently, Zandar has launched the OmniVMX system which is a replacement for the ageing Q600 series Video Montage which is no longer in production as it is at end of life. The OmniVMX is a 19inch rack system that is only 2U high but which has all of the functionality and flexibility of the OmniVideo series of PCI bus cards.
4. **Company Markets and competitive position at the start of the AE**

4.1 **Market Size & Growth**

The proliferation of video sources within CATV head ends, TV stations and satellite teleports points to the increased need to monitor multiple video pictures in an environment where monitor rack space is at a premium. Additionally, pay per view promotion and mosaic channel programme guides will become more widespread with the increased adoption of digital TV. Both of these observations point to an increasing demand for multi-image generation systems around which all of Zandar’s products are currently based.

At present there are seven Astra satellites, which broadcast more than 220 TV channels in Europe. With 11 satellites in orbit and a further six under construction, Eutelsat is the largest satellite operator in Europe. Compressed digital signals use up less bandwidth than conventional TV signals thus leaving surplus bandwidth. European broadcasters have opted for the multi-channel route, transmitting 6 or more channels using the same bandwidth now used for a single analogue channel.

Their increasing need for programming content to fill the channel capacity offered by digital and satellite transmissions is matched by a need to monitor these extra channels for video quality and content. This lends itself to cost effective monitoring using multi-image displays.

There are more than 11,000 cable TV headend systems in the U.S. (source Nielsen Media Research). Almost 75% of those systems have channel capacity for more than 30 channels. (source Warren Publishing). As the broadcast market converges towards digital video, there is a need to re-kit head-ends and studios for all aspects of TV distribution, transmission and, of course, monitoring.

These industry figures indicate a buoyant and growing market for Zandar product both in its traditional market segment of TV & Broadcast, but also in new business areas within TV & Broadcast and new markets such as A/V and multimedia.

4.2 **Competitive Position**

The Q600 16 input Video Montage currently costs 17,000 ECU end user price. With a manufacturing cost to end price ratio of approximately 3, there is only limited scope to reduce the price of the system to service broader markets. A high proportion of the cost is in the bill of materials for which semiconductors account for over 75%. In addition, the Q600 uses a simple form of video scaling which is effective for fixed size video windows but is far from ideal for arbitrary sized video windows. The existing product suffers from high manufacturing cost, limited picture quality and limited flexibility and analog inputs only. Core to these four properties is the video scaling engine used within the Q600. The more recent OmniVideo series of PCI cards has addressed some of these concerns by way of increased flexibility and lower manufacturing costs. However, the issue of average quality video scaling and analog inputs only gives the OmniVideo series in its current guise, a limited product life cycle. The AE was aimed at addressing all of the weaknesses to allow a future product to be very low cost, very flexible, allows digital video inputs, and to have the highest picture scaling quality on the market. This was achieved by developing a high performance video scaling ASIC that could be designed into the next generation of multi-image displays.

The factors that would have caused a decline in the company’s market are mainly due to increased competition. The market is growing for such systems and so is the competition. As an early entrant in the market for multi-image displays, Zandar must continue to innovate with a policy of providing more performance, flexibility and reliability at a lower cost. The start of the application experiment saw the company’s primary market in Cable TV where its Q600 series Video Montage was sold as a Cable TV Mosaic Channel. Since then, the TV broadcast monitoring monitor has now superseded the CATV as the main market for multi-image display sales.
5. **Product to be improved and its industrial sectors**

5.1 **Existing product**

The existing product available prior to the AE is a real time video multi-image display. The system comprises up to 16 video inputs where each video input is digitized, resized and positioned in full motion within a window for display to an output TV monitor. As a result, the output display is a ‘mosaic’ or montage of motion video pictures on a single display. The Q600 video montage product produces windows of fixed sizes.

Central to the generation of a multiple video window display is the video resizing electronics. With 16 video inputs, they are digitized and colour decoded prior to being fed to a video resizing circuit comprising an FPGA from Xilinx. The FPGAs perform horizontal and vertical filtering prior to decimation, which is the process of discarding pixels. The filtering is necessary in order to prevent aliasing picture artefacts in the re-sized picture. The Q600 uses a simple form of digital filtering using a maximum of 4 filter taps in each direction. The picture sizes are also restricted to integer sized images such as 1/4, 1/9, 1/16 sized images. The picture quality of this system is adequate. However, the FPGAs restrict the complexity of the filters and the cost rises sharply with FPGAs of higher gate counts. Essentially, the Q600 has a five chip solution for each video input to perform the functions of digitization, colour decoding and image resizing. With 16 video inputs, this translates to 80 integrated circuits to perform these functions per system including 16 FPGAs with external SRAM memory.

**OmniVideo Series of PCI multiple video window cards**

More recently during the AE, The OmniVideo series of PCI video cards were developed to overcome some of the limitations of the Q600. The OmniVideo series allows up to 16 video inputs to be displayed simultaneously on one monitor. Each of the video windows can be user sized and positioned anywhere on the display. Video windows can be allowed to overlap or be inserted within a larger picture as in ‘picture in picture’(PIP) displays. A proliferation of video ICs has eased the task of integrating more functionality onto a smaller PCB. Companies such as Philips and Brokmtree have integrated the digitizing, colour decoding and video re-sizing into a single chip solution. Taking advantage of this, Zandar designed the Bt829 into its OmniVideo series of PCI video cards. The Bt829 has the advantages of a single chip solution that accepts analog video and colour decodes and resizes the video to any picture size. Using an interpolator, it overcomes the restriction of fixed picture sizes which the Q600 was subject. The Bt829 and
other single chip solutions also have some significant disadvantages. Most of these solutions do not have a digital input where the digitizing stage can be bypassed. Furthermore, the video scaling quality, while better than the Q600, still leaves room for considerable improvement. The Bt829 picture re-sizing quality is only a slight improvement over the Q600. The OmniVideo series requires one FPGA, and two Bt829 ICs to generate 2 video windows. This results in a 24 chip solution for a 16 i/p system. The PCI video cards sometimes proved problematic at customer sites as each customer could have a different hardware platform running differing operating systems. As a result, the support side of a PCI card sale is quite high as distinct from a standalone system where the customer simply powersup a working system.

The block diagram below illustrates the various functions for each video input for the old, current and future products. The red outline shows what has been integrated into a single device.

5.2 Reasons to innovate
Zandar saw a number of limitations with the Q600 product. As an expensive machine to manufacture, it restricted the scope to reduce the price in order to sell it to a wider market. Competition was beginning to appear with favourable pricing which put Zandar under pressure to reduce costs. The inflexibility of the Q600 with its fixed picture sizes was restricting its deployment in other application areas.

At the time the proposal was submitted to FUSE, the choice of video ICs to perform video scaling was poor with the ICs being quite expensive. The greatest scope for cost reduction and increase in flexibility lay in replacing the expensive re-sizing FPGAs with ASICs that could perform a better job at a lower cost. It was necessary to analyse whether the NRE cost of an ASIC and the minimum quantities that must be ordered could offset the higher cost and inflexibility of the FPGA solution or indeed be more cost effective than 3rd party video scaling ICs that were available at the time.

Over the time leading up the commencement of the AE, a number of vendors brought new video scaling Integrated Circuits to the market with highly integrated functions such as video digitizing and colour decoding. These were also falling in cost so a re-appraisal was required of the impending project. The OmniVideo series of PCI cards were developed around these chip sets which appeared to provide the
flexibility that the Q600 lacked and a more cost effective solution than the FPGA based video resizing solution. It became clear however, that these new video chip sets had a number of shortcomings. Namely, they were developed for multi-media boards and as such were of limited picture quality. The video re-sizing used simple filtering algorithms to re-size the pictures and there were still visible artefacts on the scaled pictures. This has continued to be a limitation for the OmniVideo series of PCI cards. The lack of digital inputs to these highly integrated ICs also prevents a digital interface to be added to the system. This presented an argument that says that these large semiconductor companies are likely to produce the ‘ideal’ video re-sizing IC in the time frame of the proposed AE. However, the first user has a very clear understanding of market requirements in this area with a good knowledge and understanding of the application. There was a continuing need for a re-sizing IC that could overcome the shortcomings of the newly arrived video re-sizing ICs. The first user was confident that it could produce a leading edge device based on this knowledge and experience at the ‘finished product’ end of the industry.

Finally, the level of expectation amongst the potential customers has risen considerably and video quality and good quality image re-sizing has become a prime issue.

6. Description of the technical improvements
The product to be improved is a multi-image display system. Zandar currently has two product categories, those that are PC peripheral cards and stand alone systems. The future stand alone systems will be based around an embedded PC containing the same PC peripheral cards known as the OmniVideo series. The current OmniVideo series (designed during the AE) uses a chipset from Brooktree to perform video digitization, colour decoding and image re-sizing prior to being combined with 15 other identical circuits to produce the multi-image display output. The Q600 product (designed prior to the AE) uses FPGA ICs and external SRAM to perform the image re-sizing.

6.1 System level
The improved OmniVideo series product will have a number of considerable improvements over the existing analogue input product. Code named the OmniVideoDigital series, they are based around a gate array ASIC design. The main improvements are listed below:

- Very high quality output display using sophisticated image re-sizing algorithm
- The addition of serial digital inputs (SDI) or Firewire inputs
- Reduced cost due to ASIC economies of scale
- Scalable architecture allowing lengthened product life cycle
- Remove dependency on 3rd party scaling IC vendor
- All picture sizes generate same high quality output unlike existing OmniVideo series which generates best pictures only at integer scaling ratios of 1/4, 1/9, 1/16.

6.2 Component level
The gate array technology is based on a 0.8u CMOS process from chip express. The gate count is approximately 50,000 gates plus 24 Kbits of RAM. The overall device utilisation is approximately 60%. This compares with 2,000 gates in the re-sizing FPGA of the Q600 and an estimated 12K gates in the scaling core of the Bt829. This illustrates the sophisticated DSP algorithm that is utilised to effect very high quality image re-sizing.
• Image resizing using sub-pixel advanced interpolation (Accurate to 1/32 of a pixel width)
• 24 tap independent horizontal FIR filter for text book correct image resizing in the horizontal direction.
• 24 tap independent vertical FIR filter for text book correct image resizing in the vertical direction.
• Unique Filter coefficients calculated for each and every possible picture size
• Component cost < $8 in high volume
• The design is scalable and performance can be traded against cost.
• Foundry has an MOQ for as little as 3 devices allowing flexibility in manufacturing volumes.

The OmniVideoDigital system based around this ASIC will represent the next generation in multi-image display technology. The picture quality and performance improvement is the main advancement over its predecessors. The Zandar ASIC costs $25 in medium quantities going down to as low as $7 for high volume if it is migrated to the newer technology offered by the ASIC foundry. There are 16 devices in each system, so the accumulated cost savings are large for each system manufactured. The picture quality of the system is becoming more important for certain markets. Specifically, video monitoring in TV stations requires that the pictures are of the highest quality so that any picture defects are easily identified.

7. Choices and rationale for the selected technologies, tools and methodologies
Prior to the beginning of the AE, the overriding rationale was to reduce the cost of the semiconductor material in Zandar’s products. However, during the AE, the rationale behind the AE was changed reflecting the change in the market place. The increasing demand for very high quality video re-sizing that was not being adequately met by the semi-conductor companies. The focus changed from a purely cost saving exercise to one of both cost saving and quality/functional enhancements.

The First User investigated the possible alternatives to its current FPGA video re-sizing solution. They were DSP based solution, another FPGA solution, a third party video scaling IC solution or an in house ASIC development. The DSP solution was dismissed at the time due to cost and performance. The DSP offerings were only capable of basic video re-sizing in real time and even at that, would not compete favourably on cost. This left the other options which are considered further.

A comparison is made between the NRE costs of the ASIC development, the First User’s existing FPGA technology and readily available video scaler integrated circuits. This is illustrated in the table 1. The figures in brackets indicate the actual costs as opposed to the originally forecast costs. This analysis was based solely on cost savings of material and did not reflect the likely increase in system sales that would result from a product that offered considerably improved picture quality and functional enhancements.
Table 2. illustrates the worst case, projected case and best case sales forecasts and their effect on the comparative costs of the ASIC, FPGA and the third party video scalers with an FPGA controller. It is based on sales of the first user's multi-image boards and systems. The figures in brackets are the actual figures or costs that have changed over the course of the application experiment.

<table>
<thead>
<tr>
<th>Table 1a</th>
<th>NRE cost of ASIC in ECU</th>
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<tbody>
<tr>
<td><strong>Planned</strong></td>
<td><strong>(Actual)</strong></td>
</tr>
<tr>
<td>First users marginal costs</td>
<td>98K (125K)</td>
</tr>
<tr>
<td>Subcontractors costs</td>
<td>65.5K (64K)</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>163.5K (189K)</td>
</tr>
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<table>
<thead>
<tr>
<th>Table 1b</th>
<th>Alternative technology NRE</th>
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<tbody>
<tr>
<td><strong>FPGA</strong></td>
<td>30KECU</td>
</tr>
<tr>
<td><strong>Third Party Video Scalers (TPVS)</strong></td>
<td>10KECU with FPGA controller</td>
</tr>
</tbody>
</table>

Table 2a
Cost comparison of the three technologies in ECUs for 5000 video scalers
Based on worst case sales forecast of 830 multi-image systems over product life cycle.

<table>
<thead>
<tr>
<th>Unit</th>
<th>ASIC cost (5000)</th>
<th>21 (17)</th>
<th>NRE 163.5K (189K)</th>
<th>Total Cost 268,500 (274,000)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>FPGA cost (5000)</td>
<td>100 (60)</td>
<td>NRE 30,000</td>
<td>Total Cost 530,000 (330,000)</td>
</tr>
<tr>
<td>Unit</td>
<td>TPVS cost (5000)</td>
<td>50 (35)</td>
<td>NRE 10,000</td>
<td>Total Cost 260,000 (185,000)</td>
</tr>
</tbody>
</table>

Table 2b
Original Forecast at beginning of AE for ASIC quantities necessary to breakeven with TPVS option.

<table>
<thead>
<tr>
<th>Unit</th>
<th>ASIC cost (5300)</th>
<th>21</th>
<th>NRE 163.5K</th>
<th>Total Cost 274,800</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>FPGA cost (5300)</td>
<td>100</td>
<td>NRE 30,000</td>
<td>Total Cost 560,000</td>
</tr>
<tr>
<td>Unit</td>
<td>TPVS cost (5300)</td>
<td>50</td>
<td>NRE 10,000</td>
<td>Total Cost 275,000</td>
</tr>
</tbody>
</table>

Actual quantities at end of AE for ASIC to breakeven with TPVS option.

<table>
<thead>
<tr>
<th>Unit</th>
<th>ASIC cost (10,000*) (17)</th>
<th>NRE (189K)</th>
<th>Total Cost 359,000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>FPGA cost (10,000*)(60)</td>
<td>NRE 30,000</td>
<td>Total Cost 630,000</td>
</tr>
<tr>
<td>Unit</td>
<td>TPVS cost (10,000*)(35)</td>
<td>NRE 10,000</td>
<td>Total Cost 360,000</td>
</tr>
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</table>

*Assumes no price break at 10,000.

Table 2c
Cost comparison of the three technologies in ECUs for 10,000 video scalers
Based on sales forecast of 1600 multi-image systems over product lifecycle and price breaks at 10,000 units

<table>
<thead>
<tr>
<th>Unit</th>
<th>ASIC cost (10,000)</th>
<th>17(11)</th>
<th>NRE 163.5K (189K)</th>
<th>Total Cost 333,500 (299,000)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>FPGA cost (10,000)</td>
<td>90(40)</td>
<td>NRE 30,000</td>
<td>Total Cost 930,000 (430,000)</td>
</tr>
<tr>
<td>Unit</td>
<td>TPVS cost (10,000)</td>
<td>40(30)</td>
<td>NRE 10,000</td>
<td>Total Cost 410,000 (310,000)</td>
</tr>
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</table>
It can be seen from Table 2.b that sales of 6,500 ASICs whether sold as separate entities or integrated on the first user's multi-image display systems was at the break even point compared with using third party video scalers with an accompanying FPGA controller. This was the forecast at the beginning of the AE. However, unexpected price reductions with the other options pushed the breakeven point up to 10,000 units. This was over a period of 2 years. The multi-image display systems contain one ASIC per picture such that a 16 picture system requires 16 ASICs.

The first user forecast that sales of at least 800 systems containing an average of 6 ASICs p.a. could be achieved while the product life-span was projected to be 4 years. In addition, the ASIC would be incorporated into the updated Q600 series known as the OmniVideo Digital series and which will continue to sell in low volumes at high margin. With a projected manufacturing cost of 2KECU, this represents a reduction to 40% on the present Q600 series manufacturing cost. As a result, the first user should be able to either increase its margin or reduce its end price to boost sales of its multi-image display systems.

Below is a description of the Choices and rationale for the selected technologies, tools and methodologies at the beginning of the application experiment. The following section then describes the changes that evolved during the experiment as the First User reacted to changing conditions and increased awareness of the subtleties of ASIC design.

7.1 At the beginning of the AE

In moving from FPGA design to ASIC design, the choice of design entry tools are either schematic capture or VHDL. The preferred choice is VHDL as this will not bind the first user to a vendor specific technology. It is planned to acquire, learn and implement the ASIC design in VHDL. The design tools will be PC based so as to minimise cost. From this, a simulation model can be produced to verify the design and to produce a test bench. A set of VHDL to FPGA synthesis tools such as those provided by Exemplar will also be acquired so that the circuits can be physically verified. It is important that the circuit can be emulated on a small number of FPGAs as small incremental design changes may be necessary as a result of discovering visual problems on the emulated system. These are potential problems that would not necessarily be apparent on examining simulation data. An FPGA version of the design will deliver an early sample of ASIC functionality on the evaluation board. The subcontractor that synthesizes the ASIC design, will also liaise with the design team in order to provide a set of guidelines to ensure a consistent design flow and a smooth migration to the ASIC synthesis.

The other choice that was made was to what degree should the ASIC design be sub-contracted. At one extreme, the first user could have performed all of the design work and provided the final gate array design to the foundry for fabrication. This would have been extremely expensive, as the proper CAD tools such as Synopsys are prohibitively expensive and the first user does not have the capability of acquiring this degree of skill in a reasonable time frame. At the other extreme, the first user could have sub-contracted out the entire design. This was not an attractive option since little would be learned; the first user would have little or no control over the process and the first user’s existing design capability would have been wasted. The third and best choice is to perform as much of the design work in-house as is feasible and to sub-contract the actual

<table>
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<th>Table 2.d</th>
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<tbody>
<tr>
<td>Cost comparison of the three in technologies in ECUs for 25,000 video scalers. Based on best case sales forecast of 4,100 multi-image systems over product life cycle</td>
</tr>
<tr>
<td>Unit</td>
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<tr>
<td>Unit</td>
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<tr>
<td>Unit</td>
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*Based on migration to 0.25u technology offered by Chip Express
silicon compilation and fabrication to two sub-contractors. With this scheme, sub-contractor2 is independent of the foundry (sub-contractor3) and will perform the synthesis of the ASIC to the foundry’s gate level net list using foundry supplied synthesis libraries. The second sub-contractor will manufacture the ASIC. Having two sub-contractors is advantageous in that the first user will retain control over the design and moving to a second manufacturing source in the future would not pose a problem.

There are a range of fabrication technology choices available for the experiment. The three broad categories are gate array, standard cell and full custom. The full custom approach is suited to very high volume and in many cases high complexity. This is not an option for the ASIC since the cost of design would be prohibitive and the manufacturing volume could not be justified. The choice of gate array technology most closely match the first user’s requirements and will result in a low cost device at medium volumes. The resulting low NRE cost and the time taken to generate a prototype makes gate array technology attractive. As the device is unlikely to exceed 60,000 gates in complexity, there are many vendors who can offer gate array implementations to fit the size of the design.

The chosen vendor produces a coarse grained gate array architecture with a dedicated RAM area on the die. This is most suited to the ASIC design in question and as a significant portion of the design requires dual RAM. The component will be tested by subcontractor3. The first user with the assistance of subcontractor 2 will develop the test vectors to cover all normal operations of the device. This will be the simulation data that completely describes the normal behaviour of the ASIC and hence provides the benchmark against which the sub-contractors guarantee the proper implementation of the design.

The ASIC will be register rich in design and this will help the test-ability of the device after fabrication. It is hoped to design in scan path test structures in order to reduce the number of test pattern vectors to be generated as well as giving a sufficient test coverage. JTAG boundary scan will be supported and this should allow board and system level testing after manufacturing.

7.2 At the end of the AE
The implementation of the planned methodology had only one significant change. That was the use of FPGAs to emulate the design prior to migration to an ASIC. A number of difficulties were encountered in synthesizing the design of this complexity to one or two FPGAs. With all of the surrounding logic, a trial synthesis to a Chip Express CX2081 gate array resulted in 16,800 logic modules. This meant that the design would not fit into an XC4062 FPGA. Only portions of the design could be loaded into the FPGA at a time. This made the FPGA far less attractive as a verification tool. Additionally, the speed of the FPGAs were insufficient to enable the design to operate at normal speed (13.5MHz). A trial synthesis to a Chip Express CX2050 gate array reported delay paths of 115ns, this suggests that there would be significant problems operating the FPGA at speed. Finally, the FPGA synthesis, place and routing CPU time took 4 hours for each iteration. Even minor changes to the design would take this long so it was felt that an inordinate amount of time would be spent waiting for the CPU to produce a design iteration. This was based on a Pentium Pro 200MHz PC which was the fastest machine at the time. A decision was taken that RTL simulation was the best option for verifying the design instead of FPGA emulation. In taking this decision, it was necessary to devise a test methodology that would speed up the verification procedure for the design. The revised verification methodology involved writing a C program to convert an image bitmap into a file of test vectors that would stimulate the VHDL model of the complete ASIC. The output of the simulator was written to a testbench file that contained the original stimulus and the captured outputs. A second C program was developed to read the output vector file and convert it back into a bitmap. This meant that the ASIC could be quickly verified by simulating the scaling of images viewing the resulting output image as a bitmap. While only one frame of video would be simulated at a time, this was considerably faster than synthesizing, placing and routing every minor design change into an FPGA to view the results. In line with this new methodology, the stimulus vector file applied signals to the ASIC external package pins only and not to any internal signal nodes. This was considered important to ensure accuracy of simulation and to get as close as possible to accurate emulation of the ASIC.
The issues outlined above account for the largest deviation from the technical annex. Specifically, WP5 Task 3: Functional Testing was changed to the Software I/O Interface to the Model Tech VHDL simulator to allow different images to be input to the RTL model and output images to be viewed on the monitor. This replaced the multiple FPGA target which was specified for functional testing. The time taken to simulate and generate an output image was 10 minutes. This allowed many design iterations and changes to be quickly made and verified before freezing the VHDL code. Once the VHDL model was locked and all known bugs were removed, multiple bitmaps were fed into the simulation at a number of key scaling ratios. The device was put into every available mode of operation and simulated. The complete test harness took 4 hours of RTL simulation with typically 50 to 60 bitmaps generated and examined. This was much faster than painstakingly examining the video output data as waveforms. Special test images were devised to show any image defects. This revised verification methodology was considered to be more rigorous than the FPGA emulation technique. Finally, a testbench for the subcontractor was devised. This contained 73,000 test vectors with expected outputs and consisted of scaling multiple bitmaps to multiple resolutions in every mode of operation. The fault coverage achieved with this test harness was 90% without any ATPG. The subcontractor then added a large XOR tree to many of the internal nodes and brought it out to a single test observation pin. This increased the overall fault coverage to 95%. The testbench was the model that was used by the sub-contractor that precisely defined the ASIC functionality. Any deviation from the testbench after synthesis, placement and routing would have to be authorised by the First User if it did not affect real operation of the device or would have to be corrected in the event that it did affect real operation of the device. In practice, a number of issues became apparent with gate level simulation. This related primarily to clock skew and in particular to initialisation of the device with asynchronous I2C signals. The testbench was modified a number of times to achieve consistent results and to make the device testable by the foundry’s production tester.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

The Zandar Technologies division of Beta Electronics Ltd. has a development team of 5 persons with over 30 years of collective design experience. Their experience is drawn from previous industrial and academic research backgrounds and covers many areas of electronics and computing. More specifically, the team had technical design experience in the following areas: high speed board digital design, FPGA design up to 10K gates, Video and Image processing algorithms, multi-layer PCB design, schematic entry, simulation, microprocessor, analog and digital video technical standards, C and C++ programming.

The skills that the personnel lacked at the beginning of the AE were mostly technical. None of the team had worked on the design of a complex ASIC. The main technical shortcomings were lack of VHDL knowledge, no experience of ASIC design flows or verification methodologies, no experience in devising an ASIC specification.

The managerial shortcomings and lack of skills are mainly to do with lack of experience in managing an ASIC project as well as multiple sub-contractors. The interface and precise work to be defined for the subcontractors was a skill that the first user lacked. There was also lack of knowledge in selecting suitable CAD tools.

The personnel involved have considerable experience in the design of video and DSP systems. Below is a brief summary of the personnel involved.

Killian O’Sullivan (KOS) BAI (1986), MSc.
As project manager for Zandar, he managed the development of the ASIC and was responsible for the generation of reports and the scheduling of the various tasks. He used his video DSP and FPGA design experience to generate the specification and was responsible for test and verification methodology.

Gaybriel McMorrow (GM) BAI (1985), MSc.
Gaybriel was responsible for most of the VHDL coding of the design as well as. He documented the design at that level and undertook the design of the test evaluation board.

Arthur McMahon (AM) BSc. Eng (1987)
With experience in DSP systems, software and hardware, Arthur was part responsible for C code simulation of the scaling algorithms prior to their coding in VHDL.

9. Workplan and Rationale
The summarised workplan is set out. It was devised 6 months prior to commencement of the application experiment. The deviations from the workplan are set out in italicised paragraphs at the end of each section for comparison purposes.

9.1. Workpackage 1, Management

The management of the application experiment will range from the coordination of the project to the production of a detailed management plan to the liaison with the TTN and the generation of progress reports. The first user will set up experiment management schedules, coordinate the execution of the tasks and to generate periodical reports while Sub-contractor 1 will assist with the management of the FPGA to ASIC migration procedure.

9.1.1. Task 1: Project Management
The first user will develop a detailed management plan for the experiment and produce a design flow. It is at this stage that a rigorous design methodology will be put in place to facilitate a smooth design flow. Sub-contractor 1 will provide consultancy on the best approach to the flow from the FPGA based design to the ASIC. The first user will be responsible for managing the experiment.

Deviation from plan at end of AE
The flow from FPGA was altered during the experiment when it became apparent that implementing the design in FPGA would present considerable difficulties due to the speed and complexity of the design. Instead, the use of extensive simulation and a software front end to the simulator was developed.

9.1.2. Task 2: Dissemination
The first user will supply FUSE and the TTN with a set of public domain documentation describing the experiment and thereby illustrating the technological and economic benefits that result from the first use of technologies. The first user will seek to publish its FPGA to ASIC migration in a trade. The first user will speak at an open day in Ireland to be organised by the TTN and relate the experience of applying and participating in the experiment.

9.1.3. Task 3: Reporting
The first user will create and supply an up to date report on the status of the experiment to the TTN, the sub contractors and the CEC. There will also be a monthly meeting with the sub-contractors to review progress.
Deviation from plan at end of AE
The only minor deviation from this was the lack of a formal monthly meeting with the sub-contractors. Instead, the first user was continuously updated on progress and developments.

9.2. Workpackage 2, Specification

The first user will produce a precise specification down to a level of detail that enables the design team to implement the initial FPGA followed by the sub-contractor migrating the design to the ASIC.

9.2.1. Task 1: Functional Specification of system

The first user will specify the type of systems that will contain the component to be designed and hence determine the capabilities of the component. Included within this task is an evaluation of a range of scaling algorithms which produce the best result for a given ‘gate budget’.

Deviation from plan at end of AE
The gate budget was not accurately estimated. When the first user performed FPGA synthesis to a 60,000 FPGA with the original specification, it emerged that only half of the design would fit. This implied that the design was actually 50,000 gates approximately. This suggested that the claimed gate count of the FPGA was somewhat exaggerated and the so-called 60,000 gate FPGA was closer to a 30,000 gate device. The claim is based on a 100% utilisation of specific logic structures with a coarse grained architecture. In practice, utilisation cannot be high where there are dedicated logic functions such as flipflops, multiplexers, carry look-ahead logic etc. The first user discovered this after trial synthesis to the target gate array.

9.2.2. Task 2: System specification of component

This task will generate a system level specification sufficient to design the component into a target system. The specification includes a description of all external interfaces such as pin descriptions and functionality, timing, modes of operation, packaging etc.

Deviation from plan at end of AE
The ASIC was targeted to a 100 pin PQFP package based around Chip Express’s CX2050 gate array. However, it was only after the VHDL design was complete that it was discovered that there were speed and memory implementation problems such that a newer gate array technology had to be selected, namely the CX2081. This also meant that the package had to be changed to a 120 pin PQFP to accommodate the larger die.

9.2.3. Task 3: Technical specification of component

This task will generate a specification that describes the internal functions of the component to a low level of detail. The component will be partitioned into hierarchical blocks and each block will be precisely defined in terms of its inputs and required outputs. The specification will be of such detail as to allow a VHDL designer to code the design efficiently.

Deviation from plan at end of AE
The technical specification of the component changed considerably due to technology constraints. The main change was the addition of a memory management unit that was not foreseen. The level of detail in this specification was not good enough to allow a VHDL designer to implement in VHDL without a broader knowledge of the design. Many minor design issues became apparent during the VHDL coding phase and as such would suggest that the specification was an evolving document that became more refined as the design process continued.
9.3. Workpackage 3, Training

This workpackage provides the means for acquiring the expertise to successfully complete the experiment. It will provide training to personnel at technical levels. The training will be provided by sub-contractor 1 who have expertise in the relevant area. The CAD training will consist of attendance at a VHDL course. The course will enable entry of the ASIC design in VHDL as opposed to more traditional schematic entry techniques. This will result in a portable design that is more easily migrated to future alternative ASIC technologies.

Deviation from plan at end of AE

The VHDL training course started later than originally planned.

9.4. Workpackage 4, Design

The ASIC will be designed using VHDL entry and functionally simulated. The design will then be ported to a large FPGA to physically verify the functionality and to ensure that there are no outstanding design issues that may have been overlooked. The migration process will then commence to the target gate array. The migration of the FPGA based design to the ASIC will be performed by the sub-contractor. The first user will undertake the design of the ASIC at RTL level while Sub-contractor 2 will synthesize the VHDL model to target gate array and verify with simulation.

9.4.1. Task 1: System Level Design

An RTL description of the design will be produced in VHDL based on the specification. The behavior of the model will be functionally verified through simulation. The VHDL code will be partitioned into a number of functional blocks and modified as necessary to generate a multiple FPGA target. The FPGA target will emulate the design over one or more LCAs with external memory. In addition, an evaluation PCB will be designed that accommodates both the multiple FPGA target as well as up to two ASICs.

Deviation from plan at end of AE

The time taken to perform the task was severely underestimated. This was first of all due to the enhanced scaling algorithm that was decided upon during the specification phase and was driven by changing market and commercial factors. As a result, there were many difficulties in trying to squeeze the design into a single very large FPGA. Much time was spent looping back to the specification phase when it became apparent that the design would either not fit or was too slow. When the VHDL was sent to the sub-contractor for trial synthesis, this raised a number of technology related issues such as the memory partitioning in the ASIC and the speed of the system. While the original scaling algorithm was modeled in C, the translation to VHDL produced discrepancies between the C model and the VHDL model. When the design was pruned, this meant making changes to the scaling algorithm where issues such as bus width reduction and the effects of quantizing coefficients had to be investigate. The overall design flow became an iterative process rather than a one way flow.

This task required 352 Man days which far exceeds the original estimate of 230 man days.

9.4.2. Task 2: Subsystem Level Design

The physically verified VHDL design that was implemented over multiple FPGAs must then be recombined into a unified model. Following successful modification and simulation of the design, the VHDL code will be sent to the subcontractor for synthesis of the VHDL using the ASIC synthesis library. The test bench code will then be produced to enable verification of the design and test vectors will be produced to enable testing of the ASIC prototypes. The finalised design will be submitted to the ASIC foundry for prototype production.

Deviation from plan at end of AE

The design flow had changed considerably from the original work plan. The assumption in the original plan was to complete the design in a multiple FPGA target and to port it to the ASIC. The first change or deviation
was to try and target the entire design into the largest available FPGA. This would have given a unified model thereby reducing the man effort for the task. The next change to the plan involved skipping the FPGA phase altogether and targeting the ASIC directly. This rendered the task largely obsolete but placed a much larger burden on the functional testing and verification tasks.

9.5.Workpackage 5, Evaluation

ASIC silicon samples will be produced and populated onto the evaluation card. The evaluation video card will be designed to test and qualitatively evaluate the performance of the prototype. On successful evaluation, the prototype card with the ASIC will serve as a demonstration of the ASIC and will undergo limited field testing. Sub-Contractor 3 will produce and functionally test the gate array prototypes with supplied test vectors and the First user will populate the ASIC onto the evaluation card and test performance.

9.5.1. Task 1: Prototype Production

The ASIC gate array will be produced by the foundry subcontractor. In conjunction with the subcontractor, the VHDL design will have been compiled to a gate level netlist for the foundry’s gate array technology. It is expected that the gate array chosen will be based on 0.8 micron technology. The evaluation card will have both analog and digital video outputs to enable display of the ASIC output on a range of display devices. Two prototypes will be produced so as to provide a backup in the event of loss or damage.

9.5.2. Task 2 & 3: Test setup

The test setup will require the provision of a range of test equipment to test the ASIC at a number of levels. Firstly, the device must be characterised in order to verify that it operates over a range of supply voltages, temperatures and clock frequencies. A high quality video source will be used to input test pictures to the ASIC while the output will be measured on a waveform monitor and high quality CRT monitor.

9.5.3. Task 3: Functional testing

This task will consist of quantitatively testing the performance of the VHDL based model before committing the design to the ASIC. This will be done by porting the design initially to the multiple FPGA target and loading the design into the FPGA section of the evaluation card. A set of test images will be input to the video scaler and the outputs measured on a waveform monitor. Upon satisfactory completion of this task, the migration process to the ASIC will then commence.

Deviation from plan at end of AE
This task was completely replaced by an alternative functional test and verification methodology. There was no multiple FPGA target implemented for functional testing. Instead a software front end was developed in C to interface with the VHDL simulator. This front end converted bitmaps into simulated video test vectors that were used to stimulate the VHDL model of the ASIC. The output of the simulator was written to a vector file and the captured data was converted back to a bitmap for visual evaluation. This method was very effective and saved time over multiple design iterations that would have to be performed on the FPGA based system. The ideal approach would have been to conduct this methodology and then to perform a final verification on an FPGA target. However, time and resources did not permit both methods to be followed. The rigorous simulation with the front ends also assisted in the generation of a test bench with which the sub-contractor could perform tests on the post synthesis and layout of the design.
9.5.4. Task 4 & 5: Prototype testing & Field Testing

The evaluation card will contain at least one ASIC which will be fully tested. First of all a functional test must be performed whereby the ASIC is put into all of its modes of operation. This is followed by performance testing where the quality of the output is assessed and measured. Comparisons can be made with the outputs of the functional test task. Device characterisation will then be performed to establish the tolerance of the component for a range of supply voltages and clock speeds.

The evaluation card will be made available to a select number of customers who are in a position to assess the performance and features of the ASIC. While the end system is not being evaluated in this task, it allows the company to receive positive feedback, criticism and suggestions based on external assessment of the product. Any critical suggestions can then be assessed and considered for future improvements in the ASIC design.

9.6. Overview of Planning

\[ x = \text{planned activity} \quad A = \text{actual activity over AE} \]

<table>
<thead>
<tr>
<th>Activities</th>
<th>Month</th>
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<tr>
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<tr>
<td>Task 2</td>
<td>A</td>
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<td>Task 3</td>
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| Workpackage 2 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| Task 1     | X A   | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 2     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 3     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |

| Workpackage 3 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| Task 1     | X A   | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 2     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 3     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |

| Workpackage 4 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| Task 1     | X A   | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 2     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 3     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 4     | X A   | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 5     | A A   | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |

| Workpackage 5 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| Task 1     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 2     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 3     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 4     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |
| Task 5     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     | A     |

**Summary**

It can be seen from the overview of planning, the divergence between the planned activity and the actual activity. The pattern shows that many of the tasks did not commence until after WP4 task 1 was complete. This is due in part to the under estimation of the work required and the difficulties encountered during the design implementation phase. Most of the manpower was allocated to completing this critical task. However, once complete, the other tasks were performed within the estimated man effort.

9.7 Actual Effort Breakdown between FU and Sub-contractors.

Effort expressed in man days or costs in kECU

<table>
<thead>
<tr>
<th>Activities</th>
<th>First User</th>
<th>Sub-Contractor1</th>
<th>Sub-Contractor2</th>
<th>Sub-Contractor3</th>
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<td>45</td>
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</table>
10. Subcontractor Information

The first user, having taken the decision to use three sub-contractors to provide design, training and production services went about contacting a number of potential sub-contractors. The most important was sub-contractor 2 who would be performing the synthesis, simulation and final verification of the design. A request for tender was sent out to 4 potential companies who could fulfil this role. Three of the four companies proposed solutions and in all cases they would liaise with the foundry to manage production of the silicon prototypes. The factors that contributed to the selection of the sub-contractor were, fixed consultancy cost, foundry NRE cost, most suitable technology, MOQ and gate array pricing structure. The successful company satisfied the first user under all of these categories and was the best candidate under most of them. In addition, the successful sub-contractor spent much effort in understanding the nature and scale of the project and as a result was in the best position to quantify the work involved and hence deliver the most competitive fixed quotation. Sub-contractor 3 (the foundry) had a good fit in terms of the gate array technology available with important technical features such as embedded RAM, flexible manufacturing with competitive pricing on low volumes. Sub-contractor 1 provided training services as a well recognised center of learning in the field of IC design.

10.1 Subcontractor 1 – National Microelectronics Research Centre

**Company size**
200 employees

**Company business description**
NMRC offers a full range of services to industry and is involved in leading edge electronics research covering several areas such as IC process, packaging devices and basic materials research. The centre has two semiconductor fabrication facilities which process both Silicon and Gallium Arsenide.

**Company’s market(s)**
Microelectronics consultancy including IC design, CAD training, materials research, education, post graduate research, etc.

**Expertise of the company**
The NMRC has expertise in most areas of microelectronics including CAD, IC design, IC packaging, materials research, test and characterisation.

**Experience of the company**
NMRC was founded in 1981 and has 15 years experience in microelectronics research. Most of NMRC staff hold higher degrees or doctorates in relevant disciplines. The centre has an impressive list of international clients for which it has carried out research and development consultancy.

**Work Performed for First user**
The NMRC provided the VHDL training course to the first user. The course was 3 days in duration and was tailored to the first user’s requirements. The course was specifically aimed as an introductory course to VHDL since the first user had no previous experience with VHDL based design. The course did not include IC design but was strictly confined to VHDL based design and good practice.
10.2 Subcontractor 2 – Excel Consultants

Company size - 4 employees

Company business description
Excel Consultants offer a range of consultancy services for IC design to industry. Ranging from specification to full blown design, EXCEL can tailor their service to the needs of the customer. The company is well equipped with the latest in CAD tools and TEST facilities.

Company’s market(s) - IC semiconductor design consultancy

Expertise of the company - IC design, Digital, VHDL, Simulation, Test Vector generation.

Experience of the company
Excel have provided design services to a number of clients. They are approved by Chip Express to supply technical support and design services to companies using Chip Express gate arrays.

Work Performed for First user
Excel consultants provided design consultancy services to the first user. They were the most important subcontractor as they were charged with the task of taking the first user’s VHDL code and test bench and providing a fully verified gate level net list to the foundry. Chip Express performed the layout and routing of the design and returned post layout timing information to Excel. Excel then performed post layout timing verification of the design before signing off. There were a number of technology specific issues that were handled by Excel. The first user had provided a high level RTL description of the ASIC but Excel had to convert this to a working gate array. Issues such as the clock tree structure, fanout, power dissipation, scan path insertion, fault simulation and other IC design specific expertise were all handled by Excel.

Liasing with Excel was a surprisingly simple process. They provided a fixed cost quote for the Job. This was arrived at in a number of stages. Firstly, the first user estimated the complexity of the design with approximate calculations and identified a target gate array. Excel then gave a guideline quotation based on a man effort estimate. The first user generated the VHDL and sent an early draft of the code to Excel. They then performed a trial synthesis of the design and spent some time examining the design to see if good coding practices were used. Based on this information they supplied a final fixed quote for the design stipulating that it was based on the VHDL code supplied. They allowed quite an amount of leeway in terms of changes that were made to the VHDL without revising the quote. The first user ran into quite a few problems with the design but Excel provided much guidance in conjunction with Chip Express (The 3rd sub contractor). The testbench supplied by the first user was considered by Excel to have very high fault coverage and was supplied in their ‘ideal’ format. They had to perform minimal translation of the vector files and as such had a fully packaged design with a working test harness.

By the end of the experiment, Excel had underestimated the work involved in converting the VHDL into a gate array design. Their fixed quote meant that this did not affect the budget of the first user. Excel Consultants is based in the U.K. while the first user is based in Dublin, Ireland. This geographical difference had no negative impact on the work performed. All of the interaction was by either telephone or EMAIL. All of the design and technical information was exchanged using EMAIL. Excel handled most of the interaction with Chip Express. Any technology specific queries from Chip Express were handled directly by Excel and the communication was copied to the first user. This was a very efficient way of managing the sub- contractors. Commercial concerns and final sign off procedures were performed by the first user. There was no written contract specifically between the first user and Excel consultants. Instead, there were terms and conditions set down by Excel which the first user implicitly agreed to in retaining Excel as design consultants.
Payments were made on a phased basis according to agreed deliverables with the final payment made after final sign off of the design.

10.3 Subcontractor 3 – Chip Express

Company size  > 100 Employees with turnover >$18 in 1995

Company business description
Chip Express are a provider of fast turn around gate array solutions aimed at the low to medium volume ASIC market. The company uses a one mask wafer level process on a 0.8 micron 3 layer metal gate array technology to produce a low NRE medium volume product. The company has established a niche market for companies with volume requirements between 1K and 100 K pieces per anum. Using a laser machining process, chip express can produce one off prototypes in as little as three days for design testing and field trials prior to production. The one mask wafer level process allows for low to medium quantities (100 to 3K pieces) to be produced. For medium to high volume applications (>3K pieces) Chip Express offer a ‘Hard Array’ migration path with no re-engineering requirement on the part of the customer. The company will shrink the design down to a smaller die size for a small NRE fee and hence the unit cost is reduced.

Company’s market(s)
The company’s markets are in ASIC gate array production for telecommunications, multimedia, Instrumentation and computer applications.

Expertise of the company
The company has expertise in taking a gate level net list and converting it to their gate array architecture. They can manufacture one off prototypes using their proprietary laser machining process and they also can test the devices using customer supplied test vectors.

Experience of the company
Founded in 1989. Chip Express have been producing gate arrays for 7 years. They have an impressive customer list including Hewlett Packard, IBM, Philips etc.

Work Performed for First user

Chip Express are the gate array foundry for the first user. They took the gate level netlist supplied by Excel Consultants and performed IC layout of the design. They then extracted back annotated timing information from the post layout design and returned the data to Excel. They then waited for final sign off of the fully verified design and manufactured 2 prototypes. Both prototypes were tested using the vectors ultimately supplied by the first user. Excel had made some modifications in order to increase the test coverage to 95%. Finally, the prototypes were sent to the first user for evaluation and testing. Chip Express charged a fixed NRE fee for the provision of the prototypes. There is no further NRE fee for production runs unless the First User either changes the design or migrates to another gate array technology offered by Chip Express.

Chip Express dealt with the first user under its terms and conditions of sale. They charge a fixed rate dependant on the size of the design. The first user had to complete a design interface form which includes an authorisation to proceed with manufacturing after the design has been signed off at various stages. NRE had to be prepaid before final layout was performed by the sub-contractor.
Summary
Working with the subcontractors turned out to be a very straightforward process. The interfaces and the work to be performed was clearly defined. This was because the first user supplied a VHDL model and a working test harness that defined the behavior of the working model. The test harness was crucial in identifying that the work was performed as agreed. The fixed cost basis for performing the work by the sub-contractors assured the first user that this element of the project would stay within the planned budget. Contingencies for delayed work or work incorrectly performed were lacking in this arrangement. The first user had only a financial lever in terms of paying for work that was verifiably correct. However, in this instance, the sub-contractors performed very well. There was definitely a strong element of ‘good will’ between the parties with the common aim of performing the work successfully.

11. Barriers perceived by the company in the first use of the AE technology
The first user has encountered many barriers to adopting the new technologies that were utilised in this application experiment. These are summarised below under different headings.

11.1 Knowledge Barriers
The first user had previous experience with FPGA design and could clearly see the advantages of FPGAs in many products. The first user was accustomed to using schematic entry graphical tools and was comfortable with their use. The merits of VHDL seemed to escape the first user at the time since going from a graphical based representation of a complex circuit to a textual based representation seemed almost to be a backward step. It was not until some knowledge about VHDL was gained, that the first user realised the true power of hardware description languages and their flexibility. The final aspect of the knowledge barrier was how to acquire the necessary information. This related to what software design tools were available, what gate array foundry’s were suitable, how much would such a venture cost?

11.2 Cultural and inertia barriers (psychology)
Like any other aspect of life, adopting new ideas and procedures frequently meet with resistance to change. In this instance, there was a psychological barrier to adopting what was perceived as a high risk activity in terms of the cost of such development and the consequences of failure. Beta Electronics as a sub-contract manufacturer adopts a conservative attitude to high technology. The perceived risk within the organisation would have been a strong impediment to the adoption of an ASIC design. It is important to try and see the opportunities that lie beyond the risk and the resulting rewards. The adoption of ASIC technology was perceived as an uncertain road to take.

11.3 Technology Barriers
The technology barriers were relatively minor in terms of the lack of skills shortages. The first user knew the benefit in training and the jump from FPGA based design expertise to ASIC design was achievable.

11.4 Financial Barriers
The first user is a relatively small company with limited resources. The budget required for an ASIC design is large and hence the financial risk is enormous. The first user could only invest such an amount if the risks were minimal and the sales forecasts of the improved product were certain. It is primarily the size of the investment in relation to the size of the company that was the greatest barrier. The diversion of existing manpower resources was also a barrier since other activity within the company would be delayed or stalled.
12. Steps taken to overcome the barriers and arrive at an improved product

12.1 Knowledge Barriers
The knowledge barriers were addressed during the feasibility phase leading to a submission of the proposal. The first user received some advice from the TTN and was given details of a number of design consultancies. With this in mind, the first user contacted a number of consultancies to discuss some of the issues in commissioning the design of an ASIC from supplied VHDL. Some of the consultants gave useful advice and provided a draft proposal on what could be done. The first user also investigated the availability of VHDL training courses and was offered a suitably tailored course by sub-contractor1. Having received much useful advice on the procedures both technical and managerial for designing an ASIC, the first user was still uncertain about dealing with the sub-contractors. The TTN was very helpful in advising the first user on many issues related to sub-contractors. A request to tender for the work was sent out to a number of design consultancies. The knowledge gleaned from the tenders was very useful in both selecting a suitable sub-contractor as well as becoming familiar with the important issues.

12.2 Cultural and Inertia Barriers (Psychology)
The first user realised that in order to continue innovating, that it would be necessary to adopt new technologies and acquire new skills. It was successfully demonstrated to the senior management within the organisation that it was strategically important to acquire these skills. The Zandar division of Beta Electronics was viewed by management as a high technology division supplying high quality sophisticated products to a sophisticated market. Therefore it was not difficult to demonstrate that acquiring ASIC design expertise and embarking on an ASIC project would be consistent with this view.

Financial Barriers
The main financial barrier was overcome by commercially justifying the development of the ASIC. The eventual cost savings and performance improvement that the ASIC could provide were demonstrated with sales forecasts of systems using the component. The return on investment was outlined for worst case and best case forecasts. The financial risk was partitioned into commercial risk and technical risk. The technical risk was seen as the lesser risk compared with the commercial risk.

12.3 Barriers overcome during the application experiment.
The time elapsed between the submission of the proposal and the start of the AE meant that some of the financial forecasts became invalid. The NRE costs of the project had increased as well as the first user’s overheads. Two of the sub-contractors had increased their fees in the intervening period. This was overcome by negotiation with the parties involved and in persuading them to charge the previous rates. The arrival of new low cost video scaling ICs from other semi-conductor manufacturers also presented a new financial barrier. It meant that commercially justifying the development as not as clear cut as was indicated earlier. This was alleviated however, by new market information that indicated a need for higher picture quality in the video re-sizing. The new video re-sizing ICs were still of relatively low quality and the first user needed to amend its specification to design a higher quality device. This shift in emphasis from a pure cost comparison to a quality comparison was still commercially justifiable as it would enable the first user to have pole position in terms of picture quality in its multi-image display systems without having to increase its existing costs. The technical specification was amended to produce a premium quality video re-sizing IC that would be comparable in cost after NRE with the lower quality counterparts.

13. Knowledge and experience acquired
The AE was the largest and most sophisticated project ever undertaken by the first user. Previous projects and product developments were less sophisticated and required less project management expertise. The nature of ASIC design is that everything must be correct first time.
The knowledge and experience acquired falls into two categories.

**a) Technical**

The technical experience and knowledge was as a combination of formal training, interaction with sub-contractors and self-learning. These three elements were vital in being able to conduct the experiment successfully. The formal training was in the form of a 3 day intensive VHDL design course in the NMRC, Cork. The interaction with sub-contractors illustrated some of the more subtle design issues with ASICs as compared with FPGAs. In particular, the importance of test vector timing in relation to asynchronous signals was not appreciated until the sub-contractor performed worst case and best case timing simulations. The first user had never devised a test bench for an ASIC so this was a combination of self learning as well as guidance from the sub-contractor. The first user had never used a formal design method for developing a component or system. More specifically, this was the first time a behavioural model in C was written, ported to VHDL and then verified with an RTL simulator in combination with a C front end.

**b) Project Management**

The project management experience gained was most useful. The first user had never previously managed a project in conjunction with 2 sub-contractors. This is particularly significant when one considers that one of the sub-contractors was providing design services and expertise in an area where the first user had little prior knowledge.

The planning of the AE was a useful experience since it required the generation of a detailed work plan containing milestones and deliverables. The first user would normally have produced a far less detailed work plan for an internal development project so it was a new experience in producing the technical annex for the experiment. The TTN also provided much advice on the proper formatting of a work plan.

The AE also involved the generation of a detailed ASIC design data sheet. This is similar to the IC data sheets that semiconductor companies provide with their products.

**14. Lessons Learned**

Many lessons were learned as a result of conducting the AE. They could have helped to avoid the pitfalls that the first user encountered during the AE. Each of the most important lessons are listed below:

**FPGA emulation was not the best verification tool for the AE**

The time spent in trying to squeeze the design into an FPGA was largely wasted. It became apparent that a software front end connected to the VHDL simulator would give faster results. The number of changes that would be made to the design during the verification phase runs into hundreds. Given that a synthesis, place and route of an FPGA take 4 hours, makes it painfully clear that it would have taken many more months to verify the design. Instead, the FPGA emulator was abandoned in favour of a software interface to the VHDL simulator that enabled the VHDL model to accept bitmaps as incoming video and output bitmaps as the output video. The time taken to write the front end software was far less than the time it would have taken to do a handful of FPGA design iterations. However, it is still considered useful to perform FPGA emulation where time or resources permits. It is very important not to sacrifice rigorous verification through simulation in favour of FPGA emulation. In this instance, the ability to view the results graphically using the software front end had many of the benefits that FPGA emulation would have lent to the AE.

**Plan the test harness carefully at the beginning of the project by specifying it in detail**

The test harness is the ultimate verification between the first user and sub-contractors that specifies correct operation of the design. A proper test harness therefore simplifies the interface between the sub-contractors and reduces the chance of a disagreement over the correct operation of the device. This was not considered properly until the AE began and the first user got into serious discussions with the sub-contractors.
Amend the technical annex at regular intervals to take account of spec. changes
It is difficult to keep track of a project if it’s specification changes but the changes are not reflected in the work packages set out in the technical annex. The danger exists for the project to go out of control because the deliverables may have changed or their delivery dates may have altered. This is mostly to do with good project management discipline.

The refinement of the spec. as the AE proceeds. This is particularly important for ASIC design and is similar to the previous point except it relates to the product and component specification. It is not possible to produce a refined specification at the beginning as there are many ‘don’t knows’ such as technology limitations etc. The refinement of the specification as it proceeds prevents the possibility of out of date documentation. It is also important to avoid the pitfall of ‘creeping elegance’ where the specification is gradually improved with each small improvement not affecting deadlines or budgets but in their entirety, making the experiment non-viable. In practice, there was only one major addition to the specification and that related to increasing the quality of the re-sizing by changing the resizing algorithm. In actual fact, some minor functions were removed to either keep the AE on schedule or because it became apparent that the function was no longer considered useful.

The design implementation phase takes longer than expected
This phase of the AE was severely underestimated largely due to the lack of knowledge in designing a complex ASIC in VHDL. That are two unknowns for the first user, the adoption of a new language to describe a circuit, and its implementation in an ASIC.

The design flow is not a linear flow (There are loops) This relates to the design implementation. Each stage in the specification and design process should normally be signed off before proceeding to the next stage. In practice, changes had to be made to the specification as it became apparent that it could not be properly implemented during the design process. The result was that there were a number of design and specification iterations or loops to parts of the ASIC design.

Ensure that the specification is frozen before commencing design implementation. This relates to the previous lesson learned. Any design limitations must be fully understood when a specification is devised. Otherwise the prospect of multiple iterations of design changes becomes likely. Specifically, the first user did not know about certain memory limitations within the chip express gate array. They were largely undocumented. The first user only discovered the limitation, when the initial design was submitted to the sub-contractors for a quotation. The result was a loop back to specification where it was necessary to add a memory management unit to the ASIC. This is just one example of many changes that had to be made to the specification during the design phase. While it is probably impossible to avoid such loops, more time should have been spent in avoiding as many loops as possible.

Talk to the foundry sub-contractor about available IP cores to speed up development
The first user learned after the ASIC prototype was fabricated that the foundry had a number of DSP IP cores that could have been used to speed up and optimise the design. Chip Express had optimal multipliers and dividers and other arithmetic functions which could have been utilised if the first user had investigated the availability of such cores more thoroughly. Most foundries give very little technical support to small companies prior to an ASIC design so the above observation may only be valid for Chip Express who were very helpful in providing advice and technical support during the design process.

Plan the deployment of staff more carefully
The first user ran into many difficulties when staff were re-deployed to perform the AE. Other aspects of the first user’s business suffered. This was particularly acute given that Zandar Technologies has six full time people of which one third were re-deployed to perform the AE. An increase in business during the AE along
with personnel changes presented many difficulties and challenges to the first user. There was no scope to take personnel off the AE for more than a day at a time as the AE was already running behind time.

In relation to the lessons learned above, the first user considered what it would do differently if the experiment were to be repeated. The following bullets highlight the main points that the first user would reconsider.

**What the first user would do differently if repeating the AE.**
- Spend more time on putting a formal design verification procedure in place.
- Talk to the foundry directly as early as possible about technology specific issues and limitations.
- Give the sub-contractors as more information at an early stage so as to get a better quotation
- Attempt to shorten the time interval between submitting the proposal and starting the AE
- Have a clearer definition and specification of the product using the ASIC prior to commencing the AE
- Ensure staff that are allocated to AE do not adversely affect other aspects of the first user’s business.

**Summary**
The first user is very satisfied with the outcome of the AE. Most of the lessons learned have encouraged the first user to further utilise ASIC technology in its products where economically justifiable. None of the lessons would discourage the first user from embarking on another ASIC development.

**15. Resulting Product, it’s industrialisation and internal replication**
The resulting target product range has been code named the OmniVideo-Digital. This is a multi-image display system based on the concept of the existing OmniVideo series of PCI cards and stand alone systems. (See Section 6.)

The main advantages of the OmniVideo-Digital over the Q600 and existing OmniVideo series are:
- Digital video inputs in the form of SDI
- Extremely high quality video re-sizing using Zandar proprietary video re-sizing ASIC
- Low cost system
- Flexible user selectable video window sizes and positions.

The OmniVideo-Digital is in the design phase. The product will incorporate up to 16 ASICs per system to give up to 16 displayable windows. The ASIC prototype has been returned from sub-contractor 3 and is integrated on a video evaluation board. The role of this board is to test the ASIC, perform field trials for assessment of the quality of the video and finally to exhibit the technology at trade shows.

A new specification is being compiled for a planned new product known as the Raster Video Processor (RVP). This will incorporate up to three ASICs per system where very good image quality is considered essential. It is anticipated that some minor changes to the existing ASIC may be necessary to incorporate into the RVP.

In going to production of the OmniVideo-Digital, the first user will retain the same sub-contractor to provide production quantities of the ASIC. In the event, that design changes are necessary, sub-contractor 2 will be retained to assist in the re-compile of the amended design.

All of the intellectual property within the ASIC remains the sole property of the first user. This consists of the VHDL source code and compiled gate level net list. Subcontractor 2 provided design services with no claim on IP while sub-contractor 3 manufactured the gate array ASIC according to the first user’s specifications. Neither subcontractor is entitled to use any of the first user’s code without its express permission. The first user has used its own non-disclosure agreement when imparting sensitive material to third parties. The NDA
forbids any party from using or disseminating the information for any purpose other than to complete work agreed with the first user.

The improved product OmniVideo-Digital range will be launched at a Trade Show (NAB99) in Las Vegas where quality and price will be extolled as its main virtues.

The first user believes that the ASIC and the video re-sizing technology contained therein will form the basis for the next generation of products. The company will move into the broader market area of providing the display glue electronics that separate a video signal source from the display. Central to this theme is the requirement to re-size video.

16. Economic impact and improvement in competitive position
The economic impact and improvement in competitive position is complex. There are two factors that affect the impact. The existing products that were sold before and during the AE used FPGAs that are expensive and produced picture quality that was adequate. However, market demand and the changing competitive environment has meant that a demand for higher quality systems at a competitive price means that the impact has to be split in two. Firstly the effect on manufacturing cost of the new products with the introduction of the ASIC and the sales of such product that are purely as a result of that improved picture quality. The first category is simple to quantify while the second is based on sales forecasts and a rough estimate of what percentage of sales could be attributed to the improved picture quality allowed for by the ASIC.

A 16 picture card set utilising 16 video re-sizing FPGAs costs approximately 3KECU ex factory in medium quantities. This compares with the current analog input solution costing 2KECU and a solution based on the high quality ASIC costing approximately 2.1KECU. A solution based on a high quality third party video scaler would cost approximately 2.5KECU. This is based on a manufacturing and material management cost that is proportional to the material cost.

The economic impact is best assessed in comparing the ASIC based digital input solution with that of the next most viable digital input solution which utilises a third party video scaler. The ASIC component is 46% the cost of the third party video scaling IC. In this instance there is a product cost saving of 16% or a unit cost saving of approximately 400ECU per system.

The OmniVideoDigital multiviewer systems will come in a number of variants from 6 input systems to 16 input systems. As a result, they will use differing numbers of video scalers. There is one video scaler for each input such that a 6 input system will contain 6 scalers while a 16 input system will contain 16 scalers. Sales forecasts for Years one two, three and for of the product life cycle are set out in the table below in terms of the number of video re-sizing ICs.

<table>
<thead>
<tr>
<th>YEAR</th>
<th>No. of Scalers</th>
<th>Material cost TPVS</th>
<th>Material cost ASIC</th>
<th>Cumulative ASIC Cost Saving</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>142</td>
<td>6106</td>
<td>2982</td>
<td>3124</td>
</tr>
<tr>
<td>2</td>
<td>1183</td>
<td>50869</td>
<td>24843</td>
<td>29150</td>
</tr>
<tr>
<td>3</td>
<td>2810</td>
<td>98350</td>
<td>47770</td>
<td>79730</td>
</tr>
<tr>
<td>4</td>
<td>6220</td>
<td>186600</td>
<td>68420</td>
<td>197910</td>
</tr>
</tbody>
</table>

Material is costed on differing price breaks in different years

It is anticipated that a small percentage of overall sales of the OmniVideoDigital video will be achieved solely as a result of the higher quality and functionality of the ASIC gate array over any other option. This is shown in the table below as a percentage of the accumulated gross margin of the OmniVideoDigital products.

<table>
<thead>
<tr>
<th>YEAR</th>
<th>Small % of cumulative gross margin Of OmniVideoDigital Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>--</td>
</tr>
<tr>
<td>2</td>
<td>64KECU</td>
</tr>
<tr>
<td>3</td>
<td>188KECU</td>
</tr>
<tr>
<td>4</td>
<td>453KECU</td>
</tr>
</tbody>
</table>
The above tables show a return on investment of 93KECU in year 2, 267KECU in year 3 and 650KECU in year 4. For an initial investment of 189KECU, this indicates a payback period of 2 to 3 years.

16.1 Future Improvements to AE based product
The technology implementation of the first user’s video re-sizing algorithm has revealed a number of future product opportunities. The need to re-size video is going to increase as the digital TV revolution progresses and TV display technologies improve. The first user sees opportunities for further enhancements to the ASIC including the ability to re-size high definition video, to zoom video as well as shrink video.

Benefits to the First User of the AE

- Educational Value
- Core Technology
- Increase IP value of company

16.3 Competitive position since the start of the AE
A number of companies have launched new multi-image display products since the start of the AE. Many of these are high resolution output display products utilising high quality video re-sizing. Many of the products also offer digital video inputs and are competing heavily against the Q600 and OmniVideo series of products that Zandar currently sells. This new competitive position also suggests a growing market for these types of products and serves to reinforce the rationale behind the AE.

17. Target audience for dissemination throughout Europe
This AE covers the development of a Gate Array ASIC developed by an 6 person company for a video application. The FU had previous micro-electronics expertise, including FPGA design. In this AE they learnt how to use VHDL to develop an ASIC, and now have these skills in house. The project would be particularly interesting to two different types of companies:

a) Companies with an existing product using electronics (FPGA, microprocessor, etc.) willing to reduce costs or to improve the product quality by converting the existing technology to a gate array or digital ASIC. Especially for those who require a small number of units (5,000 to 20,000), where a gate array provides a better solution than a full ASIC.

b) Companies with experience in microelectronics interested on the introduction of a new (advanced) technologies in their product. Especially for those companies willing to acquire the required knowledge to be able to carry out ASIC design in-house.