An improved Linear CCD Control System
FPGA technology provides improved accuracy and flexibility
Control Applications is a small, 7-year-old research and development company specialising in the design and development of industrial automation systems. The company employs 6 employees, and in 1999 achieved sales of approximately 300,000 Euro.

Specifically, Control Applications (CA) is specialised in the organisation & automation of production lines in the industrial fields of Aluminium, Cement, Food, Manufacturing and Mining. This includes collection of data and visual representation, automatic control of productions lines and quality control of end products. CA is considered to be the only Greek company that develops machines for visual quality control. The personnel of the company are comprised of electronic engineers and computer scientists integrating backgrounds and skills from the domains of image processing, industrial applications development, s/w design and development and production automation.

Line scan sensors are utilised by the company in its products. These products range from rice to fruit sorters and operate in real-time. Speed and colour resolution are very important parameters.

Different sensors are used according to the application, and for each one a new board had to be designed with the discrete technology used today, though most of them share common characteristics. Due to the ‘old-fashioned’ technology that was used only the absolutely essential functions, such as timing, correlated double sampling, gain and offset were practicable to be incorporated.

The objective of the Application Experiment was:

i. To improve the electronics in the existing sorting systems to improve efficiency and add the capability of handling a series of line scan cameras.

ii. To design a new board using an FPGA. This board will be common to all sensors and at the same time will take advantage of the increased capabilities offered by the new technology, meaning that additional functions will be incorporated.

iii. To reduce product set-up costs by 18% and increase sales (mainly exports).
The application of FPGA technology produced the following product improvements:

* The improvement in the existing sorting systems makes the Control System more efficient and capable of handling series of line scan cameras.

* The new board has additional functions such as timing, correlated double sampling, gain and offset.

* Reduction in production costs, specifically the PCB costs were reduced by approximately 60% while the component costs decreased by 20%.

* Improvement in quality.

These additional product features provide new customer benefits and product differentiation features that improve Control Applications’ market competitiveness.

The application experiment was completed in 10 months and cost 55,000 Euro. The payback period for the application experiment will be 15 months, and the return on investment is estimated at 364 % over 4 years of life.

Following the application experiment, Control Applications is now capable of undertaking the incremental design of the improved product for other applications, and the manufacture of the new products.

**Keywords and AE signature**

Generic CCD Controller

Pixel by pixel gain correction

Quality control

FPGA

**AE signature:**

3 - 0 1 5 4 5 5 5 0 4 2 0 - 2 - 3 3 3 0 - 1 - 3 3 - GR
1. Company Name and Address

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Telephone: +30-1-93 56 005
Fax: +30-1-93 16 130

2. Company Size

Control Applications Ltd. has 6 employees. Company sales turnover is approximately 300,000 Euro.

The team of engineers working in Control Applications is comprised of electronic engineers and computer scientists, specialists in the domains of image processing. Until the completion of the AE, they had very little experience in microelectronics technologies, mainly in the fields of microprocessors. Specifically, the team is comprised of electronic engineers and computer scientists integrating backgrounds and skills in the domains of image processing, industrial applications development, software design and development and production automation.

Two persons were allocated for the project, George Stratigos, who was responsible for the technical management of the AE, and John Karatzas, who was the application specialist responsible for the development of the hardware.

3. Company Business Description

Control Applications is a medium sized, well established company involved in the design, manufacture, marketing and servicing of industrial automation. It started its activities with
the design and development of turn key solutions in the fields of Aluminium, Cement, Food, Manufacturing and Mining.

Specifically, Control Applications is specialised in the organisation & automation of production lines in the above industrial fields which includes:

- Collection of data and visual representation,
- Automatic control of productions lines,
- Quality control of end products.

Based on the vast experience of its staff, acquired through work in the different industrial fields and considering the size of the Greek market, the company has gained experience and know how in solving problems specific to industrial enterprises through the design and development of customised applications. CA is considered to be the only Greek company developing completely machines for visual quality control, featuring low cost and high-resolution capacities. These products' main advantages are their manufacturing simplicity and the efficiency of their operation.

4. Company Markets and Competitive Position at the Start of the AE

The company designs and develops products mainly for the Greek market. For the estimation of the size of the addressed market two parameters have to be taken into account.

1. The wide range of applications based on line scan sensors. These applications range from small particle sorters (rice, salt etc.) to size and quality inspection systems (bottles, plastic pipes, cigarettes, etc.).
2. The increasing demand for optical inspection systems, which is becoming an imperative stage in many production lines due to the growing quality demand of the consumers.

These products have high export potential not only to Europe and Cyprus but also to countries of the Middle East such as Egypt, Jordan and Lebanon.

Taking into account the wide range of possible applications and the diversity of the addressed market, most of the products developed by the company up to now were custom made applications with very little standardisation. It is a process of continuous research and development but at the same time the strong point of the company due to the expertise
gained. Competitors are differentiating as they are delivering products of standard specifications not easily adaptable to the customer’s specific requirements. An approximate figure is 50 quality control and inspection systems per year but it is constantly increasing. Taking into account that each system on average requires at least 4 line scan cameras, thus a number of 200 cameras per year are required. These applications are divided as follows:

<table>
<thead>
<tr>
<th>Product description</th>
<th>%</th>
<th>Pcs / Year.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small particle sorters (rice, sultanas, salt)</td>
<td>60%</td>
<td>30</td>
</tr>
<tr>
<td>Larger sorters (olives, oranges, peaches)</td>
<td>30%</td>
<td>15</td>
</tr>
<tr>
<td>Inspection systems (plastic pipes, cigarettes, drugs, wood, ceramic)</td>
<td>10%</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 4.1. Domestic Market (pcs).

Control Application's customers derive mainly from end users and distributors in the Greek food industry. Successful installations have been completed at a large, well-known rice manufacturer in Thessaloniki - Agrino SA. Agrino was extremely satisfied with the results on its production lines, particularly the large reduction in wasted material achieved with the automated vision quality control systems installed at the plant. Similar systems have been sold to other manufacturers undertaking quality control of fresh tree-born fruit (e.g., PanFruit) and nuts. Additionally, the large olive industry in Greece can benefit from such innovative technology and is a future target of CA.

Control Applications foresees a large market share for the improved product, specifically in Greece. While open to the larger European market, business in Greece is still conducted very much on a personal basis, based on personal relationships. This situation will allow CA to increase its market position against its foreign competitors. Furthermore, productivity and quality are highly motivating factors for industry, especially with today’s global competition, thus the demand for low cost artificial vision systems is constantly growing. The new technology will allow many industries to introduce this technology to their production lines in order to increase productivity and product quality at a reasonable cost and thus to became more competitive.

COMPETITOR description - market shares

Before the introduction of CA’s products in the Greek market, certain competitive products were imported from abroad, mainly from England (SORTEX) and the USA (Satake), but
only small particle sorters. The main problems faced with these systems was set-up, maintenance and servicing. Since the establishment of CA, the level of these imports has been greatly reduced. CA utilises the linear CCD control system mainly for inspection systems and particle sorters. The following table compares the market pricing for rice sorters (with a production capacity of 1.5 tn/hour)

<table>
<thead>
<tr>
<th>Company Name</th>
<th>Cost (in KEuro)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SORTEX (UK)</td>
<td>60</td>
</tr>
<tr>
<td>SATAKE (USA)</td>
<td>85</td>
</tr>
<tr>
<td>CA (Greece)</td>
<td>40</td>
</tr>
</tbody>
</table>

**Table 4.2. Competitors market situation**

The main drawback that CA’s systems have faced (because they were based on discrete technology) was the requirement for regular adjustments and calibration. This factor limited the export potential of the products. After the development of the new product these drawbacks don’t exist anymore and the export potential of the company’s products is evident.

CA’s mainly competitors in the domestic market are SORTEX and SATAKE. SORTEX and SATAKE with other minor competitors hold the 80% of the domestic market. CA currently controls approximately 20% of the Greek market.

The level of sales achieved by CA has remained relatively steady in recent years. It is believed that the new enhanced features of the AE product will provide a stimulus to drive
sales upward given the better performance and price characteristics, especially in comparison with the competitors’ products.

The AE industrial sector is Industrial Process Control Equipment (Prodcom code 3330).

The AE target markets will be in the industrial sector of Manufacturing, especially fabricated metal products (except machinery and equipment), food products and beverages.

Competitors are differentiated on the basis of the technology utilised and the price of their products. With respect to technology, most competitors use photodiodes for object detection, which is mainly monochromatic and has a limited area of detection. Due to the complexity of the mechanical systems utilised with the above-mentioned technology, the production cost of competitors’ systems is very high. CA's improved product will have a retail price between 12,000,000 and 20,000,000 GRD (37,000 to 61,000 Euro). The range in price depends upon the material to be controlled by the application, the control application level and the customer’s special requirements (which can require derived equipment) as well as the number and the technical specifications. Specifically, the factors that contribute to the cost per unit are application specific and include the following:

- Response time of the valves
- Size and number of feeding belts
- Feeding mechanism
- Resolution requirement which determines the requisite number of cameras.

Therefore, the unit cost depends on the application.

5. Product to be Improved

Control Applications is currently producing integrated image processing quality control systems, in particular vision systems using line scan cameras. Line scan cameras can be applied to a wide range of industrial and scientific applications, ranging from document scanners to transportation belt inspection systems and particle scanners for almost all the quality control artificial vision systems. The main applications of the AE product are in the food industry. Products (seeds, fruits, etc.) can be checked automatically through the use of such technology, thereby eliminating the role (and related subjectivity and fatigue disadvantages) of human quality control operators. Products are viewed by the set of cameras employed and then the acquired information is compared to a reference set of data in order to discard those of poor quality, thus increasing productivity and product quality. Such systems can often be placed at several different points on the production line.
CA has designed a camera for its applications using the discrete components available. The camera was designed in 1996 and its block diagram is as follows:

![Block Diagram of the Current Product](image)

**Figure 5: Block diagram of the current product**

**Sony ILX Series Sensors**

Four types of 3-line colour linear sensors can be used for colour image scanners with A4-size 300 DPI, 400 DPI and 600 DPI resolutions, and A3-size 600 DPI resolution. These sensors range from 2700 to 7078 pixels per line for each colour. Taking for example the smallest one, ILX524, there are three lines (RGB) of 2700 pixels each. All lines are clocked in parallel at a frequency of 1 to 5 MHz depending on the application. The sensor’s output is processed according to the block diagram and both analogue and digital outputs are available.

**CDS**

Correlated Double Sampling (CDS) is a type of circuit devised for reducing the noise generated in the sensors output stage. Using the noise correlation in the precharge and data sections of the linear sensor output, the noise is suppressed. There are two basic types of CDS:

a. **Clamp Method.** The effects of the clamp method are elimination of the reset noise and low frequency noise suppression.

b. **Subtraction Method.** This method eliminates the same effects as the clamp method and in addition reduces sample and hold pulse feed through.
Both the clamping and subtraction methods are used for optimum results.

**Timing Generator**
The timing generator provides all the necessary drive signals for the sensor’s operation and optionally the switching signal for the A/D converter.

**PGA**
The gain of the output amplifier is variable from 0.2 to 9.5 dB.

**A/D Converter**
Optionally an A/D converter can be used with a resolution of 8 bits/colour (24 bits total).

Line scan sensors are used in conjunction with lenses and lighting devices. Commonly, lens transparency is not linear for all colours across the usable area of the lens. Also, lighting in industrial applications is not uniform and it varies with time due to fatigue of the lighting devices and contamination (e.g., dust). Sometimes the sensitivity of the sensor itself is not linear for all pixels due to manufacturing tolerances. The sensitivity value is influenced by two factors. One is the photoelectric conversion sensitivity of the CCD block and the other is the output amplifier block gain. For all the above it is imperative to implement *pixel by pixel gain correction* of the sensor output.

The main parameters to be improved:
1. Reduction in the complexity of the overall control system. The hardware is going to be greatly simplified by dramatic reduction of the component count.
2. The flexibility of the system is to be improved by the reprogramming capabilities of the system.
3. Pixel rate (data rate) is to be improved by improved timing characteristics of the new components.
### Table 5.1: Comparison of the new and old designs.

<table>
<thead>
<tr>
<th></th>
<th>Old design</th>
<th>New design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel rate</td>
<td>1MHz</td>
<td>1 MHz .. 5 MHz</td>
</tr>
<tr>
<td>CCD type</td>
<td>ILX Series</td>
<td>Any type</td>
</tr>
<tr>
<td>Self calibrating capability</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Pixel by pixel correction</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Detection algorithm</td>
<td>Predefined</td>
<td>Programmable</td>
</tr>
<tr>
<td>Colour resolution</td>
<td>8 bits/colour</td>
<td>10 bits/colour</td>
</tr>
<tr>
<td></td>
<td>Total: 24 bits</td>
<td>Total: 30 bits</td>
</tr>
<tr>
<td>PCB size</td>
<td>100%</td>
<td>30% of the old design</td>
</tr>
</tbody>
</table>

Additional product improvements, which cannot be quantified, include improved diagnostic capabilities and hence improved in-service ‘reliability’. Improved operation over a much wider temperature range due to the self-calibrating features of the new board. Self-diagnostic features are to be incorporated, thus resulting in fewer service calls. The utilisation of an improved controller unit will enable these limitations to be overcome.

*Figure 6.1:* Photo of the improved product.
6. Product Improvements

Figure 6.1 (previous page) is a photograph of the improved product. As stated previously pixel correction is a very important function of a camera operating in industrial environment. Another very important function is self-calibration of the camera in order to compensate for temperature and lighting drifts at regular time intervals.

![Figure 6.1: Photograph of the improved product.]

Figure 6.2: Output of a scanning camera.

The above figure displays the actual and the ideal (required) output of a scanning camera. The actual output is not linear because of the implementation of lenses for the focusing of the incoming light on the sensor. The lens coatings are not homogeneous across the entire visual spectrum resulting the output bias shown in the figure. Furthermore, other parameters affecting both the shape and the level of the output are temperature and dust contamination of the optics. In order to compensate for these deviations the gain of PGA (Programmable Gain Amplifier) has to be adjusted for each individual pixel. During factory calibration the ideal (required) output is set up. These reference gain data are stored in memory. The scope for recalibration during operation is the adjustment of the gain factors in order to obtain the required output. The gain factor is calculated according to a machine dependent algorithm. In regular time intervals, depending on environmental contamination and fluctuations in temperature, the CCD output should be adjusted against a constant background (white balance). The individual data for each pixel are stored in RAM. During normal operation the gain for each individual pixel is corrected according to these stored data. The whole procedure is hardware implemented because of timing restrictions. The above procedure cannot be performed by software due to the number of calculations involved and the timing restrictions imposed by the CCD.

The new design which will address many of these problems is described on the following page:
A single FPGA fulfils the timing, gain and offset requirements of the sensor. Thus complex discrete circuits are avoided and the set-up for each particular sensor is greatly simplified. Most importantly, pixel-by-pixel gain correction and calibration of the camera now can be implemented. Employing external memory (RAM) into the FPGA the operation of the system will be as follows:

![Figure 6.3: Block diagram of the new product.](image)

![Figure 6.4. FPGA Internal Block structure](image)
Calibration data, such as timing, number of pixels, overall gain and offset, which are specific to the sensor and do not vary are serially stored in RAM (block2).

The Timing Generator supplies the timing signals for the sensor as well as for the ALU according to the stored calibration data.

The operation of the ALU depends on the mode selection. When in calibration mode, the data from the A/D converter are compared with a preset value (stored in the calibration data) and the results are stored inside the RAM (block1). In operation mode, the data from the RAM are clocked synchronously with the incoming pixels to the PGA. Thus the output of the PGA is corrected for each pixel.

The improved product has the following additional specifications:

a. Calibration with PGA Gain and Offset data upon system start-up. In its previous form, the product required several days work of an engineer to complete this process.

b. Self-Calibration of the system with temperature and lighting data, every 15 minutes at minimum, so that the camera can compensate for temperature and lighting drifts. This is a new feature, which was nearly impossible to be applied previously. This calibration is necessary because of the machine’s industrial working environment (dust contamination, light drifts, etc.) and is referenced to the initial native colour and sensitivity settings.

c. *Pixel by Pixel gain correction* of the output of the sensor, which is now performed in a more simplified way.

d. Incorporation of RAM in order to store the various calibration data and/or result data from the ALU.

e. Timing generator block to determine the exact timing.

The last three (c,d,e) improvements enabled the design a new board of much smaller dimensions one eighth (1/8) the initial size with much smaller component count and therefore cost.
The most important feature of the improved design is the ability of the board to process data at much higher rates (i.e. pixel rates). Here is the comparison of the two designs:

- While the previous design processed a maximum of 7.5 Mpixel/sec, the new design can easily process 15 Mpixel/sec.

The improved product will operate in 3 different modes:

⇒ PGA Gain Calibration Mode (upon start-up only)
   This is set-up at the factory.

⇒ Data Self Calibration Mode (every 15 minutes at minimum)
   Compensation for the industrial working conditions, calculation and storage of gain factors for each pixel.

⇒ Normal Operational Mode
   Pixel by Pixel gain correction mode according to the stored data.

Table 6.1: The improved parameters of the new design.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Improved Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel rate</td>
<td>1 MHz - 5 MHz</td>
</tr>
<tr>
<td>CCD type</td>
<td>Any type</td>
</tr>
<tr>
<td>Self calibrating capability</td>
<td>YES</td>
</tr>
<tr>
<td>Pixel by pixel correction</td>
<td>YES</td>
</tr>
<tr>
<td>Detection algorithm</td>
<td>Programmable</td>
</tr>
<tr>
<td>Colour resolution</td>
<td>10 bits/colour (Total: 30 bits)</td>
</tr>
<tr>
<td>PCB size</td>
<td>30% of the old design</td>
</tr>
</tbody>
</table>

Figure 6.5: The FPGA’s PCB.
7. Choice and Rationale for the Selected Technologies, Tools and Methodologies

The selection of an appropriate control technology requires the consideration of the following factors:

- **Flexibility** – as several line scan sensors exist in the market, each one with specific operating characteristics. Thus, new sensors should be accommodated for without the need for complex redesigns or circuit board changes.

- **Flexibility to modify control algorithms necessary for the product to operate in a wide range of end user environmental conditions and specifications.**

- **Low device cost.** Although the added functionality of the system will provide user benefits, it was an objective that the lowest cost implementation route should be adopted. Therefore, the criteria that the solution had to satisfy included both flexibility and price constraints. The choices that were examined for the proposed technology follow below:

◊ **Digital ASIC.** It is true that the digital parts of the existing product that are intended to be integrated do not have the appropriate complexity in order for the design of a Digital ASIC to be the recommended solution. In other words, the design for this application experiment is not as extensive as someone would expect so that the ASIC solution would be proposed.

◊ **MCM.** Likewise MCM would be even further beyond the scope of this application, economically and technically speaking.

◊ **Mixed Analogue/Digital ASIC.** On the other hand, if the chips that largely implement analogue procedures, like the D/A Converter and the Programmable Gain Amplifiers, were intended to be integrated as well, then a mixed Analogue/Digital ASIC could have been proposed. In that case though, the evidence for economic assessment would have been fairly weak, meaning that this chip would have been much more expensive than needed and subsequently the final product would not have acquired the increased competitiveness that First Users Action addresses.

◊ **Microcontroller** versus **FPGA** solution. Another solution, the Microcontroller-based design, was also closely considered. First of all, a microcontroller was proved to be so slow while operating that using it would completely defeat the purpose of an Application Experiment. Only a hard-wired design like an FPGA circuit could achieve the required performance. Arithmetic operations, such as those that are needed, would need, in a
microcontroller design, several machine cycles, where a single machine cycle occupies several clock cycles. In an FPGA synchronous design, the same operation is completed within nanoseconds during a single clock cycle. The same applies to operations like the simple AND or OR functions. Applications where a microcontroller would be a more suitable choice include the implementation and control of a serial bus protocol, implementation of a software environment like a small operation system (procedures for data input/output etc.). Furthermore, in cases where the integration of a number of discrete components that implement random logic is needed, an FPGA solution is clearly the best choice.

The FPGA option was selected by the company because of the following perceived advantages:

i. Design flexibility and cost requirements were met.

ii. The technology advance enabled the company to develop its own staff to the necessary level with minimum technical risk and offers prospects for replication by the company.

iii. A relatively low risk product upgrade path as design adjustments can be implemented in software revisions.

As previously mentioned, the choice was come to after serious consideration of the other possible solutions, including testing in some cases (e.g., microcontroller). The FPGA technical characteristics are:

- Max frequency \( \cong 50 \text{ MHz} \)
- CP lds \( \cong 300 \)
- I/O pins \( \cong 150 \)

The major task in this application experiment involved the re-targeting of an existing design that uses discrete components into a Xilinx FPGA. Design entry and functional simulation was performed using the popular Quick VHDL-Lite system. Afterwards, the appropriate synthesis tools, like ALDEC synthesiser, which is part of the Xilinx Foundation Series toolset, were used so that the VHDL source code was synthesised. The Xilinx Foundation Series tools were then used for targeting the specific Xilinx part, while XACT was used for P & R as well as device programming. Detailed timing simulations were performed using the Active CAD simulator that is also part of the Xilinx Foundation series.
8. Expertise And Experience In Microelectronics And The Staff Prior to the Application Experiment

The company’s design expertise is based on the vast experience of its staff acquired through work in different industrial fields. Due to the size and diversity of the Greek market addressed by the company, it has gained considerable experience and know-how in solving specific problems of industrial enterprises through the design and development of customised applications. Most of the designs are analytical TTL designs with limited use of microcontrollers.

Until now there is no experience in designing or applying FPGA technologies and thus the Application Experiment was an excellent chance for the company to acquire knowledge of such technologies and upgrade its products.

The engineer allocated to the application experiment had no previous electronic design experience with FPGAs or the design entry and simulation methods related to them.

This engineer possessed a technician level qualification in electronics and had over 8 years practical experience in the area of electronic products development.

The company allocated a project manager to the application experiment to act as the Technical Manager. This individual also had no previous experience in the management of microelectronic product development.

9. Workplan and Rationale

The work was carried out in a 10-month period and the major work activities conducted during the application experiment are described below.

Workpackage 1: Technical management

CA took over the Technical management since it was the party most interested and most suited for this role. It was a new field of expertise for the company and on-the-job training in
this area was considered necessary. In addition, having the assistance of a well-experienced subcontractor in the particular field of applications was considered a great opportunity. Thus the role of the subcontractor during this phase was limited to the provision of advice and assistance on a request basis. Basically it consisted of advice on availability and delivery issues of specific categories of components and on planning strategies in order to obtain optimum results in the shortest amount of time.

**Workpackage 2: Training**

INTRACOM S.A was responsible for the training of Control Applications staff. The training took place in the subcontractor’s laboratory facilities focusing on FPGA design/evaluation methodology. An open invitation existed by the subcontractor to CA engineers to sit with INTRACOM’s specialists on a regular basis and observe and be taught about the various options available. The training was complemented by on-the-job training in the areas of system design considerations, component selection, software design tools and software coding as well as in the test methods to be used. The outcome of this training stage was a first prototype.

**Workpackage 3: Specifications**

CA designed all the system specifications and the FPGA specifications in co-operation with INTRACOM. The technical specifications of the Linear CCD control system were clearly defined during this task. This task gave guidance to the involved engineers to successfully fulfil the experiment and was divided in the following subtasks:

**3.1 System Specifications**

An architectural study of the overall system and definition of the general functional specifications of the system were carried out. This task was accomplished by CA and involved the re-targeting of the existing design which was used discrete components into a Xilinx FPGA adding the new features. For the training stage a limited version of the final version of the system was considered sufficient which included only one colour (instead of three). Further improvements and the addition of the two other colours took the form of a follow up exercise in order to design the final system.

**3.2 FPGA Specifications**

This step included the definition of the overall circuit architecture and extraction of the functional specifications of the FPGA. This preliminary system design task was jointly
undertaken, but with the design subcontractor influencing the major technical decisions after discussions with the company engineer.

**Workpackage 4: Design and Fabrication**

4.1 FPGA design

The subcontractor used the results from the previous task in cooperation with CA engineers for the design of the FPGA. The VHDL models for each building block were developed and the XILINX CAD tools were used for synthesis and simulation of the design. The subcontractor provided training in the FPGA design process and in the methods of design interfacing adopted. This activity ensured that, in the future, the company engineer will be capable of carrying out similar tasks on their own.

4.2 System design

The company’s engineers were aware of the capabilities of the new technology when they set out to design a new system incorporating additional features which were considered imperative. One of the limitations of the new technology, as it was initially applied, was the requirement for the use of a serial EPROM in order to load the configuration file to the FPGA every time the system is reset. These devices (EPROMs) are one-time programmable (OTP), thus is limiting the flexibility of the system. This, coupled with their high cost, led the company to replace the EPROM with a microcontroller, which incorporates internal FLASH memory, and is reprogrammable in circuit. Some dedicated software had to be developed in order for any modifications of the FPGA to become a simple in circuit download. This additional effort was justified as it saved a lot of development time and money in comparison with EPROMS.

Finally, the new board was designed and developed. As previously stated it includes a RISK microcontroller in addition to the FPGA. The new board can also operate as a stand-alone module for simple imaging applications (mechanical measurements, simple quality control systems) as well as in parallel mode for more elaborate applications.

**Workpackage 5: System integration - Evaluation/ Testing**

In the final task the various system parts were assembled and the related functional tests of the integrated system were performed. The new board was placed in one machine, from the company, which was already operating with the previous system. Performance and output characteristics of the two systems were evaluated.
A full standard testing procedure was followed for the testing. This evaluation procedure split
the testing phase in two separate sections:

5.1. Laboratory tests.

In the laboratory tests phase, the hardware was tested in hard conditions in order to remove
all the design “bugs” from the new board.

5.2. Field trials.

The new system was then operated under real conditions in field tests in the phase of field
trials. The old control board was replaced by the new board in one of the rice sorters that the
company is producing. Rice sorters were considered the toughest test due to the nature of
their operation (e.g., contamination from the rice dust, etc.). In this way the normal operation
and proper function were checked as well as the verification of the initial system
specifications.

Additional review stages also included a prototype hardware review to ensure conformity
with cost and manufacturability requirements, and a final product review (including software)
to ensure complete information was available for production of the prototype.

After the successful testing, the system is now ready to enter the market.

Workpackage 6: Dissemination/Awareness

A final report was prepared detailing the rationale and results of the application experiment
following the latest guidelines concerning demonstrator document preparation. The First User
already participated in an international fair ‘PACKAGING 2000’, which took place in Athens
in March 2000. During this fair, considerable promotion of the new product took place and at
the same time it was a good opportunity to compare our product with those of the competitors
on a performance/cost basis. The results were encouraging. CA will also perform all
awareness and dissemination events organised by the Greek TTN or by the European
Commission on an international basis. Finally, during promotional visits to customers, the
improved features of the product due to the new technology will be mentioned as well as the
Commission funding.
**Figure 9.1: Planned and Actual Development Schedules**

<table>
<thead>
<tr>
<th>Month</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Task 1</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td>Task 2</td>
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<td>Task 4</td>
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<td>Task 5</td>
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<td>Task 6</td>
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</table>

**Table 9.1. Actual person days and subcontractor’s cost**

<table>
<thead>
<tr>
<th>Task No</th>
<th>Task Description</th>
<th>CA persondays</th>
<th>Subcontractor Cost (KEuro)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Planned</td>
<td>Actual</td>
</tr>
<tr>
<td>1</td>
<td>Technical management</td>
<td>25</td>
<td>17</td>
</tr>
<tr>
<td>2</td>
<td>Training</td>
<td>36</td>
<td>34</td>
</tr>
<tr>
<td>3</td>
<td>Specifications</td>
<td>44</td>
<td>38</td>
</tr>
<tr>
<td>4</td>
<td>Design and fabrication</td>
<td>72</td>
<td>76</td>
</tr>
<tr>
<td>5</td>
<td>System integration – Evaluation/Testing</td>
<td>25</td>
<td>20</td>
</tr>
<tr>
<td>6</td>
<td>Dissemination/Awareness</td>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td><strong>Total</strong>:</td>
<td></td>
<td><strong>210</strong></td>
<td><strong>191</strong></td>
</tr>
</tbody>
</table>

22
Knowledge Transfer process

The aim of this project was to transfer knowledge to our company and help us be able to replicate the process without the need of a subcontractor. But this does not mean that we intend to design and program an FPGA ourselves in the future without the need of an FPGA expert, but that we obtained training that took place in the subcontractor’s laboratory facilities focusing on the FPGA design/evaluation methodology, in order to observe and be taught on the various options available.

In this process, our company established links with the local TTN and started ‘talking’ a common technical language with the engineers of Intracom. It was very important for us to be educated in the FPGA terminology, since until now we had been only experienced in PCB design with discrete components. We worked with our subcontractor in such a way that it was possible for us to observe all steps and experience the actual design and testing of an FPGA. This was done by working together with the subcontractor on his premises and observing all steps taken to achieve the design and the testing of the chip.

Risk analysis

There was some technological and logistic risk for this project. The design of the processing FPGA was based on a functional model well understood and thoroughly tested by Control Applications Ltd. The transition of this functional description into a hardware model was a task that CEM handled repeatedly in the past and felt confident in transferring this know-how to other SMEs. The methodology and tools targeted for the design and implementation of the FPGA was a mature choice and the functional specifications have been used in many FPGAs produced by Xilinx. The FPGA design flow advocated by CEM and used to check a design before foundry sign-off was conservative and aimed at minimising the risk of producing non-functional FPGA due to design problems.

Another aspect of this project designed to minimise the risk of implementation was a proven implementation plan. Given the complete, fully verified, behavioural definition of the design developed by Control Applications Ltd., this plan allowed time for extensive simulations and testing to be performed to verify and validate the hardware design during each step in the design process.
10. Subcontractor Information

The selection criteria for the subcontractor were:

1. Previous experience in microelectronics, especially in designing and development: the Centre of Microelectronics (CEM) is the national industrial VLSI design and Testing centre in Greece and also acted as TTN centre for Greece (FUSE I). It promotes R&D activities in the area of VLSI design for INTRACOM's needs and simultaneously provides similar services to Small- and Medium-sized Enterprises (SMEs). CEM's main activities include System Design, VLSI Design, FPGA Design and migration to ASIC, Prototype Testing and System Production. CEM has currently designed over 50 ASICs for telecommunication applications, image processing and power control applications. In addition, it has gained a lot of experience in offering consulting services to local SMEs, universities and research institutes.

2. Equipment and training potential: CEM is equipped with state-of-the-art facilities including powerful HP-700 series workstations running MENTOR GRAPHICS CAD tools for schematic capture/VHDL design entry, digital and mixed mode simulation, logic synthesis, layout, automatic test pattern generation, Digital Signal Processing, ELDO analogue simulation S/W by ANACAD, technology and vendor independent libraries, TOPAZ V digital tester running at 110 MHz for testing digital ICs up to 160 pins, LTX-90 analogue tester for analogue and mixed signal ASICs, FPGAs development tools by XILINX and TEXAS INSTRUMENTS and also PCB design using MENTOR GRAPHICS CAD tools and P-CAD. System production is provided using UNIVERSAL assembly machines, Robotic Systems and computer-aided testing equipment. In addition CEM was able to provide training throughout the prototype development.

INTRACOM was participating in technical meetings of project working groups on demand of the Project Manager of Control Applications Ltd whenever it was necessary and depending on the technical aspects that were to be examined. Furthermore, per a joint agreement, INTRACOM informed the project manager of CA about the work progress on a monthly basis or on demand.

A contract between CA and INTRACOM was signed for the training and the design of the FPGA. The contract describes the obligations of both parties concerning deliverables, payment terms, monitoring of the design procedure, the timeframe of the project, the acceptance of the work done by the subcontractor, the ownership of the results and the
termination of the contract. In addition, jurisdiction terms and the means for changes in the contract are laid out.

11. Barriers Perceived by the Company in the First Use of the AE Technology

CA’s core technical skills are problem analysis and specification as well as the design and development of innovative solutions for industrial automations. Until now, the company did not have any experience in design methodologies adopting CPLD or FPGA technologies. Thus the company faced several initial barriers in adopting microelectronics technology. These barriers included:

i. Knowledge Barriers -

CA’s development skills are mostly traditional, thus analytical design and knowledge of the capability / cost trade-off for the new electronics technologies were not available within the company. Whilst the company was aware of the enhancements it desired for its products, the company was not in a position of being able to assess the feasibility of the new microelectronics technology in delivering these benefits. The company was particularly deficient in the ability to assess the cost of the microelectronics system required to deliver these benefits. The company’s ‘feel’ was that the adoption of the technology would be impractical with respect to cost development time.

Knowledge barriers also existed in evaluating technologies and technical advice, which further disposed the company to be reluctant to use the new microelectronics technology.

ii. Psychological Barriers-

The adoption of the new microelectronics technology required the company to overcome several psychological barriers including the perception involving high risk and high development cost. In a market where product reliability is a key factor, CA viewed the adoption of the new microelectronics as potentially being a high risk venture. The adoption of alternative product improvement strategies based on more intensive microcontroller applications was preferred.

iii. Technology Barriers -

The company did not possess any expertise in design or dedicated software development (VHDL code) for the new devices. Thus there existed several technology barriers including inexperience in electronic design project management, lack of electronic hardware and
software design skills, lack of development and manufacturing knowledge for the new systems and a lack of knowledge in selecting appropriate component vendors.

These barriers meant that prior to the FUSE programme the company had not seriously considered the new microelectronics technology as a method of improving their products.

12. Steps Taken To Overcome The Barriers And Arrive At An Improved Product

The driving force to overcome the barriers was the objectives, which were set from the very beginning. After the initial approach by the TTN and studying the published promotion material for the FUSE programme, one target was set. The new FPGA/CPLD technology could add the flexibility to the company’s products they were lacking. Thus production costs and time allocated for each application could be greatly reduced. The cooperation with an experienced training subcontractor, INTRACOM, was considered a great opportunity offering the initial guidance for getting into the new technology, which the company was missing. The viability of an electronics solution from a cost and risk perspective was only delivered as a result of this activity.

The knowledge barrier was addressed by initial training in technology selection, costing and planning provided during the feasibility study, and the development of a plan for technology support and knowledge development to be conducted during the application experiment. This lowered the initial barriers and the provision of formal training courses for the engineers and ‘on the job’ training conducted by the selected design subcontractor throughout the application experiment eradicated the technology barriers.

The psychological barriers related to the perception of high risk and costs involved were reduced by the quantification of the relatively low investment costs in hardware and software support tools required for a FPGA/ CPLD product development. Also, the possibility of compensating for minor design errors by software corrections in a low cost and timely fashion was a big advantage. Finally, the natural reluctance to enter into the new technological field was removed by the assurance of cooperation by the subcontractor.

Technology barriers were overcome during the application experiment by the purchase of design tools, engineer training in their use, consideration of production issues during initial design stages and through continued training. The viability of an electronics solution from a cost and risk perspective was delivered only as a result of this activity.
The most important factor, which contributed to the final decision, was the flexibility of the new designs and their adaptability. Only the consideration of the integration scale that could be achieved as well as the possibility to finally produce a single board adaptable to all of the company’s imaging requirements made any effort and risk justifiable.

13. Knowledge and Experience Acquired
The original expectations of the knowledge and expertise gained during the application experiment was to gain the following skills:

- Skills in the use of the support hardware and software development tools.
- Software development (VHDL coding) design skills.
- FPGA/CPLD system fault isolation and localisation expertise.
- Technical management skills in the specification and project management in FPGA/CPLD based product developments.
- Component selection skills, including the awareness of component trade-off decisions in designing hardware systems.
- Printed circuit board test methods.
- The development of new supplier bases for the company, the management of these and the management of the impact of electronic sub-assemblies of the production processes in the company.

In general most of these skills have been acquired, but the capability to design a complete system without subcontractor support has not yet been developed. The company can undertake minor design modifications to the product developed during the application experiment, but would require subcontractor support in the development of optimum system design solutions, design partitioning and in the area of printed circuit board layout design.

14. Lessons Learned
The company’s first use experience of FPGA/CPLD product development highlighted several issues, which will be absorbed into the design approach to be adopted for future product developments. In particular the company would advise that in future FPGA/CPLD product developments that:
1. Prior to the start of the product development, a clear statement of the corporate objectives for the development should be prepared and agreed on. Although minor modifications of the initial design are possible, it saves a lot of effort and cost to clearly define the development objective in the very early stages of the project.

2. The specification of a FPGA/CPLD product development introduces many more possibilities than simpler systems of analytical design, and therefore the time allocated to the specification stage should be extended by at least a factor of 3. The company originally allocated 2 weeks to the product specification phase for what initially seemed a simple transfer from one technological solution to another in order to include all possible future enhancements. Specification preparation should not be underestimated, and the time invested at this stage will ensure a better product.

3. The original specification included items that were considered desirable by the company and seemed feasible at the time such as pixel and background correction as well as noise cancellation. In the final design more features were included which made the product even more flexible and reliable. The product specification should be structured so that if a cost target is provided, the design requirements are classified as mandatory or desirable to enable value assessments to be made at the original system design phase.

4. The initial circuit schematic indicated that the component count for the prototype unit was not high. This allowed the design of a much more simplified printed circuit board which was incorporating features of much more complicated systems. Also taking advantage of the ability to allocate the device pin-out according to the user requirements the printed circuit board layout was even more simplified. The resulting board is so simplified and capable of performing so many functions that the total effort was justifiable.

5. Selection of the development tools as a result of the recommendations of the training supplier and design subcontractor resulted in a good experience in their use by the company. It is advised that such third party advice is obtained prior to development tool purchase.

15. Resulting Product, Its Industrialisation, And Internal Replication

The prototype board is already a fully functional product, requiring minor modifications in order to become a fully industrial product.
We already approached one of our customers and replaced his existing control boards with the new ones. This particular customer has three of our rice sorters as well as two rice sorters from our competitors.

Two new machines, one for nuts and one for fruit cubes, which are going to be delivered in May, are also going to be equipped with the new boards.

Any feedback for possible bugs from these installations is going to be evaluated immediately such that by the end of June all the necessary steps will have been taken for a fully industrial product.

The remaining stages for a fully industrial product are:

a. Correction of any software or hardware bugs (if they exist) max. 2 weeks
b. Design of the final boards and supplier identification for PCBs as well as for the components max. 2 weeks
c. Compliance testing of the final boards max. 1 week
d. Possible agreement with an assembling company in order to assemble the PCBs

The total costs for industrialisation are estimated at 5,000 Euro.

16. Economic Impact and Improvements in Competitive Position

Market research has proven that there is a growing need for quality control systems in the Greek market because of the quality standards of EU and globalisation of market.

During the last fiscal year, the company’s activities were mainly focused on the research and development of a new rice sorter. Due to the good references made with existing systems, the company has already contacted marketing companies specialising in machinery sales. These companies forecast a high export potential. The following figure presents the actual sales of the existing product in recent years and the forecast sales of the new product.

![Chart showing sales comparison](chart.png)

*Figure 16.1. Existed sales since 1996 and Projected sales up to 2003*
As stated previously, the existing products required tedious and elaborate set-up. This factor greatly limited the marketing capabilities of the product. In contrast, the greatly simplified procedures of the new product allow the company to focus on sales activities. In addition, the range of applications to which the AE product applies is very wide and this is another factor in the optimistic sales forecast.

A comparison between the existing and the new technology in terms of cost per system is as follows:

<table>
<thead>
<tr>
<th></th>
<th>Standing technology</th>
<th>new technology</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set up</td>
<td>5 days = 715 Euro</td>
<td>1 day = 143 Euro</td>
<td>572 Euro</td>
</tr>
<tr>
<td>Maintenance</td>
<td>3 visits (during the guarantee period) = 1,650 Euro</td>
<td>1 visit = 550 Euro</td>
<td>1,100 Euro</td>
</tr>
<tr>
<td>Electronics assembly</td>
<td>10 days = 1,430 Euro</td>
<td>9 days = 1,287 Euro</td>
<td>143 Euro</td>
</tr>
<tr>
<td>Component cost*</td>
<td>11,000 Euro</td>
<td>10,500 Euro</td>
<td>500 Euro</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>14,795 Euro</strong></td>
<td><strong>12,480 Euro</strong></td>
<td><strong>2,315 Euro</strong></td>
</tr>
</tbody>
</table>

*Reduction of component cost due to much lower component count and the much simpler and smaller PCB.

The table (previous page) presents only the quantities that can be numerically estimated. There are also additional parameters that cannot be expressed in absolute numerical terms but they influence positively the final benefit. These are:

- the increased reliability of the proposed systems due to lower component count
- the increased market potential (especially export potential).

From all the above-mentioned points it is obvious that the new technology has significant economical advantages in comparison with the previous one.

**ROI**

The following table summarises the return on investment calculation. Without taking into account the additional system value due to the improved technology, the additional profit per unit has been already calculated at 2,315 KEuro (Table 16.2)
Projected Sales for the next 4 years (Fig. 9.1) | 90 units
---|---
Additional Profits due new technology for the next 4 years | $90 \times 2,315 = 192,2$ KEuro
Total Investment covered by the project | 52,800 Euro
Return on Investment (ROI) | 364%

**Table 16.2. Return on Investment table**

The payback time is calculated by dividing the *Total Investment* covered by the project by the *per unit savings in cost* and results in 23 machines (sorters) which are forecasted to be sold in 15 months. We have estimated that the administrative and functional expenses will be about 10 KEuro. Thus, the payback period is estimated to 15 *months*.

The main advantages of the new technology have been already presented in the previous analysis in terms of cost reduction per system.

A quantity of 23 units should be sold in order to compensate for the new investment. From Figure 16.2 it is obvious that these units expected to be sold in about 15 months.

17. **Target Audience for dissemination throughout Europe**

The target audience consists of companies in the sector of Industrial Process Control Equipment (Prodcom code 3330), which is the industrial sector of the improved product. However, it can also be used by companies of Prodcom code 3340 (Optical Instruments and Photographic Equipment) and of Prodcom Code 3320 (Instruments and Appliances for measuring, testing and checking).

The target audience will include the Technical Managers, Product Development Managers, and Chief Executives of small- to medium-sized enterprises (SMEs) in these manufacturing sectors, especially those run by few people, one or two engineers, a manager and an accountant.

In addition, the experience that the company gained after carrying out the experiment would be useful to companies with electronic engineers having skills in the domains of image processing, industrial applications development, s/w design and development and production automation. Such companies face knowledge and psychological barriers and, while they know the desired improvements for their products, they believe that the cost is too high for them to incorporate microelectronics technology.