

FUSE demonstrator document**FUSE Application Experiment EPC1 EU No. 23086****Monitoring TTN: IAM F&E GmbH, Braunschweig, Germany****SMART OPTICAL SENSOR**

Mixed signal ASIC-based photo sensor allows cost reduction of more than 50%.

Abstract

VISOLUX Elektronik GmbH is one of Germany's leading companies for development, production and marketing of a wide variety of non-contact sensor systems. VISOLUX is a manufacturer with high quality level and excellent performance. The main business is in the sector of opto-sensors. The company sells its products world-wide. Our customers mostly are OEM's, operating in the markets: Industrial Automation, Material-Handling, Move and Traffic, Safety. The products are used in automation of industrial applications like folding machines, filling machines and others.

The aim of the application experiment is to start using Mixed-Signal ASIC technology, to improve competitiveness, to overcome barriers which have prevented the company to adopt new technologies, to enable the company to replicate the experiment and to gain knowledge and experience in the new technology.

The results are to see in a new improved product and in the increase of certain know-how. The existing product is a photo electronic sensor. The used technology is standard assembly of discrete components on PCB's. The existing products are too expensive to manufacture and not longer competitive in their market:

With the new developed Opto-Asic a cost- reduction and size-reduction with more than 50 % is possible. But the use of a special transparent package is absolutely necessary, which is not a standard-package.

The size-ratio for the mixed signal ASIC are about 25 % for the photodiode, 55 % digital and 20 % analogue.

This AE has its general benefits in realising of innovation, economically we expect increased profits. The forecast for the payback period will be approx. 16 month and the estimated ROI will be about 1700% for a 5-year period.

The increment in capability is the decrease of the "time to market".

The costs and duration of the AE have been approx. 77 K€ and the time of the project was 10 months to come to functional prototypes.

Keywords

Mixed-signal ASIC, photosensor, photodiode, transparent package, switched capacitors amplification, opto-electronics, packaging, sensor

FUSE-Signature

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1. Company name and address

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VISOLUX
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2. Company size

The total number of employees is 340 with 12 involved in the electronic development.

The company is structured in 4 Business Units: 1. Industrial Automation, 2. Material-Handling, 3. Move & Traffic, 4. Safety. Production facilities are in Berlin, Baden-Baden, Stahnsdorf and Switzerland. 10 subsidiaries and more than 25 representatives are responsible for world-wide sales.

The turnover of the Visolux-Group is about 60 M €. The turnover of Visolux sensoric is about 40 M€. The number of persons of the Visolux-Group is about 450 persons.

3. Company business description

VISOLUX designs, produces and sells sensors and is a supplier of a complete program including photo electronic-, inductive-, capacitive-, ultrasonic- and radar-sensors, control systems, bar-code reading- and identification-systems, laser distance measurement and data transmission systems, to name just the most important products. Approximately 6000 different articles are available products.

The company's current involvement in electronic system design are in the industrial sectors of industrial process control systems, machinery electrical and optical equipment and transportation services. Main activities are in the PRODCOM 3330 sector 'Industrial Process Control Equipment'.

The company's full-service philosophy is not just selling products but to sell problem solutions. This philosophy needs flexibility and innovation to be successful in today's market.

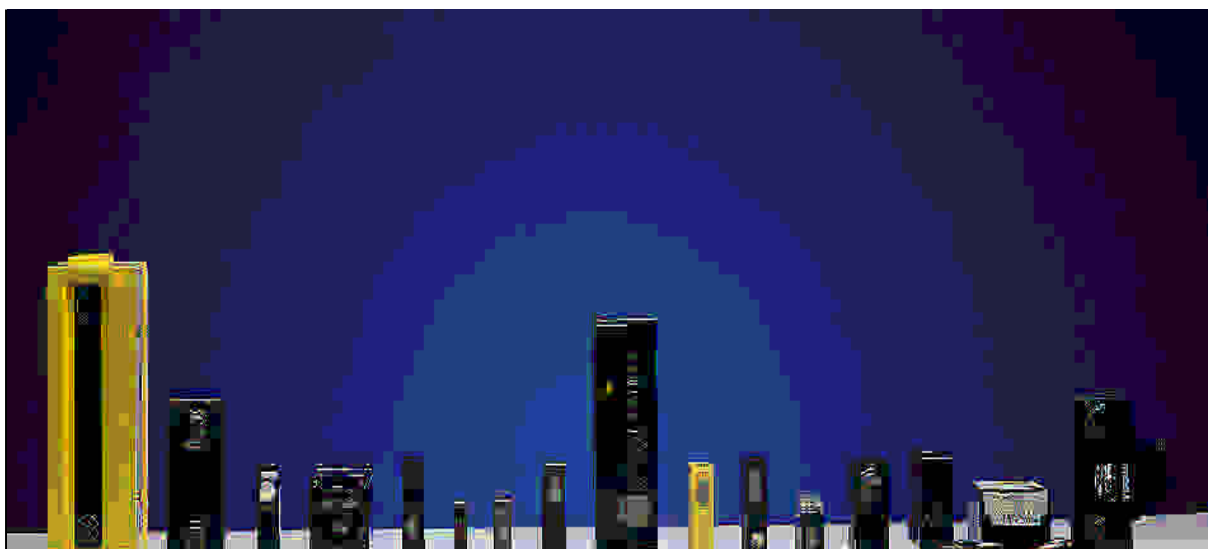
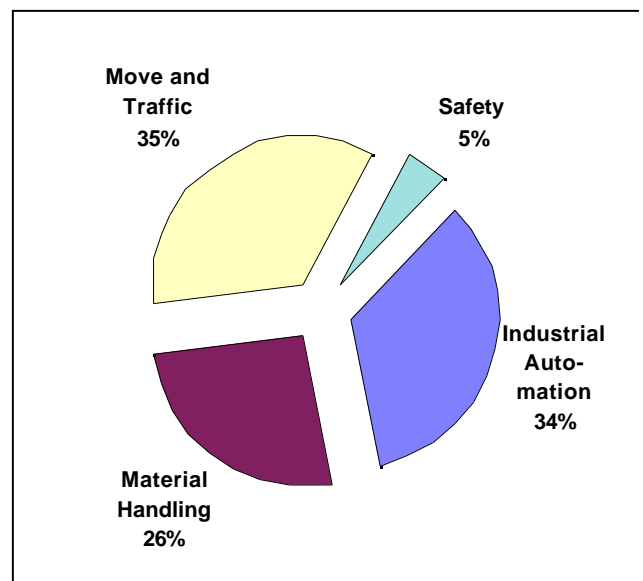
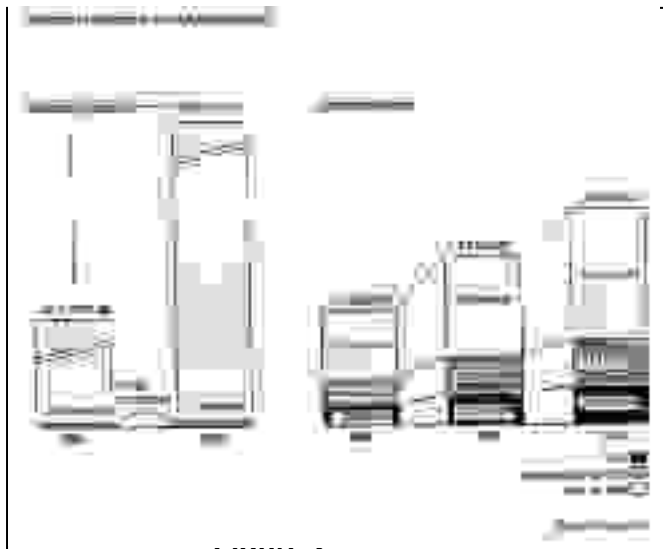


Figure 1 shows the company's range of products.

4. Company markets and competitive position at the start of the AE

The company delivers to the sensor market world wide. Our customers mostly are OEM's, operating in the markets: Industrial Automation, Material-Handling, Move and Traffic, Safety.



The world market for sensors, is an important and increasing market. The sensor market Germany/Europe is expected to grow annually with 8 %. The special area for photocells only will increase until the year 2000 up to 1.4 billion DM.

The relations between Germany, Europe and the rest of the world are shown in the above left side picture (Figure 2). On the right graph (Figure 3) you can see the company's markets in the different sectors.

Besides our home-market Europe, the US-market is one of our main targets, because of a big backlog demand in the automation sector. In this sector we operate with the small housing-products like the ML4-KSU-family which is the product to improve by the AE. Currently the device costs about 50€, but competition requires to lower costs and reduce the size. The strengths of this product family have been performance, quality and small size, however, a separate control unit was required. International competition with low prices caused an annual decline of sales figures of about 10% over the past years.

VISOLUX offers the most complete program for solving customer problems. This includes special customer designs as well as standards.

The technology of photocell sensors changes to smaller housings, intelligent processing and interconnection with PLC through fieldbus systems.

To continuously increase our market share over the complete scale of the program we do want to lower our production costs, especially for standard products. The companies market share in Europe is 10 %, in Germany it is approximately 30%. In order to internationalise the business, i.e. to open new markets in the world and maintain or improve our position against international competition in our old markets, we need to improve our organisation as well as our technology base.

Our competitors in Germany are mainly two big producers of opto sensors which are acting in the same market sector. The one of both is exceptional bigger than our company and offers the more innovative product in comparison to the product to improve. That company uses already ASIC's and the products are small sized, compact, of high quality standard and they can beat the prices. The market prices generally are decreasing about 10 % per year.

5. Product to be improved and its industrial sector

The product to be improved are small photoelectric sensors out of the ML 4-KSU-family, consisting until now of a separate sensor head including the optical components like transmitter, light-detector with preamplifier, lenses and housing connected via cable to a feeding and supplying control unit (KSU).

This control unit provides the sensor head with energy, operates the heads signals and gives the outputs to the customers following circuitry (see figure 4).

The VISOLUX-sensor-heads are strong in the market. The success of this product family in the past based on their performance, quality and small size, but the market demands more and more miniaturised sensors **without** a separate control unit. It could be considered a major technological advance if the entire device could be fitted into the housing of the current sensor.

That means, it is necessary to reduce the number of components, to integrate the electronic circuitry and to use only one small PCB (printed circuit board) to put into the sensor housing.

Therefore an ASIC is required and the only successful solution, that allows to incorporate most of the single components inclusive the control circuitry into the smallest sensor head itself.



The technical specifications of the existing product can be devised into three parts and main spec.'s are:

I. Optical principle and optical parameters:

- I.1. Retroreflective light-switch (infrared LED) with polarisation filter as well (red LED) and an operating range (depending on the reflector) from 0 ... 400 mm.
- I.2. Retroreflective light-scanner with a scanning range from 5 ... 35 mm (on white paper).
- I.3. Retroreflective light-scanner with background suppression and a scanning range from 10 ... 20 mm (on white or black paper).

II. Electrical functions and parameters:

- II.1. Supply voltage from 10 ... 30 VDC.
- II.2. Electronic output stages (NPN,PNP) short-circuit protected up to 200mA.
- II.3. Indicator LED, light/dark switching selection (more features see figure 7).

III. Mechanical features and outlines:

- III.1. Plastic sensor head: 30x 15x 12 mm. Plastic control unit (KSU): 64x 41x 20 mm.
- III.2. Protection category: Head IP 65, control unit IP 50.
- III.3. Type of connection: 2 m fitted cable (plug connector available).

The product is used primarily in industrial applications (folding machines, filling machines, ...) where a precise response time is needed.

Figure 5 shows the Block-Diagram of the product to improve (ML4-8-KSU), consisting of **two device parts**, which are connected via cable.

The number of single electronic components is 66, the manufacturing process is obviously very complicated and expensive, most of all it's a big disadvantage for the customer to install the two-parted-sensor into his machine-application.

Also a shielded cable from the sensor-head to the KSU-box is necessary, because only for a pre-amplifier is enough space in the head of the ML4-KSU.

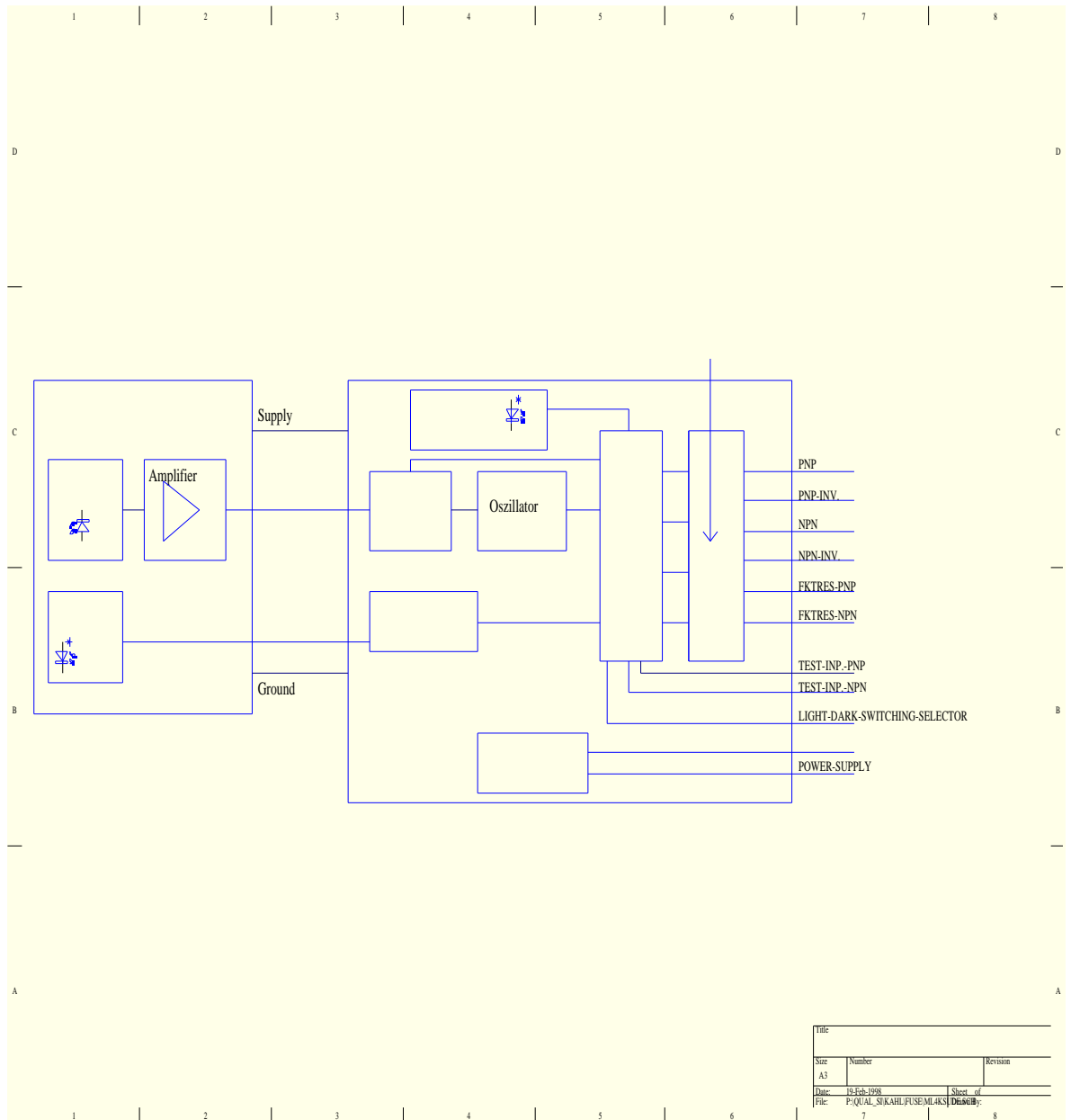
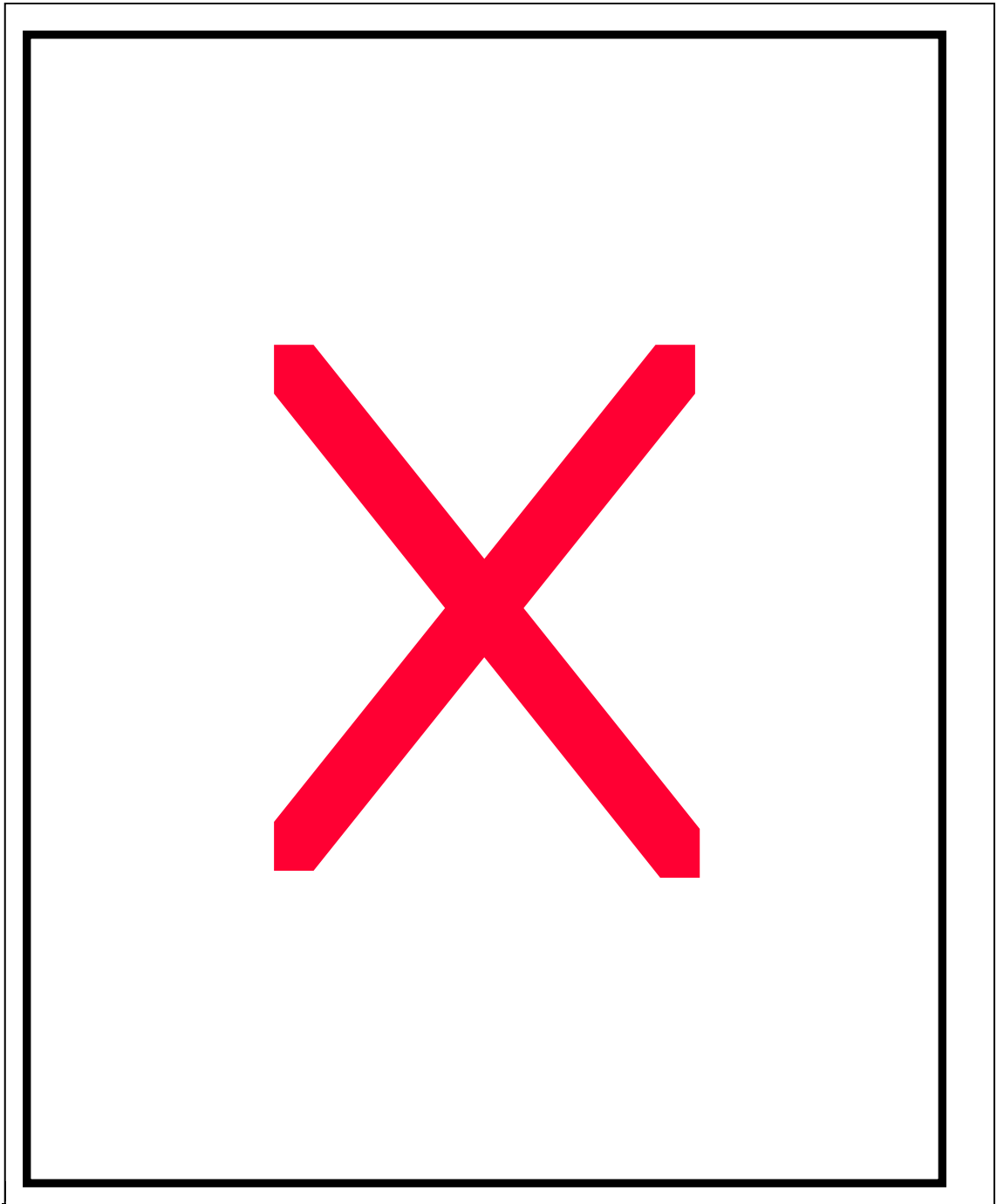


Figure 5

Brief functional description of the system (**Figure 5**):

The pulsed infrared signal of an LED will be reflected by the object (paper), arrives at the photo diode and gets amplified in an analogue circuitry. Then this signal gets to the detection unit, comes to an integration & counting stage, is compared with the own transmitter frequency in a logic circuitry and drives the indicator LED as well as different electronic output stages.

The PCB of the KSU-Box is shown on figure 5.1.



extra sensor-head.

6. Description of the technical product improvements

The new product, the **Smart Optical Sensor**, realised in a prototype, fulfils the following projected demands:

- easy interfacing with PLCs due to increased functionality
- increased accuracy due to performance enhancements;
- easier mounting due to reduced size;
- lower production effort and cost by 50% due to reduced component count;

- wide range of applications due to improved EMC;
- improved reliability, especially when mounted to moving parts due to less solder points on the PCB;
- improved quality due to fully automated assembly by using pick & place automates;
- higher flexibility due to integration of optional features (only one PCB-layout covers different possibilities) like for example light/dark switching select, indicator LED with flashing mode for function reserve indication, definite power on behaviour, chip enable (sleep mode);
- higher category of protection against environmental conditions (IP-rate, vibration, shock);
- Higher customer satisfaction due to decrease of delivery time to less than a week because of less logistic efforts;
- Low-cost cabling instead of expensive shielded cabling for connecting the sensor due to functional enhancements of the ASIC.

A further advantage is to see in the certification of the product. In some product norms (-standards) it is necessary that each single component has a definite environment-conditions-standard and so with less components it's much easier to find out.

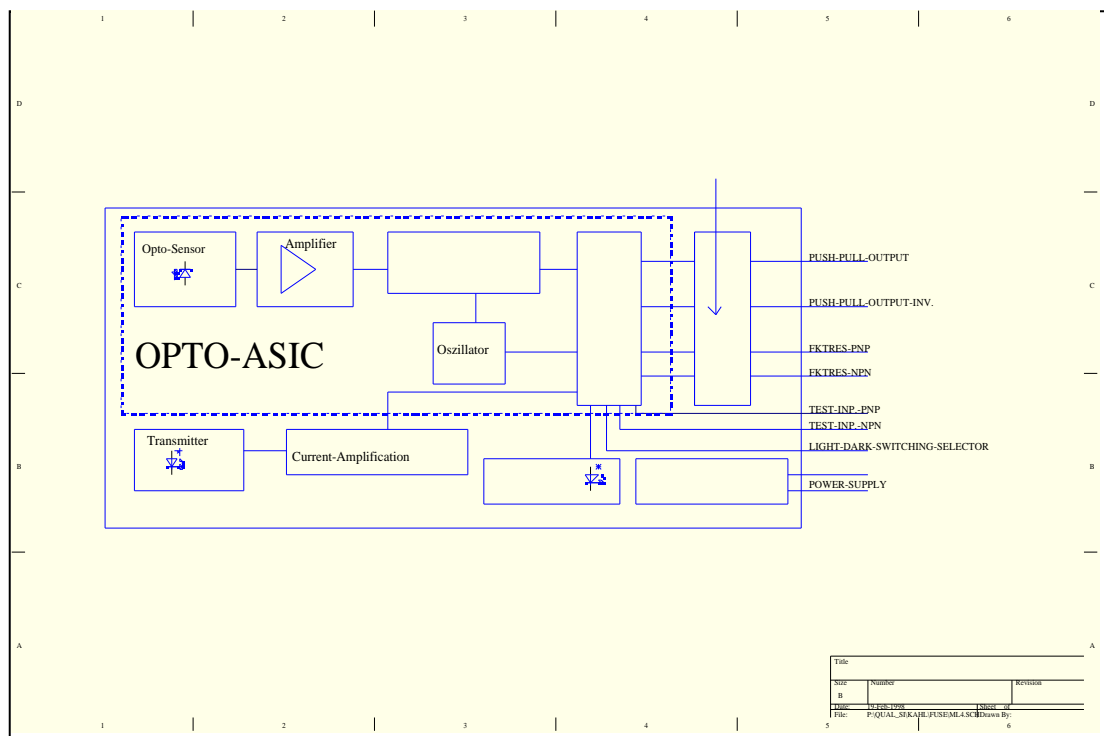


Figure 6

Figure 6 shows the Block-Diagram of the realised **Smart Optical Sensor** with the developed ASIC. Many functions are integrated and the control-outputs for the external components are fitted in the ASIC.

The modules used in Figure 6 for the developed ASIC are a switched capacitor amplifier, a photodiode, a Signal detection unit with a Schmidt trigger and perhaps a counting-stage of receiver impulse, logic for handling the outputs and a oscillator for control the transmitter. The signal of the photodiode is only about 1 nA (depends on the application) and the handling to detect it, with a good and required suppression of disturbances like EMC and ambient light, requires special analogue and digital filters which can be in an economic way included in the ASIC.

One extra input was added to couple an external photodiode with pre-amplifier to the amplifier in the ASIC, since in some cases larger photodiodes are needed.



Figure 7

Figure 7 shows the pictures of the prior product, the sensor head with fitted control unit (cable is covered) on the right side, in comparison to the new **Smart Optical Sensor** (left side) and figures out the quantum jump we made.

Figure 7.1 shows the ASIC-chip in a 16 pin housing (SOIC 16) on the PCB. It is possible to look into the integrated circuit because of the transparent plastic housing. The size of the improved Product ML 4.1 are 25 mm x 18 mm x 13 mm.

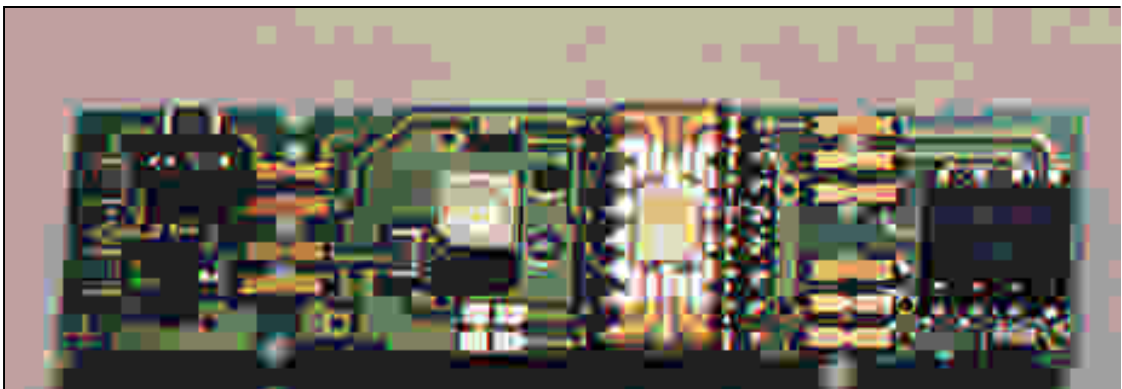


Figure 7.1: PCB of the improved Product. Only 10 ribs with two Wings are necessary in comparison to 24 ribs and 5 Wings of the PCB without Use of the developed ASIC.

The size-ratio, as mentioned before, for the mixed signal ASIC are about 25 % for the photodiode, 55 % digital and 20 % analogue. The use of a special transparent package is absolutely necessary, which is not a standard-package.

The Chip-Size of the ASIC is now about 6 mm² in 1 μm CMOS process and has actual 19 pins.

In the too improved Product one solution with standard cells and one solution with a mixed signal ASIC have been made. A picture of the SMD based solution with 6 folded small boards are shown in figure 7.2. The solution with standard cells contains 75 components and 7 folds of the boards. This solution is absolutely not so good as the ASIC based solution, especially in terms of manufacturing and cost.



Figure 7.2: Printed circuit board of the to improved product. Also a special EMC-shielding over that complete board is necessary to get sufficient EMC-results (s. Figure 7.3)



Figure 7.3: Folded PCB with EMC-shield.

7. Choices and rationale for the selected technologies, tools and methodologies

The most important requirements for technology selection have been a major size and cost reduction. Size reduction should allow to fit the entire device into the sensor housing of the current device. Cost reduction should allow to build devices at least 30% less expensive.

For implementation SMD and mixed signal ASIC have been evaluated. The SMD approach allows sufficient reduction in size but requires high production effort. Please refer to figure 7.3 with the folded PCB. Mixed signal technology on the other hand allows to integrate all functions into a single device. Size reduction is well sufficient to fit the chip into the housing, production effort can be reduced and quality increased.

We choose to fabricate the component in a double metal layer 1.0 μ CMOS process. The reason for choosing this technology is the relatively low cost of the manufactured chips. The first fabrication run is realised as MPW-run (multi project wafer) together with other projects. The conditions offered with the minimum costs are 2.500 €. This includes also the first 5 sqmm. chip area, additional area costs 250 € / sqmm. Taking these rather low costs into account, different versions of the chip can be investigated.

More than that, we expected knowledge and experience of integration of photo-detectors, the analogue capability and performance of the used S-C-circuitry (switched capacitors).

Alternatively the BICMOS, FPGA and Microprocessor-Technologies have been discussed but we decided finally to use CMOS-ASIC because with this technology we got an optimum of advantages. The main points are listed in the following table:

Choice	Advantages	Disadvantages	Price-situation/Remarks
Discrete solution (SMD)	Technology & components available	Lot of components (75 + 25 ribs)	High costs, expensively production and assembly
Opto-ASIC (Mixed signal CMOS *)	Less components (24 + 10 ribs)	Design tools are not available.	Low costs in the production per Sensor with the ASIC.
FPGA	Flexibility	Analogue circuitry is not possible.	High costs per sensor relative to the solution with an ASIC.
Micro-controller	Flexibility (Software)	Much components are necessary because analogue components must be additional used.	High costs per sensor relative to the solution with an ASIC.

* The realised ASIC have only full custom analogue cells. The possibility of choosing BICMOS were rejected because of the price and the possibility to overcome the disadvantage of CMOS with the full custom analogue cells.

We choose to design the system a top-down and iterative a bottom-up design methodology, using the Cadence-design-system with network simulator (Spectre). The reason for choosing this methodology is the high sensitivity of the analogue parts of the IC combined with sophisticated strategies of digital signal processing on the same chip.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

The company has expertise in development and production of opto-electronic devices (retro reflective light switches, -scanners, single path light barriers and control-units) and the biggest experience in manufacturing and assembly of complete sensor systems is based on more than 50 years to be in the business. The electronic design expertise incorporates PCB-layout, discrete analogue and digital circuits. The testing after assembly is done by self developed and self produced test equipment using more or less discrete devices and PC's/ micro controllers and mechanical test fixtures.

We don't have experience in the design of Micro-controller and integrated circuits, we just use available standard components from different manufacturers.

To develop the capability of the design and the use of **Application Specific Integrated Circuits (ASIC)** in our company, is the target issue to participate in the FUSE-project. The discrete technology has limits in the way that very small housings cannot be realised.

For the project we allocated personnel with technological experience in discrete analogue and digital design and from the production department to the team. By allocating senior engineers it was assured that the experience can be replicated with other products. During the key phases specification, training and design 8 engineers have been involved with different effort of person days.

9. Work plan and rationale

The project can be divided into single subtasks (activities) which follow the standard flow of design, fabrication and test.

Figure 8 shows the detailed work plan we followed during the AE.

Activities	Month											
	1	2	3	4	5	6	7	8	9	10	11	12
1. Management												
Project management	X	X	X	X	X	X	X	X	X	X		
Dissemination			X							X		
Reporting	X	X	X	X	X	X	X	X	X	X		
2. Specification												
Functional specification of system	X											
System specification of component		X										
Technical specification of component		X	X									
3. Training												
Management training												
Specification training	X	X										
CAD training		X	X									
Design training		X	X	X								
Evaluation training				X								
4. Design												
System level design			X									
Subsystem level design			X	X	X							
5. Evaluation												
Prototype production					X	X	X=>					
Test set-up							X=>					
Functional testing							X=>	X	X			
Prototype testing								X	X			
Field testing									X=>	X		

Nearly all of the work packages have been realised as planned, only the tasks: Prototype production, test set up, functional testing and field testing listed (see mark =>) in work package No. 5 Evaluation, had a delay for one month each. The reason for this delay was because the prototypes of the component have not been available at time (subcontractor).

The project was divided into 5 main task phases as follows:

WP1: Management

Visolux Perform project management tasks, controlling and reporting. This also included preparation of documents for possible internal replication of the new technology.

Subcontractor Give advice and support

Duration: 10 month
 Visolux effort: 20 person days
 Subcontractor cost: none

WP2: Specification

Visolux Provide specification of new product, define the verification and tests.
 Subcontractor Give advice and support, add technology-specific aspects to the specification, check feasibility.
 Duration: 3 month
 Visolux effort: 20 person days
 Subcontractor cost: 8.9 k€

WP3: Training

Visolux Attend general training classes on mixed signal ASIC technologies, design flows and design tools.
 Subcontractor Supply training measures.
 Duration: 4 month
 Visolux effort: 30 person days
 Subcontractor cost: 6 k€

WP4: Design

Visolux Implement the specification.
 Subcontractor Support for critical parts, check correctness of description .
 Duration: 3 month
 Visolux effort: 40 person days
 Subcontractor cost: 16.8 k€

WP5: Evaluation

Visolux Test set-up and verification of ASICs.
 Subcontractor Fabrication of the chip as MPW (multi project wafer).
 Duration: 6 month
 Visolux effort: 25 person days
 Subcontractor cost: 9.5 k€

This workpackage has been delayed by one month because prototypes were delayed.

The effort on person days for VISOLUX to each single work package had been: Management 20 days, Specification 25 days, Training 30 days, Design 40 days, Evaluation 25 days. The effort on person days for the subcontractor to each single work package had been: Specification 37 days, Training 25 days, Design 60 days, Evaluation 40 days.

Work Package	First User [<i>person-days</i>]	Subcontractor [<i>k€/person-days</i>]	Total [<i>person-days</i>]
WP 1 (Management)	20	None	20
WP 2 (Specification)	25	8.9/37	62
WP 3 (Training)	30	6/25	55
WP 4 (Design)	40	16.8/60	100
WP 5 (Evaluation)	25	9.5/40	65

Knowledge transfer was done during general training measures in the training workpackage but also during training on the project in workpackages design and evaluation. Visolux had the chance to conduct own experiments with most design steps and discuss results with the subcontractor.

In order to minimize risk, MPW were planned to produce the ASIC samples. The first MPW run was done with a smaller Chip-size and not all digital functions were implemented. It was expected that at least two MPW runs would be required in the project. The second MPW run included all the functions. The analogue part worked fine, but the digital part was not fully compliant with the specification.

10. Subcontractor information

VISOLUX has selected the subcontractor for the following reasons:

The ability and agreement in the objective of transferring knowledge via a co-operative development process.

The subcontractor has expertise of the design and series fabrication of mixed mode circuits under one roof.

The designers have full knowledge of the processes of their own foundry.

They have experiences in characterisation and design of photo-detectors integrated into standard (CMOS) full custom ASIC's. The subcontractor also could provide one special transparent package from an external supplier.

The subcontractor co-operates with another silicon foundry, as back up production for reliable delivery to their industrial customers.

The offer of this subcontractor for their efforts in the design process and costs for delivery was considerable better than others.

They are able to simulate the design result completely by network simulation (Cadence/Spectre). This minimises the risk of failures and the necessity of a redesign.

The flexibility and ability to deal with small projects and to reach the time targets.

To be available at any time (phone, fax, e-mail, visit).

VISOLUX is going to conclude a detailed framework agreement (15 points) with the subcontractor wherein all the relevant relations between supplier and customer are confirmed. Some of these points are: IPR-links, order & delivery methods, prices, quality & test procedures, penalty clauses, warranty agreements and so on.

Hints for an optimum of collaboration and to avoid misunderstandings.

It is necessary to prepare all the meetings with the subcontractor very detailed, to write down all the parameters and tolerances and to have written agendas and protocols.

11. Barriers perceived by the company in the first use of the AE technology

There were different barriers in our company to accept the new technology and which have blocked to use ASIC's. The main barriers are:

Knowledge barriers:

Due to the increased competition in the area of industrial automation where the product is sold, VISOLUX knew that there is a need to improve this product. We realised that if we don't innovate the existing product their will be no further success in the market.

But we didn't know how to find out what the possible solutions are and what technology should be chosen.

We had the understanding that the product has to be minimised, but how to manage?

Psychological barriers:

It is the genuine fear to risk a new technology in a range you are not familiar with and to depend on a subcontractor. Some engineers were thinking that there is a better flexibility in development of new products if discrete components are used, because they are always available and there are no creating limits.

The belief of high risk and to depend on only one main component to realise the product, to be responsible if there are problems coming up e.g. quality is not as expected, or the availability of the component is not guaranteed, explains the main psychological barriers.

An other barrier is the resistance to change the well known technology and to go into unknown areas.

Technology barriers:

The lack of knowledge in the use and development of ASIC's has manifested itself in technology barriers that have contributed to the overall difficulties of introducing a new technology. Not to know how to specify the requirements due to the technology and skill shortages of design rules or test procedures have been the main technology barriers.

Financial barriers:

There existed the belief that high investment costs are necessary until first results are to see and further decisions for modifications can be made.

12. Steps taken to overcome the barriers and arrive at an improved product

The start to overcome the barriers facing VISOLUX in adopting the ASIC technology was when we contacted the TTN and the feasibility study was figured out and documented in the form of the FUSE proposal for this AE.

Knowledge barriers:

The training in this pre phase by the TTN made it possible for the company to overcome some of the barriers especially the knowledge and psychological barriers.

Psychological barriers:

During the implementation of the AE, the company overcame the barrier, that the quality and reliability may not be as expected, by a certain training at the TTN.

Technology barriers:

The different technologies and their advantages or disadvantages due to the product to be improved became clear to decide, by connections to experts of the local university and the offers of different subcontractors.

A self learned experience was, when the company had to develop because of a customer require, a small optical sensor in discrete technology. A high failure rate existed in the production with the first samples because of requirement of using different PCB's which had to be connected together. The number of connection pads are very high and must be flexible and very small. This requirement was difficult to fulfil. So the only solution could be to use ASIC technology.

Another barrier was overcome during the AE when two disadvantages of the chosen CMOS-process have been compensated in changing the standard receiver circuit schematic.

Financial barriers:

This input and the steadily communication with the supporting TTN as well, as the preparing of the work plan and the economic point of view, made it possible to overcome also the technology and financial barriers.

13. Knowledge and experience acquired

The company has gained multiple knowledge and experience during this AE. The most significant points are as follows:

The project management including marketing analyses and requirements to the component (spec.'s).

How to find out the right technology, subcontractor and which tasks have to be taken to succeed (see work plan).

Experience with specifying and designing a full-custom ASIC with mixed analogue/digital functions.

Experience with S-C-Circuit Technology, which are normally realised in integrated amplifier, but not in discrete technology.

- Experience with Noise Suppression of S-C-Technology.
- Experience with Cross-Talk of S-C-Technology.
- Experience with EMC-Behaviour of S-C-Technology.

Experience with integration possibilities in integrated circuits and semiconductor physics.

Experience with chip-size requirements and costs of a known circuit, when the circuit should be integrated.

Experience which semiconductor-process will be the optimum for a certain circuitry to integrate.

Further experience with simulation tools and solutions for existing restrictions with simulation tools.

Test strategies and methods of qualifying the component (together with TTN & subcontractor).

Visolux had acquired a SPICE like circuit simulator which, for example, makes it possible to simulate the circuit before the design is realised in an ASIC.

All forecasted goals have been acquired. Visolux now is capable of planning and executing mixed signal projects.

14. Lessons learned

During this application experiment VISOLUX learned:

The feasibility study and the choosing of the subcontractor gives a lot of technology input, so that the lack of information can be overcome and the risk of an unknown technology as well.

It is very important to determine the persons and their certain competence in the project.

At the beginning of the AE and in the preparation phase of the project it was a very good decision to spread out all the information and teaching contents to all the electronic engineers in the company, with the result of higher acceptance. Then for the project three engineers were selected to do the main work.

The co-operation with an experienced subcontractor and a helpful TTN during the AE, opens synergy effects for all partners (advises for qualification of IC's and general problems in industrialisation and reliability). The numerous meetings had been very successful and instructive, so that the barriers perceived before the beginning were unfounded.

We learned where the limits are and the problem areas in integration of functions in relation to the chosen technology. This limits are:

Signal to noise relation of CMOS technology is significant worse than in bipolar technology.

Results of simulation tools should be evaluated carefully for their correctness.

At the end of this application experiment is to say, that we would like to have instructed more intensively the subcontractor to the key requirement of opto-electronic switches (e. g. ambient light suppression).

To overcome the different knowledge of the partners it is absolutely necessary, to have a very precise and complete specification of the wished function of the ASIC. This should include general requirements, which are for one partner normally self-evident.

15. Resulting product, its industrialisation and internal replication

Industrialisation:

The new component (ASIC) will be used in miniaturised light switches and light curtain applications. VISOLUX will remain after this AE in the same market sector of opto sensors.

The decision is already made to produce our ML4.1 family with the new ASIC and the presentation is made at the Hannover fair in this year.

That means to start with volume production with the same subcontractor of the ASIC in a SOIC 16 housing as soon as possible. At this time we are investigating the possibilities of fine pitch housings for even more miniaturising. The chances are very good because the chip size is small enough. The only difficulty is to find the right tool to encapsulate the existing fine pitch lead frames.

The encapsulating of the chip into a housing is the general necessity for:

1. Fully qualifying the component (ref. MTBF / reliability).
2. Easy assembling with SMD automates and reflow soldering in the production line.

Another aspect of this new ASIC is the possibility for a patent application (IPR) which is investigated at the time by our patent attorney and we are preparing an agreement between VISOLUX and the subcontractor.

Internal replication:

We are just starting a new ASIC project with a lot more features integrated, to complete our product variety.

Another ASIC project is at the push-start for a certain improved pre amplifier in bipolar technology. The circuit diagram of this IC will be complete developed at VISOLUX by the persons which took part at the AE. After this project the next step will be to layout the developed circuit with similar software tools which are trained during the AE.

Next ideas are going into the direction of chip on board (COB), flip chip or multi chip module (MCM) technology.

VISOLUX will inform the TTN about the progress of all the numerous activities mentioned above and likes to participate in further projects.

The prototype produced and demonstrated during the review is working, but does not comply with all the specifications. A redesign to fix these problems is started and the prototype should be completed in the first quarter of 1999. Visolux is working on a contract with FhG-IMS for production and qualification.

The special transparent package costs are 0.25 € in one possibility versus 0.60 € for the not-packaged ASIC.

The costs of industrialisation can be divided in three cost blocks:

1. Initial costs for the tested dies (same as projected 110 K€).
2. Housing costs (approx. -0.25 €/chip).
3. Qualification costs (approx. 5 ... 25 K€).

16. Economic impact and improvement in competitive position

The project will give VISOLUX the ability to compete successfully in the markets of very complex low cost light curtains and the smallest light beam switches where the profit margins are decreased annually for approx. 8 %.

VISOLUX will be able to evaluate fabrication processes, design tool systems, hardware simulators and test systems. We will be able with the help of the new designed chip to build a new generation of highly competitive light switches and light curtains.

The proposed optical sensor ASIC will replace the majority of conventional electronic components in the processing circuitry of a light-switch.

Only some EMC-protective components, filter capacitors, the transmitter diode incl. power stage, the LED, 5VDC-regulator and the electronic output will remain on the print board.

Because of this reduction of electronic parts a miniaturised family of sensors like the ML 4 series mentioned in the submission can be developed within only one housing. The number of print boards, mechanical parts, connecting cables decreases also and the assembling and checking processes will be simplified. So we are able to reduce the production costs per unit in the range of 50 %. The cost reduction will enable VISOLUX to strengthen its market position and open new markets. The ASIC allows to develop new products with specific requirements, e.g. for low-cost applications.

The technical improvements result in a significant quality improvement. Mean time between failure (MTBF) rises significantly. Small size and high reliability allows to mount the device to moving parts of machines and in places that may be hard to reach.

A further important and very competitive, price sensitive range of application of the ASIC are light curtains, where multiple light beams in a system are used. Therefore we have here a multiplication of the benefits.

Based on the total investment of 110 K€ and with the carefully estimated sales shown in the graph, the forecast for the payback period will be approx. 16 months.

The estimated ROI will be about 1700% for a 5-year period.

Development of company's market: The Sensor market Germany/Europe is expected to grow annually with 8 %. VISOLUX expects an increase of it's market share in the sector of industrial automation with the new ML4.1 family in the minimum of + 10%.

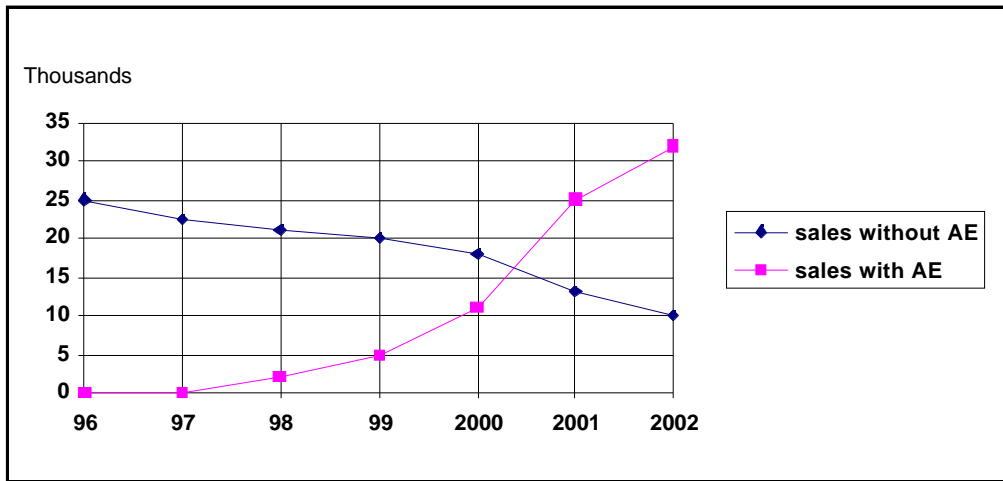


Figure 9 shows the economic trends of the product since 1996

The result of this AE is a full application specific integrated circuit with an on-chip-photo-detector, an ASIC to use for low cost light switches (see figure 10).

To have the ability to continue with the developing of more and different IC's .

To start with the continuous product innovation for the coming years.

To overcome the backlog in technology and price situation.



The cost of the existing product is 100 %. The cost of the SMD based product is 56 % of existing product price, while the ASIC based one is 31 % of existing product price. The manufacturing time can be reduced with about 50 %.

17. Target audience for dissemination

The application experiment may be of special interest to replicate for all companies which are assembling and developing discrete printed circuit boards, but are kept from using to ASIC technology due to the barriers, described in this document.

The advantages of using ASIC's instead of standard IC's are reduction of costs and improvement of quality. Products will be more competitive and will have a direct benefit because of a short time ROI. Even small companies shouldn't be afraid of going into the new technology. In Germany the market assessment indicates that only a few companies of the competitors currently use ASIC's in their products to meet customer requirements. For example the manufacturers of proximity switches working in the sector for non-contact sensor systems like energy sensors for water flushing in lavatories.

This AE provides an unique experience of special interest to such companies throughout Europe and will demonstrate how the assimilation of ASIC design capability can be undertaken with low risk and result in a significant commercial benefit to their businesses.

There are also many possibilities to use ASIC's in other industrial sectors and not only in opto-sensors. The whole range of sensor industry will be interested of the AE.

In general the results of this application experiment will be of interest to companies from the prodcom domain 33 (Precision Instruments) and especially 3320 (Instruments and Appliances for Measurement).