

# **FUSE Demonstrator Document**

## **Application Experiment Number 264**

### **Proposal to improve the parametric testing of Relays**

#### **Abstract.**

Applied Relay Testing Ltd is an SME, formed in 1992 in response to a small but significant niche market requirement for turn-key relay test equipment. Using our products, relay devices can be tested in both production and laboratory environments, with the benefit of standard test methods and well developed software facilities. The objective of the application experiment was to produce new test circuitry suitable for incorporation within a new parametric relay test system product, the RT290, enhancing technology in three general areas as follows:

- Replacement of mechanical relays by new-generation MOS devices.
- Upgrading existing 74-series logic circuitry to higher density programmable logic devices.
- Use of DSP techniques within the test system.

This new technology has allowed us to offer, at a given price, shorter test times, higher reliability, and the flexibility to adapt to individual customer's needs. This has increased the cost benefit of our product, making it more attractive for inclusion in highly automated systems. We are now actively planning new markets in Japan and the USA where a high-quality, high-specification product is expected to appeal greatly to prospective customers.

Following completion of the experiment, it was clear that the originally perceived risks of introducing the new technology were much greater than in reality. This was due to natural caution and 'fear of the unknown'. However, with good advice, guidance and the adoption of a planned approach to the project, these perceived risks were quickly replaced by expectations of success.

The costs of the experiment were 29KECU, and the project took 9 months. These costs will be recovered within 16 months and the Return on Investment during the life if the product is anticipated as being in excess of 200%.

#### **1. Company name and address.**

Applied Relay Testing Ltd,  
27 Cobham Road,  
Ferndown,  
Dorset BH21 7PE  
UK.

#### **2. Company Size.**

Number of employees is 3, and all are engaged on design and development. Prior to the Application Experiment their electronics expertise was limited to discrete analogue and digital components as well as simple PLDs. Company turnover is three hundred and fifty thousand ECU per annum.

#### **3. Company business description.**

Applied Relay Testing Ltd was formed in 1992 in response to a small but significant niche market need for turnkey relay test equipment. We now offer several relay test systems which combine high-speed and test integrity with software features which are the result of extensive development across a wide variety of relay applications. Using our equipment, relay devices can be tested in both production and laboratory environments with the benefit of standard test methods and well developed software facilities.

Most test systems have been supplied to manufacturers although some are supplied to test houses.

*Applied Relay Testing Ltd is registered in England No 2715226, VAT number 580161948*

These are pre-dominantly in Europe with a small amount of sales to Canada. With these satisfied customers, it is our intention to open a potentially large market for our equipment with Relay manufacturers in Japan and the USA and to develop new applications of our products to emerging relay technologies such as Photo-MOS.

The equipment is highly specialised and therefore has a limited market, annual sales volumes being typically of the order of ten units. All manufacture and test is carried out in-house

#### **4. Company markets and competitive position at the start of the AE.**

The company's markets are potentially world-wide, but until now most test systems have been supplied to users in Europe and Canada. Applied Relay Testing Ltd is one of only three known suppliers of relay test equipment. The other two are based in the USA and in Germany respectively. The USA company is our closest competitor technically and prior to the foundation of Applied Relay Testing in 1992 their products were purchased by several European relay manufacturers and users. The German company does not represent a significant competitive threat since their equipment is produced along with other non-relay equipment products. It is estimated that Applied Relay Testing Ltd had 30% market share, at the start of the experiment.

The majority of the customers are manufacturers of relays who require equipment that will either be used in the laboratory in order to verify new designs, or analyse production samples and devices returned by customers, or will be used in a production environment to carry out checks on the quality of the product being manufactured. The equipment must therefore be capable of supplying accurate, repeatable results as well as being simple to operate and robust enough to withstand operation on a production line.

Over the last five years, Applied Relay Testing has achieved acceptance of its products across Europe, in many cases as replacements for the products of the USA company, however our flagship RT90 relay parametric test system product is based on a technology which does not permit a great deal of the flexibility now being demanded by our customers, particularly where we wish to open up new markets based on high-automated production lines.

Following completion of the application experiment, our new product has now created significant interest in the USA and our expectation is that this will become the next strong market for us. Interest from the Far-East has been seen and we will be spending some time addressing this market during 1998.

#### **5. Product to be improved and its industrial sectors.**

The product sector is 'TA' - Technical Testing and Analysis.

At the start of the experiment the company's RT90 test product was selling well, but used a very conventional level of product technology involving analogue circuitry, mechanical configuration switching and 74-series 'glue' logic. It was clear that each of these areas would respond to a step-function technology increase with some important benefits.

Applied Relay Testing has successfully employed its FUSE experiment to obtain significant technology benefits in three main product areas:

- Replacement of mechanical relays by new-generation MOS devices.
- Upgrading existing 74-logic circuitry into programmable logic devices.
- Use of DSP software techniques.

It was decided to make the experiment a three part project which incorporated appropriate targets in each of these three topic areas with a final new parametric relay test system product design as the ultimate goal. With the experiment now complete, this product is complete, performs well and is attracting significant sales interest.

#### **6. Description of the product improvements.**

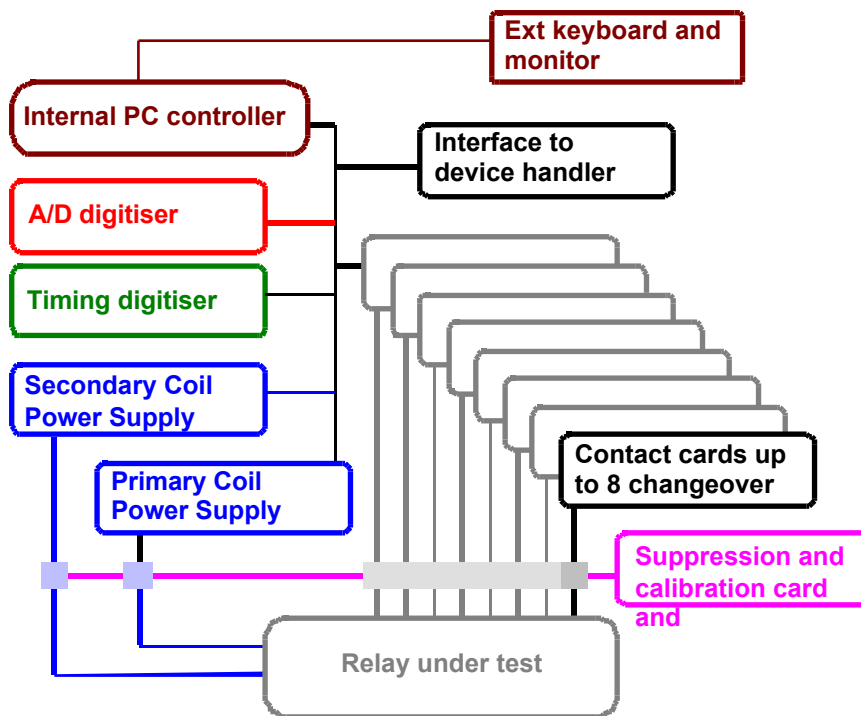
The experiment was designed to produce new test circuitry suitable for incorporation within a new parametric relay test system product, although the technologies transferred were intended to be also

suitable for use within other of the company's products as these become due for enhancement. The experiment resulted in a new parametric relay test system – the 'RT290' – shown in the following photograph:



The new system is, outwardly, very similar to the previous system (RT90), this was a deliberate choice in order to ensure that existing customers would not have to re-train their operators in order to be able to use the new system. Any changes therefore relate purely to the performance and functionality.

This new system (RT290) relies on the transferred technology to implement an architecture based on modules as shown in the following block diagram:



This block diagram is based heavily around the implementation of each of the three technology areas which have been enhanced. They are now described in more detail.

## **Replacement of mechanical relays by new-generation MOS devices.**

The FUSE experiment allowed the company to investigate the more recent MOS analogue signal switching devices. The company's products had all used small reed relay devices for setting up test configuration paths and it was clear that if it were possible to replace these with a solid-state equivalent there would be gains in system test throughput due to a reduction in measurement time, and significant increases in reliability due to the elimination of any mechanical movement while testing.

With the introduction of MOSFETs and devices such as the photo-MOS relay, a real alternative to the mechanical relay is emerging. In terms of switching speed, rigidity and bounce free silent operation a mechanical solution cannot compare. With careful circuit design the reliability of a solid state solution will outperform any mechanical part.

Our development program has shown that more care is required when designing the circuitry based around such a MOSFET solution, but as long as its limitations are understood it is not beyond the scope of any competent engineer to avoid the pitfalls. These pitfalls include temperature vs. on resistance and leakage characteristics, source-drain body diode conduction, latch-up, charge injection, capacitance (particularly between with large MOSFET devices), distortion, bandwidth etc.

Our product now uses all solid-state switching for its routine test tasks by employing a range of specially selected devices ranging from low-level CMOS multiplexer parts through to single and grouped power-MOS transistors.

## **Upgrading existing 74-logic circuitry using FPGA techniques.**

Prior to the experiment, the company's products used 74-series 'glue' logic which was inefficient for space, flexibility, cost and power. The objective was to replace such logic by a single more flexible, configurable logic device.

After sampling a range of parts and tools it was finally decided that the MACH family of CPLD devices from AMD offered a good compromise between cost, flexibility and programming and would provide an upgrade path to future more complex and dense FPGA parts if required.

During the subsequent evaluation program it was soon clear that circuit flexibility and small physical size were among the key attractions of a CPLD solution with additional benefits of reduced PCB tracking time, more flexible pin assignment and reduced programming time.

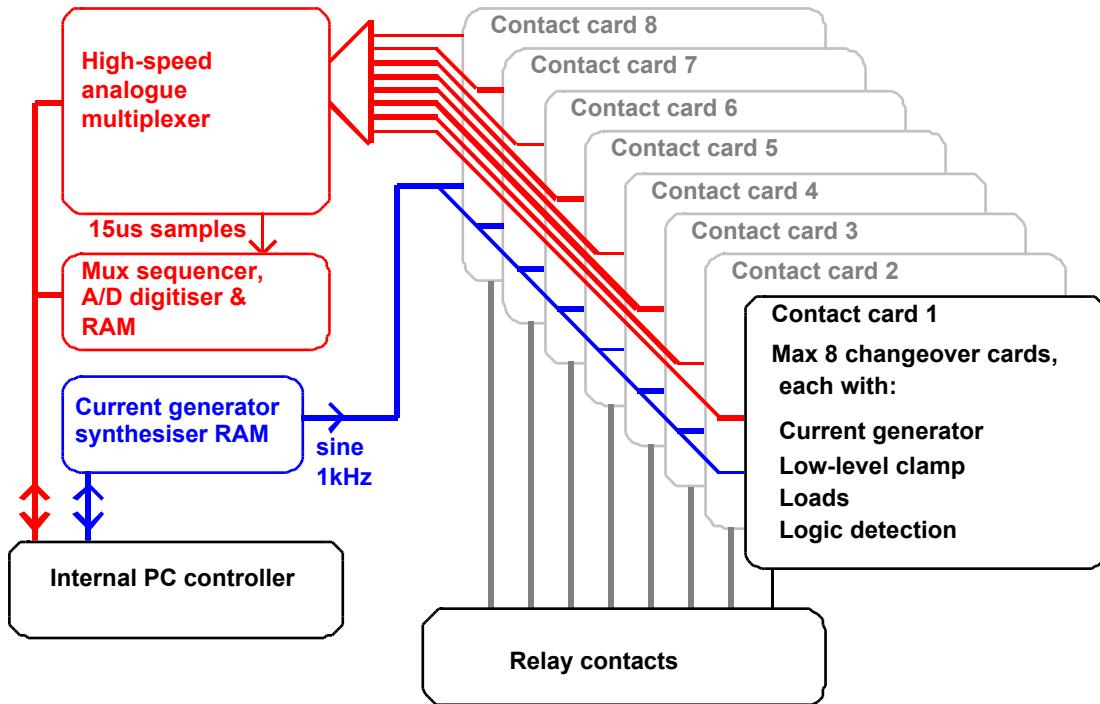
As with simple PLD devices, software tools are required in order to generate suitable JEDEC files for device fuse programming. Traditionally Boolean equations can be used for simple functions but they are complex and difficult to read when more complicated functions such as counters are to be implemented. Use of the schematic-to-JEDEC tool OrCAD SDT 386+ in conjunction with OrCAD PLD 386+ simplified the design process by using existing building block such as counters, comparators, shift registers etc. without any specific knowledge of the Boolean equivalent being known allowing direct creation of a functional logic block from a 74-series circuit diagram. Another benefit of this tool is that it offers vendor independence so that a design only need be linked to a specific part at the final fitting stage. Device fitter software tools are written by IC vendors specifically for their products in order to translate the universal PLA format file output to the JEDEC format required by the device programmer and cover all major devices.

The result of the evaluation has been that our new product created during the FUSE experiment is now fully based on a small number of CPLDs - typically one per circuit board. This has provided us with great flexibility and has already saved significantly on the cost of obtaining the repeat revisions of prototype PCB cards which would otherwise have been required when using the 74-series solution.

## **Use of DSP software techniques.**

As the third and final part of the FUSE experiment, the company was able to carry out a development and evaluation program to create a new product architecture which would replace existing analogue circuitry with a number of processor-based digital signal processing algorithms. Of the three parts of the experiment, this part has been the most interesting from an engineering viewpoint.

Digital signal processing techniques are becoming much more common in high-end measurement systems and the FUSE experiment has enabled the company to replace traditional analogue circuitry by using subsequent software processing, minimising drift and stray pick-up as well as centralising measurement resources.



As a result of this development the figure above shows the internal signal flow which is employed when measuring the contact resistance of a mechanical relay by our new parametric test system 'RT290'. Contact resistance must be measured 'in parallel' on all contacts together. The RT290 implements up to 8 'contact cards' each containing the necessary contact interface analogue circuitry and acting as a 'head unit' which connects using a 4-wire (Kelvin) connection directly to one changeover contact on the device-under-test. For low-level contact resistance measurement this circuitry translates a common test current sine waveform into a constant applied contact current of typically 10mA, limiting the maximum open-circuit voltage of this waveform to a programmed level (for example 20mV) and buffers the resulting contact voltage-drop.

In normal test systems, this voltage drop would be processed using additional analogue circuitry to rectify and filter it before presenting it for measurement by an analogue to digital converter. Instead, using the RT290's DSP approach, each contact card output feeds a high-speed CMOS analogue multiplexer which is automatically sequenced around all contact cards and allows the A/D digitiser to 'capture' a single pattern which contains information about the contact resistance of the entire device in one 'snapshot'. This digitised version of all observed contact voltage drops is complete by the end of the contact resistance measurement period and subsequent software processing extracts individual contact resistance results for each contact.

Correctly applied, this software processing achieves measured results which actually improve on stability over equivalent analogue techniques, and since the necessary algorithms do not need to run in 'real-time' we have easily implemented in a PASCAL language on our internal PC controller.

Another benefit of this DSP processing is that the quality of the measurement can be traded-off against measurement time by the User.

This part of the FUSE project was very beneficial and will lead to other technical spin-offs as well as significant cost savings .

## Summary Table

Existing Technology	New Technology	Benefits
Mechanical relays used for test configuration paths.	CMOS and MOS solid-state switching devices	Higher reliability; reduced measurement time; bounce free operation; silent operation
74-series logic / low-density PLDs.	CPLDs/FPGAs	Space saving - up to twenty 74-series devices in one CPLD; design flexibility via re-programming of devices.
Analogue circuitry.	PC-based Digital Signal Processing	Lower drift; lower stray pickup; design flexibility since analogue algorithms re-configurable by programming; higher throughput.

## 7. Choices and rationale for the selected technologies and methodologies.

### Replacement of mechanical relays by new-generation MOS devices.

Our existing older product included a number of mechanical relays which are a vital part of the testing process. We felt that we needed to re-design the test circuitry to accommodate the new generation of photo-MOS relay devices and to provide us with improved speed and reliability.

It is clear that the manufacturers of the newer generation of Photo-MOS 'solid-state relays' are pushing hard to gain acceptance of their product in place of traditional mechanical relays. The Photo-MOS product offers a number of apparent benefits such as increased reliability (no mechanical switching) clean switching (no bounces) and faster switch times, however these benefits are not without the significant disadvantages of a leakage current in the 'off' state, and an 'on' state resistance which can be several 10's of ohms.

Although the Photo-MOS disadvantages make them unsuitable as 'direct' replacements for mechanical devices, it appears to be possible to engineer the surrounding circuitry to 'work-around' these limitations, making the solid-state device an integral part of the circuitry instead of an isolated mechanical component.

We had already identified the existence of Photo-MOS parts with on-resistance's in the order of 10 ohms, and with off-state leakage's of around 1uA, and we were able to integrate these parts within an analogue measurement 'front-end' circuit designed to accept these limitations.

As a secondary task, suitable protection mechanisms for these solid-state devices were investigated.

During the investigation, we ruled out the use of other solid-state switching techniques such as thyristor, triac, bipolar transistors and IGFETs due to unacceptable voltage drop and / or leakage current limitations.

### Upgrading existing logic circuitry using FPGA techniques.

Our older product incorporated logic control circuitry which was based on a mixture of traditional '74'-series TTL devices and some low-density PLDs for combinatorial gate logic. To incorporate our additional requirements for a new product, we needed to further integrate this logic within higher density FPGAs. The use of microcontrollers or even DSP chips was ruled out due to the requirement for real-time capture speeds of 100ns per cycle. Only FPGAs are capable of operation at these speeds.

At first we intended to move to an FPGA device which was perceived to offer a wide range of logic capability and flexibility, but based on a short in-house investigation and discussions with our TTN, we identified the availability of the 'MACH' series of CPLDs from AMD. These

offered a good compromise between cost, density (from 1000 gates up to 4000 gates) and commercial availability. With these devices as our prime logic blocks we have been able to integrate some 5-20 existing 74-series devices into one new MACH device as well as gaining us flexibility in circuit changes. A full ASIC solution was ruled out due to our limited volume requirements.

### **Use of DSP techniques within the test system.**

Our existing relay device tests were made using dedicated analogue signal-conditioning circuitry which performed well but has limited flexibility. We proposed to adopt newer 'DSP' techniques which would integrate a significant proportion of the analogue circuitry within DSP algorithms, greatly enhancing test flexibility and speed, whilst simplifying the circuitry.

Our older product measurement circuitry is based on an AC voltage-drop measurement technique using a phase-sensitive pre-amplifier and integrator assembly. Both the amplifier and integrator are implemented using op-amp techniques. Our device test method requires a parallel architecture which provides one measure circuit per device contact, resulting in the use of significant space and power by these circuit blocks. In addition, the analogue nature of the integrator leads to a slower measurement and some thermal drift during testing, causing a problem if the test system cannot be re-calibrated for some time.

Using DSP techniques in the new products, we were able to replace the integrator section of the architecture with a high-speed multiplexer which scans all measurement channels at a high rate, placing the digitised results into a local memory. Choice of suitable DSP algorithms allowed us to implement two important features currently achieved with analogue circuitry:

- Existing channel duplication of the analogue solution was eliminated by storing all channel data in the memory and 'unpacking' this data into the relevant channel results.
- The digitised data is now an AC test waveform to which is applied a phase-sensitive rectification algorithm returning it to a meaningful value and removing unwanted line noise.

During the investigation we were able to rule out the need to use a discrete DSP processor due to our limited bandwidth requirement, and this has resulted in a more cost-effective solution.

The use of a microcontroller or microprocessor solution was also ruled out because of the need to carry out a series of multiply and accumulate instructions in a relatively short period of time.

For best cost / performance trade-off, these DSP algorithms execute on the internal PC-compatible controller which forms a part of our new product. This gave the benefits of using a DSP approach, without incurring the costs of additional devices.

## **8. Expertise and experience of the company.**

The Company has a staff of 3 employees and each concentrates on a specific area of expertise. These are

- Hardware and circuit board design. This was limited to discrete analogue and digital components, and simple PLDs
- Software design
- Mechanical design and production

Our system circuit design and procurement is all in-house. Circuit-board production and assembly is all contracted out, but module and system test and commission is retained in-house.

## **9. Workplan.**

The use of subcontractors was restricted to the provision of the DSP training described in the

section in Training , and represented a small percentage of the budget.

The Workplan laid out the tasks required to get us from our existing level of technology to a new product design which encompassed the new technology points. We tackled these tasks under the following broad areas:

### **Specification.**

During this initial phase of the Workplan we drew up lists of MOS and Photo-MOS switch parts potentially suitable for our solid-state switching application, a new circuit architecture to accommodate the effects of finite MOS and Photo-MOS device parameters, and a list of suitable complex FPGA and CPLD logic parts to incorporate our existing '74-series' logic. In addition we created some simple DSP algorithms using simulated data to use in initial comparison of results against equivalent analogue circuitry such that we could evaluate projected test performance and define our exact training requirements. A total of 21 days of engineering design work was required to complete this phase.

### **Training and preliminary engineering investigations.**

During this part of the Workplan various training components were provided to obtain the necessary experience to fulfil the experiment. These components included –

- A short training course on Digital Signal Processing techniques provided by our subcontractor and involving both our software and hardware engineering staff.
- In-house training on solid-state switching by making actual measurements on MOS and Photo-MOS sample switch parts.
- Training on FPGA and CPLD programming using the ORCAD design tools provided by A.R.S Microsystems as part of our purchase of their software package, enabling us to use high-level programming of these parts using schematic entry.

A total of 24 days of hardware and software engineering effort was required for these components.

### **Design work.**

The design phase set out to create various hardware and software components ready for integration within our final system. The solid-state switching technology was implemented by creating an assembled prototype Photo-MOS switching card, an assembled prototype logic card was created based on our chosen CPLD device and the digitiser card was created ready for implementing our chosen DSP algorithms. A total of 45 days of engineering effort was required for this phase.

### **Evaluation.**

With the components created during the design phase, we were able to move on to their individual evaluation and then to their performance as part of the complete measurement system. This work produced a report on the measured performance of the prototype Photo-MOS switching cards, an operational logic card based our CPLD device and a report on the measured performance of the completed digitiser circuitry. It was at this stage that we first experienced the benefit of the new DSP algorithms. Some 27 days of engineering effort were required during this phase.

In addition to the engineering phases above, the company's manager dedicated a total of 15 days of effort to the tasks involved in planning, implementing monitoring and reporting on all phases of the experiment.

The following diagram is a Project Plan which shows both the actual and planned timing for the principle tasks.

The following key explains the symbols used on the chart

Symbol	Meaning
g	Planned task that occurred
r	Planned task moved or cancelled
a	Actual task – moved from planned

	Jun-96	Jul-96	Aug-96	Sep-96	Oct-96	Nov-96	Dec-96	Jan-97	Feb-97	Mar-97	Apr-97
<b>Management</b>											
Project Management	gggg	gggg	gggg	gggg	gggg	gggg	gggg	gggg	gggg	rrrr	rrrr
Dissemination									a	a	r
Reporting	g	g	g	g	g	g	g	g	a	a	r
<b>Specification</b>											
Photo MOS Devices	g	g	g								
FPGAs	g	g									
DSP Algorithms	g	g	g	g	g						
<b>Training</b>											
Photo MOS Devices			a	r							
FPGAs			g								
DSP Algorithms				a	r			a			
<b>Design</b>											
Photo MOS Devices		g	g	g	g	g					
FPGAs		g	g	g	g						
DSP Algorithms			g	g	g	g	g	a			
<b>Evaluation</b>											
Photo MOS Devices							g	g	r		
FPGAs						g	g	g			
DSP Algorithms								g	g		

The planned and actual effort and costs are shown in the following table. It should be noted that, although the experiment was finished ahead of schedule, more effort had been spent on the project than had been planned. The results of the experiment, in terms of the project planning, will be utilised in future projects as Applied Relay Testing has improved knowledge as to the anticipated task durations for such a project. The results also show that projects can be completed ahead of time if additional effort is applied to them.

	Planned		Actual	
	Effort (person days)	Cost (kECU)	Effort (person days)	Cost (kECU)
<b>Management</b>				
Project Management	3	0.43	8	1.22
Dissemination	6	0.86	6	0.92
Reporting	6	0.86	8	1.22
<b>Specification</b>				
Photo MOS Devices	12	1.72	15	2.29
FPGAs	3	0.43	8	1.22
DSP Algorithms	6	0.86	12	1.83
<b>Training</b>				
Photo MOS Devices	10	1.43	10	1.53
FPGAs	4	0.57	4	0.61
DSP Algorithms	5	0.72	5	0.76
<b>Design</b>				
Photo MOS Devices	18	2.57	28	4.28
FPGAs	15	2.15	22	3.36
DSP Algorithms	12	1.72	22	3.36
<b>Evaluation</b>				
Photo MOS Devices	8	1.14	12	1.83
FPGAs	2	0.29	7	1.07
DSP Algorithms	17	2.43	26	3.97
<b>Totals</b>	127	18.16	193	29.51

## 10. Subcontractor Information

Applied Relay Testing appointed Bournemouth University as a subcontractor to provide the required training and consultancy in Digital Signal Processing techniques and FPGA design. The reasons for this were :

- Applied Relay Testing already had knowledge of the Universities capability and commitment to training.
- The University offered a cost-effective solution.
- Close physical proximity enabled informal short-notice contact to be maintained.
- The University's experience of handling the formal training of its other industrial contacts made it possible for Applied Relay Testing to receive broader-based guidance than would be possible with a smaller sub-contractor.

The Department of Electronics at Bournemouth University has been involved in teaching, research and consultancy in microelectronics for over 10 years. During this time, the Department has worked closely with companies in the South-West region of England, in the industrial applications of microelectronics. In the specific areas addressed by this experiment, expertise exists in the fields of Digital Signal Processing, FPGA design and the application of these technologies to industrial situations.

The sub-contractor provided training and design support on DSP, the design support being provided in the form of a review of the algorithms used to perform the required functions. This proved a very useful means of verifying the effectiveness of the Technology Transfer activity, as it confirmed that staff at the company had acquired the necessary knowledge. The sub-contractor was also able to provide useful input with regard to the choice of Programmable Logic.

Some training was also received as part of the purchase of the software tools used for the FPGA/CPLD design.

All other aspects of the project were carried out by Applied Relay Testing personnel, and therefore the full IPR associated with the product rests with Applied Relay Testing. This was especially important to Applied Relay Testing because, as a very small company they are vulnerable to loss of market share if the details of their technological advances are not retained solely within the company.

## **11. Barriers perceived by the company in the first use of the AE technology.**

The barriers perceived by Applied Relay Testing Ltd preventing the adoption of new technologies are as follows:

### **1. Knowledge barriers.**

Applied Relay Testing Ltd needed to re-design its existing RT90 parametric test system to remain competitive, yet the extent of the changes required knowledge of the benefits and limitations of FPGAs, digital signal processing algorithms and new-generation solid-state switching devices which was not available to us before the project.

### **2. Psychological barriers.**

As with many companies, strong arguments against adopting new technologies were to simply lower the selling price to compensate for inadequacies and not to re-design, and there was a management feeling that it was better to stick with small changes to the existing product rather than to start with a totally new concept.

### **3. Technology barriers.**

The company had been using its existing technology solutions for some years and had grown very comfortable with these tried and tested solutions, making it an even harder task to break out of these traditional design solutions.

### **4. Financial barriers.**

As a small company with only three employees, Applied Relay Testing must concentrate on the demands of day-to-day production, leaving little time for the longer-term investment in developing new technologies. Undertaking any new development incurs risk and this creates a barrier by making it unacceptable to allocate disproportionate funds against a possible negative outcome. Such financial barriers only serve to reinforce the knowledge and technology barriers further.

## **12. Steps taken to overcome barriers and arrive at an improved product.**

After acceptance of the proposal, Applied Relay Testing allocated the time of 3 engineering staff toward various tasks in the experiment Workplan, enabling them to experience individually and at first hand the positive effects of the training and technology as compared with the techniques which they were currently using. The DSP and logic programming training were particularly useful in transferring-in experience from our sub-contractors into our company. Towards the latter stages of the experiment, these benefits were strengthened further by a team feedback as the new product came together and each member of staff could see additional benefits which were also accruing outside of their own specific field of expertise.

Specifically the barriers were overcome as follows:-

### **1. Knowledge barriers.**

The initial consultations with the TTN enabled Applied Relay Testing to become aware of the possibilities that the various available technologies, and how these could be applied to their own unique range of products.

### **2. Psychological barriers.**

Staff from the company attended an awareness seminar organised under the DTI's Microelectronics in Business programme, and the case studies presented there, coupled with others that the TTN made available demonstrated the real benefits that could be achieved. Although the company could now see the benefits of performing an intensive re-design of its products, the financial barrier detailed above still made the allocation of staff to the tasks extremely difficult.

### **3. Technology barriers.**

This barrier could only be overcome by the training, both external and internal that was carried out prior to and during the actual experiment.

### **4. Financial barriers.**

This final barrier was overcome as a result of the company's successful application for a FUSE Application Experiment. It is difficult to see how, without some outside source of finance, that a company such as Applied Relay Testing could have been able to allocate the necessary resource to carry out what were in fact essential product innovations.

## **13. Knowledge and experience acquired.**

Prior to the experiment, the company's approach to the design and manufacture of its products relied on traditional techniques which had been used by its staff for a number of years.

From the construction of the original Workplan and as the experiment progressed, the liaison with our TTN and subcontractor began to change the way in which we viewed our existing solutions as our realisation increased of the benefits of these new techniques. By the end of the experiment our experience had increased significantly in the following main areas:

- Project planning for development.
- Management of a project to meet planned objectives.
- Predicting the long-term sales implications consequent upon engineering issues.
- The application and trade-offs of solid-state versus mechanical signal switching.
- The benefits of digital signal processing techniques for handling analogue measurements.
- The ability to utilise DSP techniques to improve the performance of its products
- Improved manufacturing and stocking methods possible by the use of CPLDs.
- Utilising FPGA/CPLD technology to reduce component count, improve manufacturability, and reduce the cost of its products

## **14. Lessons learned.**

The experiment has been a valuable tool in acquiring a wide range of experience which covers all areas of engineering. We feel that these lessons for us fall broadly into the following groups:

## **1. Perception of risk.**

Following completion of the experiment it was clear that the originally perceived risks of introducing the new technology were much greater than in reality. This was due to natural caution and 'fear of the unknown', however with good advice, guidance and the adoption of a planned approach to the project, these perceived risks were quickly replaced by expectations that enough success would be achieved to justify the experiment. Applied Relay Testing will in future make a more systematic approach to its product development, and would advise any other company to do the same. Such an approach will involve a thorough initial investigation into any new technologies to ensure that a balance decision is taken as to their applicability.

## **2. New engineering solutions.**

The technology solutions derived during the experiment have provided Applied Relay Testing with a first-class set of knowledge tools which will allow all future products to directly benefit from their application. In particular the digital signal processing techniques will allow faster time-to-market for future products as well as providing high levels of flexibility now being demanded by customers. The physical solutions of solid-state switching and the integration of 'glue' logic into CPLDs will also provide the company with increased reliability and lower manufacturing costs, all contributing to better profitability. With these technology solutions the company has learned that even differing products can be made to more closely share solutions with resulting lowering of costs and development risk.

## **3. Design for EMC.**

Since the solutions had such a radical impact on the architecture and implementation of our relay test system, the company used the Workplan to implement a parallel 'design for EMC' internal program. Several years ago, Applied Relay Testing foresaw the costs and delays which might result from the need to meet the forthcoming European EMC Directive, and invested in a small in-house EMC test facility. This ensures that the full impact of new technology can be assessed at the design stage, instead of delaying this, and therefore possibly incurring re-design work. Although this EMC work was not part of the experiment, the discipline of the experiment Workplan and its phased approach made it possible to integrate the EMC testing and to ensure compliance with the relevant EC directives without incurring time penalties.

## **4. Project Management.**

With the benefit of hindsight, the task of producing a suitable Workplan with the required milestones and deliverables was a formidable one. Applied Relay Testing was one of the first applicants to be approved for a FUSE experiment and this resulted in a high level of forward planning having to be applied at an early stage. The extent of this forward planning is unusual for a small company and the amount of work involved was unexpected, however due to the support and encouragement of our TTN (Bournemouth University) the Workplan was adjusted to include realistic and manageable deliverables. The benefit of this early work was that during the implementation of the Workplan, the attention to detail and accuracy resulted in a very controlled and measurable project which was easy to monitor and report. Due to the amount of early planning and thought which went in to the Workplan, where small changes had to be subsequently made to time-scales, these were then easily accommodated by simple discussion with our TTN and the relevant adjustment to the plan without actually changing the nature of the deliverables.

## **5. Customer reaction.**

Since the launch of our new RT290 parametric test system which includes all

solutions derived during the experiment, the company has received very positive reaction from customers. There have already been upgrades of existing older equipment by the new system to allow customer to take advantage of the new facilities offered, and Applied Relay Testing has already begun opening up new markets in the USA where demanding customers expect these new solutions to be in place. The indications are clear that without adopting these new techniques, it would have been much more difficult to penetrate these new markets and to obtain repeat sales.

## **15. The Future: Industrialisation and internal replication.**

By adopting a 'Right First Time' approach, including making use of the in-house EMC test facility, described in the Workplan section, Applied Relay Testing was able to put the new RT290 product parametric test system which includes all solutions derived during the experiment, straight into production. AS already mentioned, the total cost of the product update was 50 kECU, but the benefits of this investment have already been experienced. Since the product launch, the company has received very positive reaction from customers. To date, it is estimated that three of our sales are due to the technical improvements. There have also been upgrades of existing older equipment to allow customers to take advantage of the new facilities offered. A budget 'entry-level' product version is planned, which will address some sales opportunities known to be price-sensitive.

Our new product has created significant interest in the USA and the Far East, and our expectation is that these will become strong markets for us, particularly for a high-quality, high-specification product.

All three engineering staff have been trained in the new technologies, and further designs are being considered. The software CAD tools were more than adequate for the current designs, and can provide an future path to more complex and dense FPGA parts as necessary. Despite the expected increase in activity, it is envisaged that the manufacturing and testing will still be carried out by the existing staff and that the marketing strategy will remain unchanged. These policies will, of course, be regularly reviewed in order to ensure that the best use is made of all available resources.

## **16. Improvement in competitive position.**

It is expected that these new technologies will result in an improvement to our competitive position by the following increments:

### **1. Higher sales volume of the product.**

The transferred technologies will allow us to offer additional capability and reliability at a given price, increasing the cost benefit of our product and making it more attractive for inclusion in highly automated systems. We have a plan to open new markets in Japan and USA where a high-quality, high-specification product is expected to appeal greatly to prospective customers. In fact since the launch of the new product, we have sold four systems to customers in the USA and these are the first sales into that, potentially, large market.

To date, it is estimated that at least seven of our sales have been made as a result of the technical improvements.

Expected gain 1997 - 2001 inc., ECU 350,000

### **2. Upgrade Sales to existing customers.**

In Europe, we have already made several years of sales of our existing product which has been well received. With an updated version of the product incorporating the planned technology improvements, we expect to be able to encourage existing customers to upgrade to the new product. Interest has already been expressed in this.

Expected gain 1997 - 2001 inc., ECU 110,000

### **3. Sales of lower-cost products to new customers.**

The increased digital integration and DSP algorithms will allow us for the first time to offer the new product at a range of end-user capability. A budget 'entry-level' product version will address some sales opportunities known to be price-sensitive.

Expected gain 1997 - 2001 inc., ECU 60,000

### **4. Lowering of product manufacturing and warranty costs.**

Each of the improved technologies will lead directly to cost savings, resulting in a reduction in product cost of approximately 30%. The end user cost however will not change appreciably because of the additional functionality and improved performance that the new unit gives to the end user.

Use of CPLD logic devices will provide the benefits of faster product assembly and programming as well as easier field changes, with the reduction in chip count resulting in a higher reliability with the customer. It is highly likely that this approach will also result in less development risk of circuit cards based on these devices, since changes will often be possible at the cell level instead of circuit card modifications.

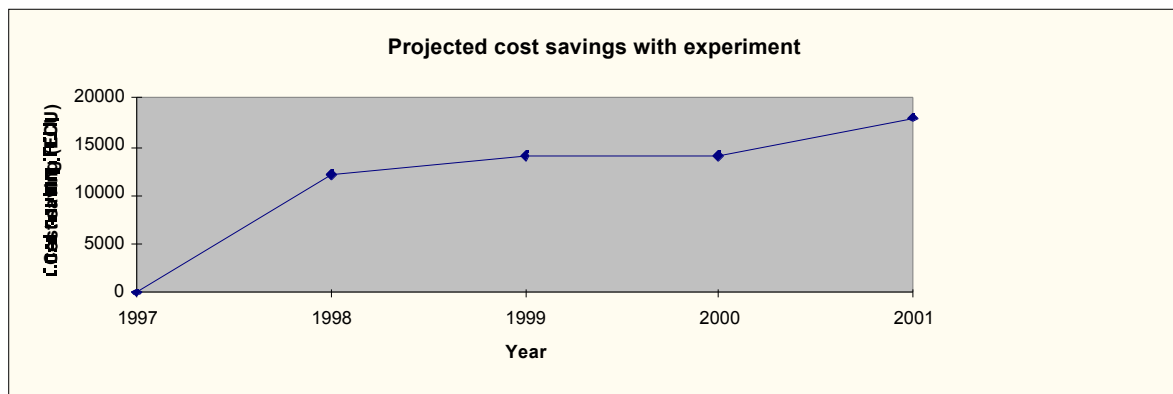
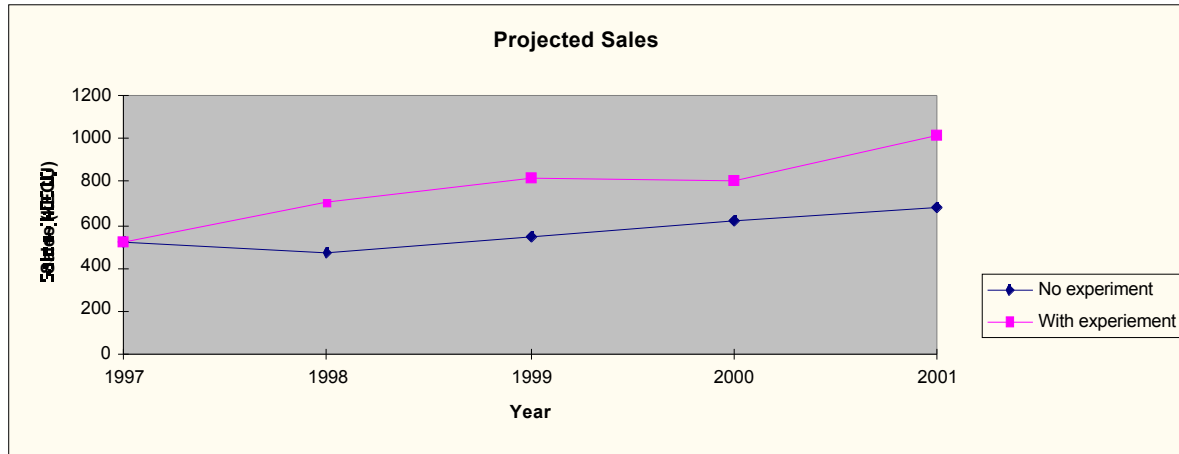
The DSP algorithms will eliminate a number of analogue components resulting again in lower manufacturing costs, a more electrically stable test system throughout life and increased flexibility.

The MOS replacements for mechanical relay switching will lead to some small increases in build costs, but will reduce expensive warranty repairs.

Total expected cost savings 1996 - 2001 inc., ECU 40,000

## 5. Summary of benefits.

These figures are also shown graphically by year in the following two graphs.



The sales figures to date amount to 6 units in the first year (1997/8) of sales of the new product, and 10 units on the second year (1998/9). It is anticipated that this will level off with sales of 10 units in each of the two subsequent years, after which it will be necessary for ART to have developed a new model in order to maintain market position.

Return on investment - the cost of the experiment plus the additional costs of putting the improved product into production were approximately 50,000ECU. It is expected that the profit on the increased sales, and the cost savings described above will allow recovery of the investment within 16 months. It is also anticipated that the overall Return on Investment as a percentage of the investment will be 200%.

## 17. Target audience for dissemination.

Applied Relay Testing manufactures equipment with internal features common to equipment produced by many other small companies who work in the test equipment field. We expect that the success of this experiment can be directly ported to such other equipment and is expected to be of great interest to test equipment designers in the TA sector motivating them to move to more reliable and flexible solutions than traditional analogue techniques.

Moreover the use of DSP techniques should be of interest to any company that is currently performing some form of analogue signal conditioning, sine the appropriate use of such technology can bring enormous benefits in terms of flexibility and predictability. Similarly the use of FPGA/CPLD technology to reduce component count and increase product flexibility will be of interest to any company that currently utilises discrete logic to perform a “glue logic” function.

This will include companies in the following industry sectors, and with the following Prodcom Codes :-

<b>Industry Sector</b>	<b>Prodcom Code</b>
Communication Equipment	321
Sound and Image	323
Medical Instruments	331
Instruments for Measurement	332
Industrial Process Control	333
Electrical	31
Musical Instruments	363

In addition to this more general dissemination, Applied Relay Testing has already seen local interest in the result of the experiment from other small companies with whom we have informal technical relationships.