An Enhanced Data Acquisition System

FPGA Leads To Cost And Space Reductions

Prosig Ltd.

TTN: University of Glamorgan Commercial Services (UGCS) Ltd
AE Abstract

Prosig Ltd is a small, rapidly growing company that designs, manufactures and markets high quality data acquisition and data processing systems for harsh environments such as those experienced in the automotive, power generation and fatigue testing industries. These field data acquisition and analysis applications include vehicle development and refinement in the automotive industry, and condition monitoring with emphasis on vibration in power generation industry. The company employs 45 staff, and in 1998 the company achieved sales of 3.3 M Euro. 30% of the company’s sales are achieved from the Protor data acquisition system.

The company’s Protor data acquisition and data processing system utilises discrete digital and programmable logic device (PLD) technology to implement the Plant Monitoring Module (PMM) which is central to the functionality of the system. The generation of speed monitoring and clock generation functions using this technology limits the equipment’s performance in terms of its range and resolution. The increasing data acquisition rates required as the speed of many of the plant items now being monitored is increasing made it essential that the PMM capabilities are upgraded.

The market for vibration condition monitoring is also cost sensitive, particularly in the UK. Any reduction in hardware costs provides commercial advantage. The objective of the application experiment was therefore to introduce cost savings by the rationalisation of the system architecture and reduced component costs based upon the use of a flexible FPGA technology, and to improve the systems performance.

The FPGA device enabled the following functional improvements to be made:

i) Replace the speed sensing and clock generation circuit with one that has sufficient bandwidth to cope with current and future demands for monitoring of plant with higher shaft frequencies.

ii) Replace clock circuits based on a combination of discrete components and small scale programmable logic devices with a single in-circuit programmable device implemented on a PC/104 compatible PC interface card.

iii) Rationalisation of the main PROTOR hardware component through the use of proprietary hardware made possible by the availability of a standard PC card with the required clock logic.

The rationalisation of this key component of the PROTOR system provides not only extended operating parameters but have significant impact on the manufacturing and maintenance cost of the system. The increased product sales will result in a return on investment (ROI) of the prototype development costs of 27 KECU over the product life of 5 years of 500%. The payback period for the investment costs in developing the prototype system is 13 months.

The duration of the application experiment was 9 months.

The application experiment will develop a sustained company capability in FPGA design, which will enable the development of other improved products, using this technology.
AE Signature and Keywords

AE Signature
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Keywords:
Timing synchronisation
Clock generation
Data Acquisition
Processor Interface
FPGA
1. Company name and address

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2. Company size

Prosig is privately owned and has its headquarters in purpose-built premises in Fareham, England. The company also has a sales offices in Dover, New Jersey and Detroit, Michigan. A total of 45 staff are employed in these offices. Prosig also owns the Lysses House Conference Centre, which is run as a quality hotel (AA 3 Star). It employs another 15 staff. The company had a turnover of 3.3 M EURO in 1998.

3. Company business description

Prosig Limited designs, manufactures and markets high quality data acquisition and data processing systems for field data acquisition and analysis applications in the automobile and power generation industries.

From its inception, Prosig has supplied complete turnkey hardware and software solutions, initially using third party hardware and Prosig software. Some 10 years ago Prosig began to design and manufacture its own data acquisition and signal conditioning hardware. This has continued to the point where we are able to provide advanced cost-effective solutions to a whole range of acquisition requirements.

The current staff of forty five consist principally of software and hardware engineers, with a small administrative support group. Part of the team include software support and hardware maintenance staff. A number of technical agents are in place to provide support internationally.

Prosig produce systems to ISO 9000 standards, and are approved suppliers to several large companies including Westinghouse (USA), CIS-Amriien (France) and Nuclear Electric (UK).

**Industry sector**: Instruments for Monitoring and Checking (Prodcom Code 3320)
4. **Company markets and competitive position at the start of the AE**

Prosig Ltd is a small, rapidly growing company specialising in the design, manufacture and marketing of high performance data acquisition and data processing systems. Prosig’s principal customers are from the following sectors

- Automotive
- Aerospace
- Power generation
- Vehicle manufacture & test
- Defence & Military

Most of the company turnover comes from direct sales although some sales are now through distributors for low cost software products. Prosig have supplied and installed systems in Germany, France, United States, Canada, Portugal, Korea, Austria, Argentina, Sweden, Chile, Italy, Australia, Taiwan, India and China in addition to those in the UK.

Prosig specialises in the supply of data acquisition systems for high quality data gathering in difficult environmental conditions, such as those experienced in car crash monitoring, car noise and vibration testing, and nuclear power generation. These products are generally high value systems that can either be used as a standalone equipment for monitoring single systems or as a distributed system capable of monitoring several plant items, for example in large multi-power plant installations.

System costs can range from 20 K Euro to over 130 K Euro (including operating software) depending on the configuration of the system required.

Sales of the company’s existing data acquisition system, the Protor, are strong in the UK and the company has an estimated 30% of the target market share. In addition there is a large potential for systems in both the US and Europe for systems to monitor major plant systems, such as power generation plant equipment. The company has recently installed systems in both the US, China and Australia.

Prosig compete with a number of European and United States companies in the supply of monitoring systems for plant in the power generation marketplace. In the USA there is a strong existing USA based manufacturer, Bentley Nevada. The European market is more diverse. In both of these areas technological performance and price competitiveness is essential. Our principal competitors are shown in Table 1 below with the geographical market.
Company | Geographical Market
--- | ---
ABB | Scandinavia
B&K | Europe
Bentley Nevada | USA & Europe
Beran | UK
Westinghouse | USA

Table 1: Principal Competitors for Industrial Monitoring Equipment

The price / performance ratio of the Protor system provides a distinct competitive advantage in this market. However purchasing decisions are often dominated by cost. This is particularly true in the UK, our main market. Also when penetrating new markets the cost advantage to the customer has to be greater to gain market share against established competition.

Prosig consider the Protor system to represent the market performance leader. However, there are clear signs that competitors are beginning to reduce this technical advantage. The company’s sales growth for the data acquisition and processing systems have shown a 10% annual increase over the last 3 years.

![Protor Sales Revenue (relative to 1996)](chart)

Chart 1: Sales Trend for Existing Systems

The demand for more sophisticated monitoring systems, such as PROTOR, is expected to grow as concerns over energy efficiency and environmental issues grow. There are also a larger number of smaller power stations in the US that will require this equipment. For the rest of the world the adoption of plant monitoring systems, as opposed to just measuring overall vibration levels, offers another emerging market.

This growing market represents a major opportunity for high performance data acquisition and data processing systems such as the Protor. However, this potential market is very price
sensitive. In addition, this sales growth for the system will also be restricted by the ability to
deal with auxiliary plant and smaller power plants that have higher shaft speeds and hence
data acquisition rates than is possible with the existing system.

The economic rationale for the application experiment is to improve the company’s data
acquisition equipment’s performance in terms of acquisition rates and to reduce the cost of
manufacture and cost of maintenance of this system. An enhanced system with increased
flexibility and lower production costs will allow Prosig to improve its competitiveness in the
UK market and provide increase margin required supporting further sales in export markets.

5. Product to be improved

The product to be improved is a multi-purpose, high performance data acquisition system
designed for vehicle crash testing, vehicle engine and noise level monitoring, and vibration
analysis in large plant applications. The company’s PROTOR system (previously based on
the P4400, now obsolete) is a complete solution for such applications as the vibration
monitoring of rotating machines.

The complete system design is configured so as to enable the equipment sub-modules to
provide individual multi-channel acquisition and processing system linked to one or more
powerful central database processors in an open structure network. The system also
provides facilities for comprehensive alarm checking, mimics, trends, vector plots, Fast
Fourier Transforms and other processing of real time and historic data.

The Remote Monitoring and Data Acquisition System (RMDAS) is central to the Protor
system’s data capture capability. Each unit is a self-contained system that includes signal
conditioning, data capture and first stage processing hardware. Each unit is either connected
directly to a host using a high-speed serial link or several units are connected to a central
Host system that acts as the central database via an Ethernet link.

The existing RMDAS unit contains:

- A Remote System Control Module (RSCM) which is connected to the network and
  acts as a subsystem controller.
- A Plant Monitoring Module (PMM). One PMM module is required for each equipment,
  for example a plant item, to be analysed.
- A number of data acquisition modules. These Signal Measurement Modules (SMM) are
  controlled by the PMM. The number of channels being monitored for each plant dictates
  the number of SMM’s.
This system architecture is illustrated in Figure 1.

The Remote System Control Module (RSCM) is based on a proprietary single board computer. Whilst its primary function is to connect the subsystem to the network, the RSCM must also provide additional functionality to overcome the shortcomings of the original Plant Monitoring Module design.

The Plant Monitoring Module is the target for the design improvement. This unit is a custom designed data capture controller that incorporates the processing algorithms that make decisions about when to capture data. The PMM processing also includes data reduction and formatting of data packets for transmission to the host through the RSCM. The functional block diagram of the PMM unit is illustrated in Figure 2.
The functions performed by the PMM include:

- The generation of a sampling clock synchronised to the ‘tacho’ synchronisation input. This input is used where data analysis must be related to external events. For example, in machinery applications the physical systems to be monitored (vibration or noise) are often related to the shaft speed. Speed tracking and the generation of multiple, synchronous, equiangular spaced sampling pulses are therefore required.
- The generation of a wide range of clock frequencies related to the synchronised signal so as to provide for alternative measurement resolutions to meet the needs of particular applications.
- Clock generation in non-synchronised sampling applications.
- General purpose inputs and outputs (I/O) that are used to set alarms and monitor external events, such as equipment states.

The PMM is configured by parameters downloaded by the processor.

The current PMM utilises two AMD 9513, 5 channel 16-bit counters, a programmable logic device (PLD) and a dedicated processor to implement the functions required in the PMM.

The AMD 9513 device is a sophisticated counter device that has several facilities crucial to the implementation of the speed sensing and clock generation circuit. These include:

a) Continuous operation with count saved and flag set on each leading or trailing edge of the gate input. Connecting the gate input to the tacho signal provides a means of stabilising the count on each tacho edge while continuing to measure the next period. The flag output can be used to generate an interrupt on the control processor. Two counters must be used to achieve the current resolution as the counters are only 16 bits wide and the measured speed range is from less than 10 RPM to 3000 RPM at a resolution of approaching 1 RPM.

b) Precise Clock generation triggered on an external event and a duration of exactly N ticks. This is required to perform the clock generation so that a clock pulse stream is generated synchronised to the tacho pulse and lasts for exactly N pulse which relates to a number of complete cycles of the shaft at the predicted rate.

c) Selection of wide range of clock frequencies to provide the resolution required.

d) Support for other clock generation modes: Trigger – non-Triggered.

e) Support for software parameter control.

The 9513 is the only clock chip that we have found that provides these facilities. However, to meet the performance requirements it is necessary to include a dedicated processor in the
design. The processing algorithm requires that the processor to measure speed, decide to capture and set-up capture within 20 ms.

There were several reasons for improving the market competitiveness of the system. These include:

- Several of the components on the Plant Monitoring Module were becoming difficult to source. This would only be resolved by a redesign of the board.

- It was desirable to increase the sampling clock frequencies, without loosing any sampling resolution. This could not be achieved with the existing technology.

- An additional level of processing is required. Current processor performance is such that this processing could now coexist with the main control algorithm implemented on the control and communications processor.

- The cost of the RMDAS unit was effected by the need to have both a Remote System Control Module and a Plant Monitoring Module. The Remote System Control Module was also considered a weak link in the system as had a higher than average failure rate during integration testing and was expensive compared with current Single Board Computer prices.

A system consideration indicated that if the clock circuit of the Plant Monitoring Module could be combined with an industry standard interface compatible with a proprietary Pentium based single board computer, the construction of the RMDAS could be dramatically rationalised. The new board combination would then functionally replace the sometimes unreliable and relatively expensive Remote Control System module and the Plant Monitoring Module.

The parameter improvements effected by the improved design are illustrated in Table 1.

<table>
<thead>
<tr>
<th>Parameters to be Improved</th>
<th>Existing System</th>
<th>Improved System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition speed (equivalent rpm)</td>
<td>3000</td>
<td>9000</td>
</tr>
<tr>
<td>System Modules</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>
6. Description of the technical product improvements.

The improved product architecture is based on a flatter hierarchy by combining the functionality of the Plant Monitoring Module (PMM) and Remote System Control Module (RSCM).

The new PMM unit comprises of a Single Board Computer (SBC) with a custom PC/104 board based clock generator circuit. This system design approach allows the use of a low cost, high performance Pentium based SBC with an Ethernet link and a solid state disk for data storage. The new system configuration is illustrated in Figure 3.

![Figure 3: Improved System Architecture](image)

The design incorporates a number of fundamental changes to the existing system. First the RSCM is discarded. The RSCM not only provided a network connection for the sub-system but also provides power fail recovery. Both functions are provided by the new PMM. This reduces system complexity and reduces system cost.

A Pentium based SBC with DiskOnChip or solid state hard drive, NE2000 compatible ethernet and EPP parallel port is available from several suppliers in a standard format (EBX) with a PC/104 socket. The new clock board with the FPGA device is mounted on the SBC using the PC/104 interface.

The FPGA device is used to implement both the computer interface and the counter logic necessary to implement the speed measurement and clock generation logic. The functions performed by the FPGA device are illustrated in Figures 4 and 5.
The PC/104 interface is organised as a number of read/write registers. These access the working registers of the speed sensing and clock generation circuit. The block diagram of Figure 5 shows the organisation of the internal registers that are implemented in the FPGA.

The revised system design incorporating the FPGA device produces several technical benefits. These include:
• Improved performance. The new design allows signals derived from higher speed sources to be monitored (the equivalent of up to 9000 RPM).

• The new PMM is compatible with the older systems making it possible to use it as an upgrade to existing systems.

• The SBC is a standard issue board available from several manufacturers and suppliers. The standard embedded processor card EBX format defines the dimensions and mounting formats for these SBC cards, and therefore, makes it possible to change supplier if necessary. This reduces dependency of single suppliers and provides a clean upgrade path.

• All the custom logic is concentrated on a single printed circuit board (PCB) that has a low manufacturing cost.

• The acquisition control system logic is on-board programmable, allowing a variety of applications to be considered.

Photograph 2: Picture of single Board computer with P 104 circuit Board Mounted

7. Choice and rationale for the selected technologies, tools and methodologies.

The application requires a technology that can be used to implement a bus interface and extensive control signal and sampling clock logic on a circuit board that conforms to the PC 104 format. The device used should also provide sufficient re-configurability to allow subtle changes in the clock logic to accommodate some future customisation for new applications. A single device that can be reconfigured under software control would be ideal.

To improve the existing product, several microelectronics technology options were considered, including microcontrollers, complex programmable logic devices (CPLDs), field programmable gate arrays (FPGAs) and digital application specific integrated circuits (ASICs).
Microcontrollers and Microprocessors: The main functions to be implemented in the improved Plant Monitoring Module are concerned with speed sensing, clock generation and general I/O. Microcontrollers were rejected because these devices did not provide sufficient hardware support for the complex timer circuits required. Although microcontrollers with counter logic are available the counters are rarely 32-bits wide and cannot be easily combined to provide the required synchronisation between sensing and generation circuits. External logic would be required to implement the required functionality. Additional logic would also be required to allow the device to communicate with the host processor over the standard bus. The solution was therefore rejected.

Complex Programmable Logic Devices (CPLDs): The system currently utilises `low end' PLDs and two programmable counter devices each with five, 16-bit counters. An increase in functionality is also required. It is estimated several CPLDs would be required to perform the desired functions, and the inability to have a single chip solution requires several device pins to be used for interconnecting processor bus signals, and `internal' control signals between these devices resulting in a sub-optimum solution. The enhanced functionality of the system also requires a large number of registers and counters, and as CPLD architectures are generally optimised for combinational logic these devices are inefficient in implementing these functions. These factors, and the adverse impact on board space led to the rejection of this technological option.

Digital ASIC: Digital ASIC devices provide a technically feasible solution to the requirements of the enhanced Remote Monitoring and Data Acquisition equipment. However, the projected sales volumes for the equipment do not justify the significant investment in the production of an ASIC, and this solution was therefore rejected. Additional considerations confirming the rejection of ASICs included the lack of flexibility in expanding the system's capability at a later date, and the degree of risk involved.

FPGAs: FPGA devices offer increased gate density when compared to CPLDs, and allow Prosig to achieve the goal of a single chip space saving solution for the enhanced Remote Monitoring and Data Acquisition equipment. FPGA devices enable Prosig to correct any design errors and undertake several design iterations at a relatively low cost, and consequently this offers Prosig a low risk design route. The unit costs of FPGA devices are relatively high, but these costs are low in relation to the price of the system. The flexibility achieved by having a one chip solution and the low initial costs makes this solution the most economic solution to meeting the increased functionality. FPGA device technology was therefore selected as the most appropriate technology for this application.

The main FPGA technologies available in the market are one-time programmable devices, which are usually based on anti-fuse technology, and re-configurable devices, which are based on static RAM (SRAM) cells. The latter is usually configured at power-up from a memory device located on the same board. Prosig selected for this application the re-configurable devices. This decision was influenced by the following factors:

i. Prosig policy has been to incorporate reconfigurability into any new systems where ever practical. Several variants of the logic of the existing PMM exists and it is entirely plausible that some enhancement may incorporated in installed systems.
ii. Although power consumption is a consideration it is not critical so no significant advantage could be gained through use of the lower power fuse programmed devices.

The final selection of the optimum FPGA device was made during the application experiment and a Xilinx XC4010E device was used.

**Design Methodology**

The design procedure was based on the use a PC-based FPGA development system. The design entry was via VHDL rather than the traditional development of schematic diagrams. This increased the initial risk but it was decided that the nature of the application would be better suited to a VHDL based approach. The company’s design engineer has extensive knowledge of C programming which helped to minimise the culture shock of using VHDL.

The circuit's design was based on the use of a structured approach, and the high level architecture's functional blocks was allocated lower level components. Functional simulation was performed on these lower level components to demonstrate the adequacy of the design. The top level schematic was then tested in a similar manner. Design efficiency in terms of logic block usage and routing efficiency, as well as the impact on signal delays was considered during this stage. The final routed design used signal delay information to perform a final timing simulation on the FPGA design to demonstrate design compliance prior to functional testing.

The Designer software from XILINX was then used to generate the FPGA programming file. The prototype FPGAs are programmed using XILINX loader during development. In the final product the programming file is loaded over the programming port designed into the PC/104 board. The diagnostic test methods for on-line testing are software based. Software reads back register contents to check integrity. Boundary scan test methods were considered but rejected on the basis that the extra registers and control circuits required a larger, and more expensive, FPGA device.

Prosig do not currently possess Automatic Test Equipment, and the relatively low number of products does not justify the investment in such equipment for production testing the final FPGA based circuit boards. The company will use specific software test routines running on the single board computer (SBC), and readily available test equipment and dedicated functional test equipment to demonstrate the correct operation of the production circuit boards.

**8. Expertise and experience in microelectronics of the company and the staff allocated to the project**

Prosig possess expertise in the development of data acquisition hardware and of the signal processing algorithms required for the analysis of the captured data. The company has experience in the software programming skills required to implement the operational code for the embedded microprocessors in the data acquisition systems, and the software development of software for any connected personal computer. The systems designed by Prosig operate in harsh environments, and the company has developed hardware packaging expertise to satisfy extreme levels of physical shock (1000g), and for the management of heat dissipation in systems designed for the automobile market.
Prosig's hardware development experience is limited to the development of accurate analogue signal processing circuitry, analogue to digital conversion, and the development of processor systems. The digital design experience of the company is limited to the development of logic circuits using discrete components (registers, counters, etc) or low level integration programmable logic devices (PLDs).

The company had no design experience in the development of FPGA based circuits. Prosig did not use high level digital design tools or simulation methods, beyond the use of test vectors for PLD design and manufacturing test.

The work undertaken on the project was carried out principally by two employees. The Systems Director a graduate computer science engineer who has been with the company for 20 years and the Principal System Engineer, who had no formal electronic qualifications, but has over 20 years practical exposure to electronics systems.

9.       Workplan and rationale

The rationale for the workplan was that the First User needed to gain a full understanding of the new technology, in order to be able to apply it to future projects. This was not a one-off project. Maximum participation and understanding was therefore required throughout.

The workplan for the project was broken down into different tasks as follows:

Specifications

This task involved the preparation of the following documents:

• A System Requirements Specification that defined the functions to be performed by the improved Plant Monitoring Module (PMM) module. This document was prepared by the company Technical Manager.

• An FPGA Device Specification which defined in detail the low level functions to be performed by the FPGA, the timing relationships between external signals, diagnostic test requirements, and the physical features (including device packaging and power requirements). The company’s Technical Manager produced this specification after the initial systems design had been completed, and with assistance from the subcontractor.

• The System Test Acceptance Specification which defined the complete range of functional demonstration tests to be conducted to demonstrate that the FPGA based equipment met it's requirements, and that all modes of the FPGAs operation were fully tested.

Design

The design task comprised of the following activities:

• Systems Design - involving the high level partition of the PMM clock and I/O function requirements to individual component groups in the equipment. In particular, the systems design task confirmed the functions to be performed by the FPGA, the FPGAs interaction with other system components, and the device type to be used. The role of
the subcontractor was to provide interim and final reviews of the initial systems design produced by the company's engineers.

- **Circuit Design** - This involved the design of the complete PC/104 circuit. This included the design of interfaces to devices currently connected to the PMM, and the design of the PC/104 interface to the FPGA. This task involved the creation of schematics for the PC/104 board and the creation of new designs, using VHDL, for implementation of the clock circuits within the FPGA device. This task was undertaken by the company engineer with advice from the subcontractor.

- **FPGA Design** - During this task the FPGA circuit design was allocated to logic blocks within the FPGA using FPGA macros wherever possible, and the layout and interconnection of these logic blocks undertaken. Several iterations were performed to ensure that the performance of the FPGA, as indicated by timing and functional simulation was achieved, and that the device area usage was acceptable. Pin allocation for the device inputs and outputs were also confirmed at this stage. Again, this was carried out primarily by the company engineers.

- **Circuit Board Design** - This task involved the design and layout of a new circuit board to accommodate the FPGA and was done in-house by the company engineers. At an early stage during familiarisation training with the FPGA, it was decided that instead of using examples from the training manual, a “real” example would be used, based on a very much-simplified version of the application experiment. For this, a simple PCB was designed. This proved highly successful and, with minor modifications was used as a first prototype board for the AE.

- **Software Design** - This involved the development of a software interface resident on the single board computer to provide the PC/104 interface with equivalent functions to that in the existing PMM application software and provided the basis for diagnostic software for the FPGA. The task was performed entirely by the company’s engineers.

**Test**

The testing task involved the following activities:

- **Design Simulation** - This involved the detailed simulation of both the circuit design expressed as a hierarchical circuit schematic drawing, and the timing simulations for the routed FPGA device. These tasks were completed prior to the assembly of the circuit board and FPGA programming.

- **FPGA Functional Test** – As the FPGA device was designed to provide a standard computer interface, the programmed FPGA device was initially tested using dedicated PC based software routines. Testing also utilised external test nodes and the use of built-in test circuitry to ensure the FPGA's functions were performed correctly.

- **Circuit Board Testing** - The assembled circuit board was functionally tested using currently available test set-ups, and any modifications required to the hardware design were implemented.

- **Acceptance Testing** - The operation of the FPGA was demonstrated using a demonstration of the FPGA circuit board in an assembled equipment against the
Functional Acceptance Specification. Successful compliance with the requirements of this test specification concluded the application experiment.

The testing tasks were conducted primarily by the company engineers, with support and advice from the subcontractors in FPGA simulation and test methods.

Training

Training was conducted by the sub-contractor and provided the two company engineers with sufficient knowledge of the specific FPGA device and on FPGA development systems using dedicated CAD tools, to enable them to carry out the application experiment with subcontractor support. On the job training assistance, incorporating reviews of the design solutions produced by the company's engineers, was also provided.

Management

The management of any new technology implementation is important, to ensure control, to ensure the objectives described in the proposal were achieved and to gain the ability to replicate the application. The task includes all the liaison activities, and project management and cost tracking and control activities required for the application experiment.

The knowledge transfer process incorporated formal training in FPGA device design, and through project subcontractor assistance in the areas of digital systems design methods, VHDL implementations, simulation methods, and CAD tool use. This support process involved the subcontractor providing detailed technical support when requested by the company during the application experiment. The knowledge transfer process was also assisted by the development of a prototype circuit board early in the application experiment, and the initial trial FPGA design developments based on this circuit board.

The timing plan for the application experiment shows the planned duration and the actual duration for each activity. The major timing deviation occurred early in the application experiment, where the initial specification task took longer than anticipated. The reasons for this variation was the fact that the company engineers involved needed some more confidence in the technology before being prepared to sign off a formal requirements specification. This confidence arose from the parallel training in FPGA device technology which included the evaluation of tutorial packages, and the development of a small prototype board as part of the training process. This enhanced design confidence thereafter lead to the completion of the majority of the following tasks within the allocated time and in the planned sequence, albeit in some cases delayed. The availability of the prototype board developed as part of the initial training allowed the final FPGA design task to be conducted in a quicker time, thereby enabling the original project duration to be maintained.

Overall, the application experiment ran more smoothly than had the company had feared would have been the case, and the company engineers were pleased with their ability to assimilate the knowledge transfer they required. There were no major variances to plan in the resource required for the various tasks.
<table>
<thead>
<tr>
<th>Workpackage</th>
<th>Planned Company (days)</th>
<th>Actual Company (days)</th>
<th>Subcontractor cost (kEURO)</th>
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<td>Training</td>
<td>5</td>
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<td>1.4</td>
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<td>Specification</td>
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<tr>
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<td><strong>Total</strong></td>
<td><strong>147</strong></td>
<td><strong>162</strong></td>
<td><strong>13.4</strong></td>
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Table 2 Work Package Costs
### Workpackage 1:

1. **1.1 Systems Requirement Specification**
   - 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39

2. **1.2 FPGA Design Specification**
   - 2, 3, 4

3. **1.3 System Test Specification**
   - 4

### Workpackage 2:

1. **2.1 Systems Design**
   - 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39

2. **2.2 Circuit Design**
   - 1, 2, 3, 4

3. **2.3 FPGA Design**
   - 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39

4. **2.4 Circuit Board Design**
   - 1, 2, 3

5. **2.5 Software Design**
   - 4

### Workpackage 3:

1. **3.1 Design Simulation**
   - 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39

2. **3.2 FPGA Functional Test**
   - 1, 2

3. **3.3 Circuit Board Test**
   - 1, 2

4. **3.4 Acceptance Testing**
   - 1, 2

### Workpackage 4:

1. **4.1 Training**
   - 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39

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**Actual** = x

**Plan** = □
10. **Subcontractor information**

Prosig undertook a thorough examination of the external inputs required for the Application Experiment, including the identification and participation of the subcontractor involved. The subcontractor needed to bring to the experiment skills and knowledge that were particularly relevant to this application, having been involved in other similar FPGA developments.

A number of alternative sub-contractors were considered.

The selection criteria included:

- Extensive experience in the selection of FPGA devices to meet specific functional requirements
- Previous experience in designing and developing FPGA designs
- Experience in the use of a wide range of design CAD tools for FPGAs
- Previous knowledge transfer and design support experience

The selected subcontractor, the Centre for Electronic Product Engineering (CEPE) at the University of Glamorgan, beside meeting these criteria was also an UK Department of Trade and Industry (DTI) selected design support centre. As a consequence of these factors, Prosig selected CEPE to provide the training and design assistance support to the company during the application experiment.

The contract for the sub-contractor made provision for stage payments upon completion of deliverables and training separately, and for retention of IPR by Prosig. There was no specific penalty clause included for late delivery.

11. **Barriers**

In giving consideration to adopting FPGA technology in the company, Prosig had identified several areas that are perceived to be potential barriers to ensuring the successful completion of the project. These barriers are as follows:

**Lack of Knowledge**

Having identified the need to develop the product and the technology route to accomplish that development, Prosig was aware that they did not have the necessary skills in-house to undertake the project on their own.

Whilst being relatively conversant with modern electronics technology, Prosig had no prior experience of using FPGAs. Being a small company, Prosig have a highly developed skills base in other areas, and the challenge was to encourage existing staff to take on board the FPGA technology.

**Lack of Technological Expertise**

Prosig were already familiar with microelectronics technology, but had no expertise in the field of FPGA technology. Quite often in small companies, the will to learn new techniques is there, but other constraints such as lack of time or lack of resources prevent or frustrate this process. Fortunately, the fact that Prosig have used other forms of microelectronics
technology meant that the staff were receptive and open-minded when it came to introducing the new technology to the company. Working with subcontractors to introduce technology into Prosig is an area in which the company had some concerns: Prosig had to ensure that they were in a position to grasp FPGA technology and successfully capitalise on their experience through FUSE, so that other products could benefit with this technology.

**Financial Risk**

As with all aspects of business which are ‘new’ to a company, there are always real or perceived risk associated with the introduction of something new. This element of ‘risk perception’ is particularly apparent when it comes to the field of new technology. Within this field, the greater the complexity of the technology, the greater is the ‘perceived’ risk, as assessed by the company. However, in many cases, adopting ‘high-technology’ solutions, particularly in microelectronics, need not mean associated high risk. Prosig were concerned that any such introduction of new technology did not leave them exposed or at risk, either financially or commercially.

12. **Steps taken to overcome barriers and arrive at an improved product**

Prosig carried out a thorough examination and risk assessment of this project, in order to develop the FUSE proposal. Working closely with the TTN at University of Glamorgan and representatives of the Centre for Electronic Product Engineering, Prosig agreed a format that they believed would overcome the barriers identified.

**Lack of Knowledge**

Prosig found that their perceived lack of knowledge was not be a barrier to the success of their Application Experiment. Having already worked with the subcontractor and the TTN to carry out the preparatory work forming the feasibility study and proposal, Prosig became conversant and comfortable with FPGA technology. This process of gradually reducing the barriers continued throughout the duration of the Application Experiment. Prosig found that having both the subcontractor and the TTN to provide support, advice and training had a vital impact on the successful introduction of FPGA technology to the company.

By choosing the selected subcontractor and design methodologies that use existing technology, Prosig found that the development risk could be managed. In addition, the training undertaken at CEPE enabled Prosig to intelligently review and participate in the tradeoff decisions and carry out a risk assessment of each milestone. This contributed greatly to the successful outcome of the project.

**Lack of Technological Expertise**

In practice we found that the main barrier was actually a cultural one. The knowledge barrier was largely a perceived problem that did not materialise. The confidence obtained by going through a simple tutorial with the XILINX Foundation package in conjunction with an evaluation board was significant. This was reinforced with some informal training with the subcontractor. A factor in our favour was our software background, the similarities between the synthesis tools and various software development environments made the environment feel familiar. Also, although the implementation details of the various FPGA architectures are still not clearly understood this did not seem to impair our progress in the implementation of the design. This was a cultural barrier for our design engineers, as few designers will feel
comfortable designing a circuit with a device they do not fully understand. Because the perceived technological risk was reduced at an early stage then the perceived financial risk was also reduced. This was reinforced by trying to keep the development work required to gain experience with the new technology clearly focused to avoid dilution by tasks which were necessary to the project but which did not advance our knowledge or confidence in our ability to use the technology.

**Financial Risk**

Concerns about the financial risk of the project were reduced in the early stages once Prosig’s engineer had gained some hands on experience with the tools. This was further reinforced when we had some developed a simple prototype board with the target FPGA device mounted on it and we had loaded some simple logic. This gave the whole team confidence in the approach taken.

13. Knowledge and experience acquired

The application experiment has allowed Prosig to gain for the first time knowledge in FPGA product development. The knowledge gained by the company includes the following:

i. Technical management skills in the development of FPGA products.

ii. Specification skills for FPGA, including the development of skills in the selection of the appropriate FPGA device technologies to meet functional requirements.

iii. Digital design methods, including skills developed in top down design and simulation methods.

iv. The use of CAD design tools in the development of FPGAs.

v. Design skills in the routing and placement of functional ‘blocks’ within the FPGA device, and the design trade-offs involved in this process.

vi. The development of test strategies for the FPGA device, including the acquisition of knowledge in the use of test pattern generation and boundary scan techniques.

Overall, the acquisition of these skills and the knowledge transfer achieved, exceeded the original expectations of the First User, particularly with regard to their confidence in its further application.

14. Lessons learned

The cultural impact of introducing the FPGA technology into the company has been significant. Most of the previous design work has been with small scale devices. Although there was an awareness of the capabilities of larger scale devices the actual realisation of the potential with respect to our product development was not fully appreciated until some experience was gained with these devices.

The company’s engineers gained enough confidence using the small development board supplied with the XILINX Foundation software to undertake the design of a prototype board with a 10,000 gate device at a very early stage of the project. It is advised that other first users also investigate the availability of simple starter kits with their FPGA device suppliers to build up initial confidence levels.

The development of a simple prototype board by the company early in the application experiment not only made the design engineers feel comfortable with the new technology but
proved a useful demonstration for senior management not involved in the project. The prototype board actually got very close to being the final design for this project and was used for most of the development and testing. This approach is advised as one method of building up the design expertise of the others considering FPGA adoption.

The big difference between the FPGA prototype board design and previous designs was that the circuits for the logic to be implemented on the FPGA was only established in an outline form. This proved to be sufficient but for the allocation of physical pins of the device. The device had different types of pins and the full implication of the restrictions associated with each pin type was not fully appreciated when the prototype board was designed. This was the only occasion when the decision to go to a prototype board early in the project caused a problem. This was also a decision we made in isolation from our sub-contractor and this limitation could have been avoided had we brought them in at this stage. This did not detract from the effectiveness of the prototype board but stopped it from being the final product. It is advised that technical advice is sought for the pin allocations before committing to the first FPGA circuit board layout.

The company’s original intention was to use a schematic design methodology as the level abstraction between VHDL and the target hardware seemed too great. The promise of VHDL was therefore viewed with some scepticism. However the heavy bias of software experience within the company meant there was a strong bias toward the use of VHDL and this won through. Again this decision was greatly aided by the comfort of producing hardware at an early stage.

The software tools, although easy to use in terms of the steps required to synthesise the design, add another dimension to the knowledge base required to use the device. To use the tools proficiently requires time to become familiar with the user interface and training is required to help understand how the various software settings and switches effect the synthesis process. Adequate time should be built into the first design activity with FPGA devices to allow for this familiarisation process.

Familiarity and regular use of the design tools are are essential to achieve a good level of productivity. Retaining the knowledge gained is not be easy without regular use of the tools and there is also a case for establishing an in-house expert to ensure the skills are focused.

Simulation proved to be a useful tool. In most of our previous designs, the company did not employ simulation to verify the design. The tools tried in the past were cumbersome and did not reflect the true timing of the circuit. The simulation facilities were used to great effect in the main design. As a result our general design skills have been improved and we have become convinced of the benefits of simulation.

An important feature of the design and simulation process is that it can flow freely. The final design took up to 20 minutes to complete the compilation and synthesis process on a 200 Mhz Pentium with 32 MB of memory. Whilst this type of PC is acceptable for most applications it was felt that a much higher performance PC would have had quite an impact on productivity. Other first users of FPGAs should consider the capability of the PC platform to be used.

15. Resulting product, its industrialisation and internal replication
The enhanced Protor system is now in the final stages of development. The product improvements identified in section 6 have been successfully achieved.

There were two main target areas for improvement. The first was in improved performance. This was achieved through the use of a custom design of the clock logic. The use of 32-bit counters and a higher base clock frequency provide the necessary improvement in the operating range of the speed sense and clock generation circuits. The second aspect of the product improvement was to be in reducing the system cost thus making the unit more competitive. This target has also been met. In fact since the start of the project the replacement hardware has reduced even further in cost. The increased use of commercially available single board computer boards has also reduced our in house design load.

The further industrialisation of the prototype PMM board is restricted to the following activities:

i. Modification of the RMDAS chassis design to replace the existing board (RSCM and PMM) with the single board computer and the FPGA based PC/104 card.

ii. Porting of the existing software to the new system.

iii. Performing in house trials with the new system.

iv. Performing field trials with the new system.

No special test equipment is required to support the improved system as the existing test harness can be used.

Finally once the system has been proven EMC tests will be performed on the RMDAS chassis. It is anticipated that the full industrialisation of the improved product will follow the timeplan given.

<table>
<thead>
<tr>
<th>Task</th>
<th>Description</th>
<th>Completed By</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Modify Chassis Design</td>
<td>May 99</td>
</tr>
<tr>
<td>2</td>
<td>Porting of RSCM software to new board</td>
<td>June 99</td>
</tr>
<tr>
<td>3</td>
<td>Porting of PMM software to new board</td>
<td>October 99</td>
</tr>
<tr>
<td>4</td>
<td>In House Testing of enhanced RMDAS unit</td>
<td>November 99</td>
</tr>
<tr>
<td>5</td>
<td>Field Trial of Protor system incorporating enhanced RMDAS unit</td>
<td>December 99</td>
</tr>
</tbody>
</table>

The industrialisation costs are estimated as 20 KEcu.

Since the introduction of the technology to the company it has been used in a number of projects and further product enhancements are being considered. The replications include:

- **A General Purpose Parallel PC Interface**

  The original prototype board for the Protor project has been reprogrammed to act as a general purpose parallel interface. The modified interface is being used in conjunction with a Pentium mother board to provide a ‘black box’ Ethernet based data converter unit to allow data to be transferred into a Windows NT based display system in real-time.

- **Serial to Parallel Converter**
A new circuit board has been designed which incorporates a CPLD device to implement an enhanced bi-directional serial to parallel converter. This will be programmed using VHDL.

- **Updated DPX Board**
  A new board is being designed which will replace a design implemented with discrete 7400 based logic. The VHDL code is a subset with some modifications of the Protor VHDL and the board will be much smaller and cheaper to manufacture.

16. **Economic impact and improvement in competitive position**

The FPGA implementation realises several cost benefits. These are achieved as a result of the following factors:

- Replacing the existing RSCM and PMM modules with a proprietary single board computer and custom PC/104 peripheral board reduces the typical cost of a 24 channel RMDAS unit by over 20% in raw materials alone. The total cost saving is probably higher as the system build procedure will be simplified but it is not possible to quantify the cost savings at this stage.
- Cost savings achieved through reduced power consumption, less rack space and interconnecting cables.
- Reduced maintenance costs as the cost of spares is reduced and the system is less complex.

The reduction in RMDAS unit cost reduces the cost of a typical Protor system by between 4 and 8%, depending on the size of the system. The lower cost of the RMDAS unit will have a larger impact on the cost of the smaller systems.

This reduced system component cost will increase the price competitiveness of the product. The improvement in price competitiveness and the reduction in costs will not improve the profitability of the system in itself, but will result in additional sales and hence increased overall company profits.

In addition the Protor system has been enhanced by increasing the data acquisition rate for the system. The improved performance of the Protor system will result in additional sales where the main plant to be monitored has a high shaft speed which cannot be supported with the existing system, or by enabling the system to provide monitoring support for additional plant. This is an important advantage, as the company is aware of installations where existing systems are being extended to cover extra plant as the customers appreciate fully the benefits of plant monitoring.

The impact of the cost and performance improvements in the existing system is illustrated in Chart 2. The chart illustrates that sales of the enhanced system will increase by 8% per annum. The company attributes 4% of these additional sales as coming from the lower product costs and another 4% coming from increased product functionality. As the Protor sales contribute 30% of the company’s turnover, company profits will increase by approximately 3% in the first full year of sales of the new product.
Chart 2: Sales Projections for the Existing and Improved System

Based on the company’s current profitability levels the return on investment (ROI) of the prototype development costs of 27 KECU over the product life of 5 years is anticipated to be 500%. The ROI in the first year is anticipated to be a 75%.

The payback period for the investment costs in developing the prototype system is 13 months.

The industrialisation costs are estimated as 20 KECU.

17. Best Practice and Target Audience

This application experiment has demonstrated best practice elements in terms of knowledge development, including the use of prototyping circuit boards in developing the design skills, good specification processes, and the utilisation of the design skills in terms of other replications. This information will be available be of value to other organisations currently evaluating the commercial and technical benefits of FPGA technology within the FUSE programme.

This experiment will be of considerable interest to a organisations involved in the design, manufacture and supply of data acquisition and data processing systems. Specifically, the two sectors which will have particular interest in this application experiment will be the automobile and power generation industries. As a small company and a first user of FPGA technology, the dissemination of the company’s experience is expected to be of considerable value to technical and commercial managers of other similar organisations in this engineering sector.

The target industry sector codes are:
- Instrumentation (Prodcom code 3320)
- Automotive (Prodcom code 34)
- Energy Generation (Prodcom Code 41)
- Machinery (Prodcom code 41)