

FUSE DEMONSTRATOR DOCUMENT

MONITOR FOR DENTAL FURNACES

AE No : 26243

ASSOCIATED TTN : INTRACOM

July 1999

This document has been prepared mostly by Prokopis Prokopiou. He was working on this, till Sunday 22nd of November 1998 and time 12:26:00.

Prokopis Prokopiou was killed in a terrible car-accident on Sunday 22nd of November 1998 at 14:15.

KEL's staff and the Applied Electronics Laboratory's staff will remember him forever.

Abstract

KEL is a well-known Greek manufacturer of dental equipment. The company supplies the local market since 1988 with high technology furnaces used by dental laboratories specialised in construction of artificial teeth. Since 1997, KEL also manufactures one of the most advanced worldwide casting machines, also used by dental laboratories. The main products of the company, so far, are the vacuum porcelain furnaces.

The objective of this application experiment was to implement an FPGA, which would adapt the porcelain furnace microprocessor to new peripherals. The main, and most demanding, peripheral is a VGA monitor, which has replaced the Hercules monitors that were used by the original design of the furnace. The need of high speed digital circuits along with the non standard for VGA monitors format of the images generated by the software of the furnace, had made the conventional design of the VDU card non functional. MSI circuits of High Speed CMOS technology could no longer support the new monitors and the company lost a huge share of the local market the last 4 years. The FPGA implementation of the VDU card turned out to be the most efficient way as it offered high speed, flexibility in the design, small size PCB, short time to market and relatively low production cost.

The project lasted 11 months with a company effort of 12.5 person-months and a funding of 61.6 KECUs.

KEL is expecting to increase the net profit of the company by more than 100 KECUs for the year 1999. A prototype introduced during an exhibition in Athens (September 19th). The company started (September 1998) the production of the SAT (Series 4) porcelain furnace model and 5 pieces have already been sold (end of November 1998). Estimated payback period is 7 months from the end of AE. The FUSE ROI ratio for the next 3 years (1999 - 2001) is expected to be 672% as the net profit will exceed the 400 KECUs.

The main issue from the AE for KEL was the economical one as the company straggled for a couple of years after the loss of the market. A second issue is the adopted technology. The company already plans to apply the FPGA technology to the casting machine increasing significantly the functionality of the device. KEL also values the co-operation with the University of Patras, which acted as a subcontractor and is looking for a permanent co-operation in the future.

It is believed that the experiences and lessons learnt through this experiment by KEL will be of interest and benefit for companies with conventional capabilities on microelectronics and have to improve their products using a new technology.

Keywords and signature

Keywords : FPGA technology, dental furnaces, display unit, medical & surgical equipment, precision instruments

Signature : 3-01415550420-2-3310-1-33-GR

1 Company name and address

Company name: KEL I. KIRIAZOPOULOS & CO G.P.
Address: 14 Stavropoulou St. GRE 265 00 Rio - Patras Greece
Phone: +30 61 99 0646
Fax: +30 61 99 0746
E-mail: kel@otenet.gr
Contact: Mr. Stergios Roudis



2 Company size

KEL's turnover is about 200 KECU. The company currently employs 7 full time people, 5 of them engineers, in the production and research fields. The experience in the electronic field is wide, since both analog and digital design is used to implement the electronic part of the products. Four of the company's personnel are highly experienced in electronic design and PCB design, involving discrete components (analogue and digital). The company personnel have also excellent experience in the microprocessor field, both in hardware and software design. After the AE, two of the company engineers have sufficient experience in VHDL, and FPGA based design.

The personnel involved in this AE were:

Mr. Ioannis Kiriazopoulos, who had the overall management of the project,

Mr. Stergios Roudis, an electrical engineer and specialist in electronic design and PCB design. He was the main link of the company with the engineers from the University of Patras and was involved in specifications, FPGA design and PCB design.

Mss. Sotiria Tsekoura, an electrical engineer and specialist in production engineering and quality control. She, along with Mr Roudis, was involved in the FPGA design and market research.

3 Company business description

KEL is a small Greek Company established in 1988 specialized in the field of high precision dental equipment such as Porcelain Furnaces, Inductive Casting Machines and Preheating Furnaces. The company has activities mainly in the local market where it holds a good share. The company engineers have designed all of its products. The production line of the company is capable of producing more than 300 devices a year of a total amount of 800 KECUs, although the actual production is significantly smaller due to local market size. KEL also has a well-organized sales department with 8 sales points in Greece and 1 in Cyprus. The company engineers are responsible for the installation of the devices in the customers' laboratories and for the maintenance, along with 5 cooperating technicians, covering Greece and Cyprus.

KEL has emphasized on the reliability and the quality of its products. A short description of them is listed in the following paragraphs:

There are two models of porcelain furnaces, the SAT 4 and the BRAIN 4. These equipment can perform accurate firing cycle in the range of 100°C-1200°C at a high resolution and accuracy (1°C). Moreover these equipment can generate adjustable vacuum in the oven of the

furnace and to control the position of the automatic door. The difference between the two models is on the user interface. The BRAIN model has a 2X40 LCD screen whereas the SAT has (due to the FUSE/FILECUP project) a VGA monitor. Both apparatus are controlled by a CPU based system that employs advance techniques on measurement and control resulting to their high reliability, efficiency and flexibility.

The preheating furnace (DEDALOS 4) is used for the formation of the dental muffles. The firing circle required for this procedure is extremely long (1-3h) and requires accurate control of the temperature (2°C), at a high range (100°C-1500°C). The advantage of this apparatus is that can achieve accurate increments of the temperature in a range (3°C-60°C/min). This apparatus is also controlled by a CPU based system that employs advance techniques on measurement and control resulting to its high reliability, efficiency and flexibility.

The inductive casting machine (Hephestos 4) is used for casting the metal in the dental muffle so as to form artificial teeth. This apparatus has the ability to melt and preheat at a programmable temperature several types of alloys in a sort time (15-45 sec). Afterwards, it casts the metal in the muffle at a programmable acceleration that can be as high as 150 g. This apparatus is controlled by a CPU based system that employs advance techniques on measurement and control resulting to its high reliability, efficiency and flexibility. Additionally is equipped with a special signal processor that controls the 4KW high performance amplifier.

KEL also sells some other products related to the dental activities such as consumables (alloys, porcelain powder) and products such as steamer for dental applications, boding apparatus and apparatus to polymerize dental acrylic.

4 Company markets and competitive position at the start of the AE

KEL is focused mainly in the domestic market. The main competitors are two Greek manufacturers and three importers who represent JELENCO (USA), IVOCLAR (Liechtenstein) and VITA (Germany).

The Greek market is sized from 1900 dental laboratories employing approximately 4.400 dental technicians. The market is sensible to the type of monitor used rather than the price. We estimate that the market is 70% sensible to monitor and 30% sensible to the price of the furnace. Concerning the company's products, the customers statistically prefer the CRT monitor from an LCD one in a rate of approx. 3/1 .

Similar competitor's products are priced higher than KEL's ones.

KEL Pricing:

SAT 4 (monitor).....	3000 ECU
Brain (LCD).....	2600 ECU

IVOCLAR

Model 80.....	4500 ECU
Model 95.....	5500 ECU

VITA

VacuMat.....	4000 ECU
Model 2500.....	5300 ECU

De Trey

MultiMat 1.....	3500 ECU
MultiMat 3.....	5400 ECU

KEL manufactures three different devices.

1. The preheating furnace

This product will be affected from the current AE in the future as it shares the same CPU card with the porcelain furnace. There is an average of 2 preheating furnaces in each Greek dental laboratory amounting a total of almost 4000 devices in the Greek market. The mean

lifetime of those furnaces is 12 years sizing the market to 300 - 350 units a year. KEL has a small share of this market (14-16%) and has supplied the Greek laboratories with 230 units so far. The company's sales are approximately 60 KECUs with a net profit of 42% (25 KECUs).

2. *The casting machine*

The casting machine market is a developing one in Greece. Not more than 12% of the Greek Laboratories are equipped with these devices. Sales in Greece before 1997 were at a very low level as, due to the high cost of the devices, there was practically no pay back for the investment. KEL introduced its casting machine early in 1997 and sold 12 units the same year and 33 units during 1998 (until September) far ahead from the total sales of all the company's competitors together. The company estimates that annual sales will exceed 50 units amounting more than 230 KECUs with a net profit of 45 % (103 KECUs).

3. *The porcelain furnace*

This product is involved in current AE. The estimated number of porcelain furnaces already sold in the Greek market is 1700-1800, 650 of which have been supplied by KEL. Thus, with an 11-year mean lifetime for each unit, the Greek market is sized to an average of 165 porcelain furnaces sold per year. KEL domains the market from 1991 until 1994 with a share that peaked at 78% in 1993. The best selling models of porcelain furnace were the SAT models (SAT-II and later SAT-3), both equipped with a *Hercules* type monitor. The company's customers did not prefer the BRAIN models that were equipped with LCD display.

During 1994, KEL introduced BRAIN-3, an identical to SAT-3 porcelain furnace, with an LCD unit replacing the declining company's stock of *Hercules* monitors. The result was that the company's sales dropped significantly during 1995 and 1996. At the same time, IVOCLAR regained most of its share that it had before 1991 and KEL's main Greek competitor almost doubled the sales of a PC based porcelain furnace equipped with a monochrome standard VGA monitor. In Figure Fehler! Unbekanntes Schalterargument. we present the effect of the withdrawal of the *Hercules* monitor in the company's sales.

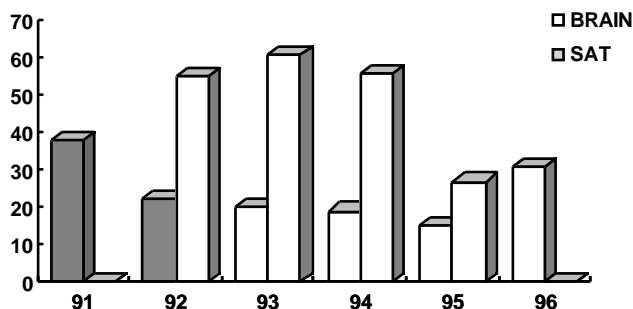


Figure Fehler! Unbekanntes Schalterargument. The sales of the BRAIN (LCD display) and the SAT (HERCULES monitor) furnaces. In 1992 the SAT-II was introduced and dominated the market. In 1995 the sales of the SAT-3 were reduced due the company's limited stock of the *Hercules* monitors. In 1996 there were no *Hercules* monitors available.

Before the AE, the Company's sales have had dropped from 87 pieces (1993) to 22 pieces (1997) and 18 - 24 pieces in 1998 (14 pieces until September). The main reason for this continuous reduction was due to the old product which had no advantage compared to similar competitor's ones. Basic competitive strengths (like smaller size, lower cost, higher reliability and compatibility with not only HERCULES but also VGA monitors) were missing from the previous product.

For an average of 20 units per year, the company's sales amount 65 KECUs with a net profit of 40% (26KECUs).

After the AE, the SAT-4 model incorporating the CRT monitor is expected to regain the market. KEL plans to sale more than 80 units from December 1998 to the end of 1999 and stabilise its sales to 75-90 units a year for the next 2 years. Due to the new more compact

design of the furnace, the estimated net profit will increase to 48%. The annual income of the company will exceed the 265 KECUs and the net profit the 127 KECUs, 100 KECUs more than the net profit before the AE.

5 Product to be improved and its industrial sectors

All the products of the company are microprocessor controlled to ensure the highest performance and reliability. The software that supports the devices is continuously upgraded and updated to keep the devices up today to the scientific and technical innovations in the dental area. Moreover, hardware and mechanical redesigns result to the presentation of new models every 3-5 years while applying the latest available technology in manufacturing process. The total effort of the company is three-fold: product research, mechanical design, hardware and software development.

This project is focused in one category of the company's products, the porcelain furnaces.

The functional layout of the present electronic part of the unit is depicted in Figure Fehler! Unbekanntes Schalterargument. and it is mostly a conventional design.

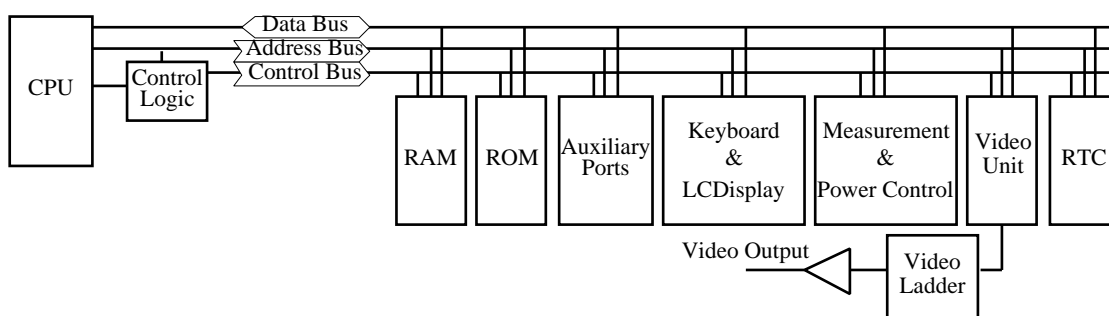


Figure Fehler! Unbekanntes Schalterargument. The block diagram of the existing electronic part of the devices.

The control signals of the CPU and some of the higher address bits are combined to generate the Control Bus of the system. For this reason, five commercial available SSI digital ICs are employed. The system employs two Auxiliary Ports that are implemented by two 20 pins ICs. The Keyboard and the LCD unit are also implemented by the use of two 20 pins ICs. The Measurement and Power Control is the most complex unit of the system since it has to measure very high temperatures with an improved accuracy. The digital part of this unit employs two ICs. Finally, the timekeeper of the system is implemented by a Real Time Clock (Motorola's MC146818ACP) and it will not be affected by this implementation.

The developed FPGA will mainly implement the Video Unit. The video unit is an option in today's units and is mounted on a separate PCB. It employs eighteen SSI and MSI IC's, a ROM and a RAM. All these ICs, except for the RAM, will be included in the FPGA. The functional layout of the Video controller is depicted in Figure Fehler! Unbekanntes Schalterargument. In the future, the company plans to integrate the CPU card and the VDU card in a single PCB, extending the functionality of the FPGA so that it will implement the Control Unit, the Auxiliary Ports, the digital part of the Measurement and Power Control circuitry, the Keyboard and LCD interface as well.

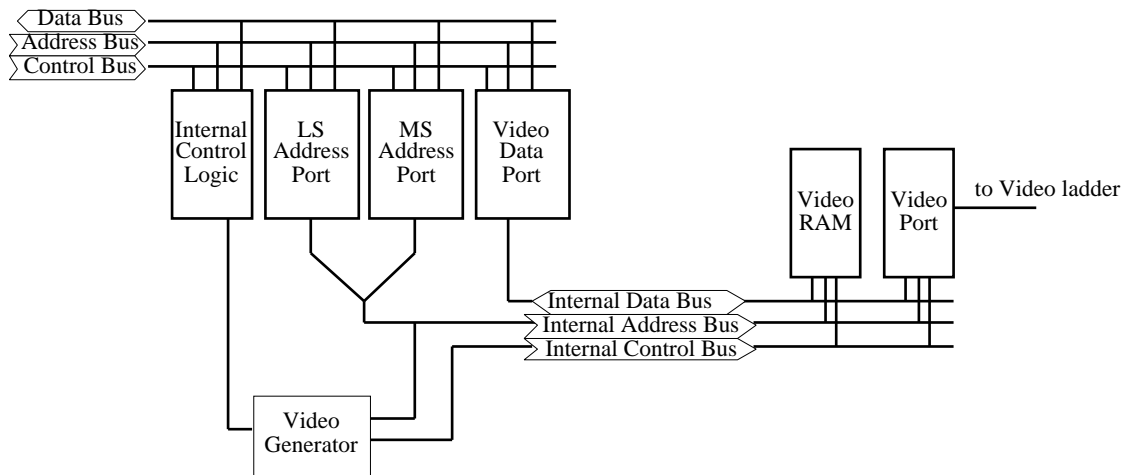


Figure Fehler! Unbekanntes Schalterargument. The block diagram of the Video Unit.

The CPU accesses the Video RAM by assigning the address, the data and the operation to be performed. All this information is stored in the Least and Most Significant Address Ports, the Video data Port and the Internal Control Logic. The Video Generator is responsible to access both the proper byte of the Video RAM and pass it to the Video Port and serve the CPU request by polling the Internal Control Logic. This scheme works successfully for the CGA and the *Hercules* monitors, but fails to create the proper video output to drive the VGA monitors since the clock for this type of monitor should be 27MHz. The developed FPGA overcomes the speed barrier and increases the flexibility of the design.

6 Description of the technical product improvements

The developed FPGA to be used in the porcelain furnaces has replaced a lot of discrete components used by the earlier version of the VDU card. A photo of the new product is given.

It should be mentioned that the new FPGA is hardware and software compatible to the old HERCULES driver so that the rest of the system does not have to be changed and thus the



upgrade of the old system is straight forward. In other words the new board replaces the previous ones without any change in software since the FPGA has the capability of switching from HERCULES to VGA.

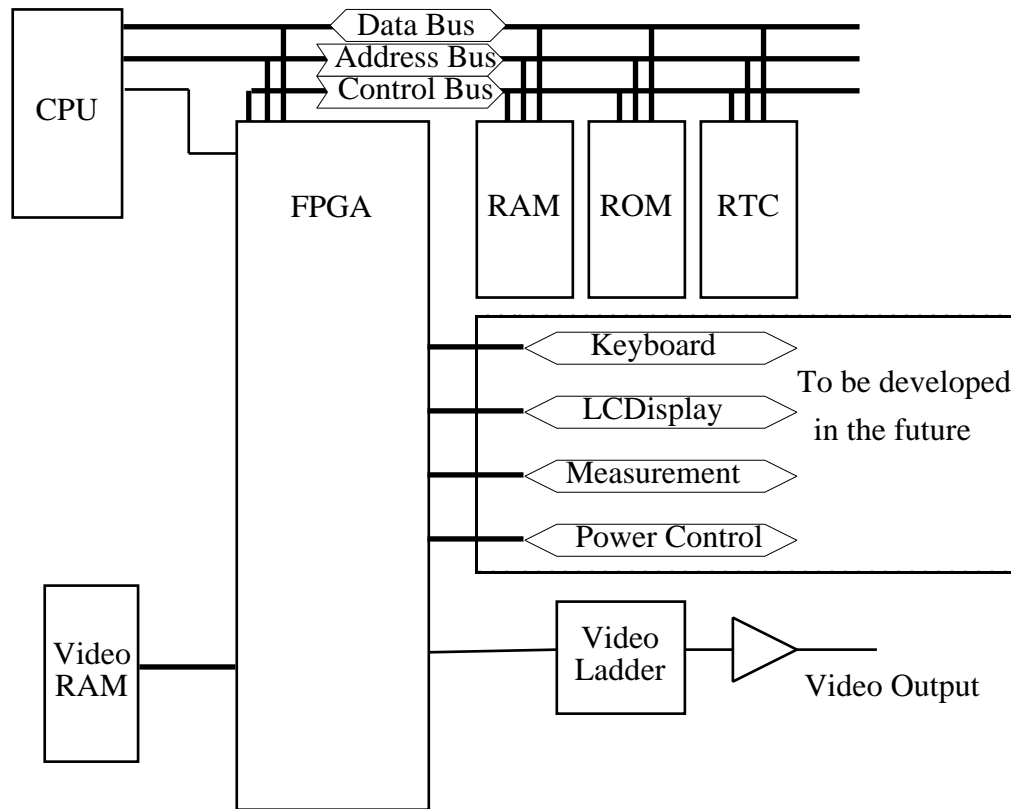


Figure Fehler! Unbekanntes Schalterargument. The FPGA based electronic part.

In Figure **Fehler! Unbekanntes Schalterargument.**, the developed configuration using an FPGA is depicted.

The most crucial part of this application experiment is the VDU. This has been designed so as to achieve in a VGA monitor the resolution attained with the *Hercules* one. This has been achieved as the FPGA based VDU satisfies the Horizontal and Vertical scan rates of the VGA monitor. The VGA monitors have excellent tolerance on the number of the vertical lines that they have to display. It has been tested that the 348 lines of the *Hercules* vertical resolution can be successfully displayed in the VGA monitor. Thus, the FPGA based VDU can be considered as a **hardware stretcher** of the *Hercules* resolution within the VGA scan rates.

Moreover, there is a color option of the VDU. The color output from the VDU will be realized in a hardware way. The color option of the VDU requires some predefined windows to be filled with a predefined color. These windows are activated in a hardware way using digital comparators that define their four coordinates (top, left, bottom, right). When the flag that enables the color assignment of the window and its coordinates are true then the RGB output is affected so as to fill the window with the predefined colour. This is an easy and cheap way to produce nice color output screens without using four times more RAM to store the color and rewriting 25.000 lines of existing software.

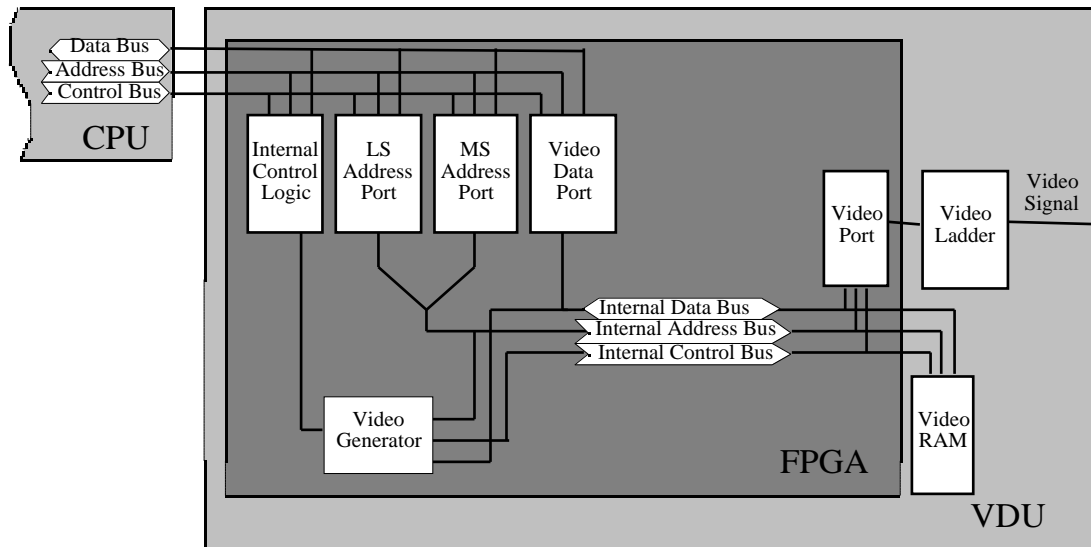
6.1 Product improvement

The developed VDU card is not directed comparable with the earlier version as its VGA compatible while the one used in production of SAT furnaces were Hercules compatible. Additionally, the benefits of this AE are not the improvement of a product but the restart of its production that has been stopped since 1995.

- The cost of the developed VDU is 22.5 ECU's while the cost of the earlier MSI version was 41 ECU's. One of the most demanding issues of this project relates with the maintenance of the furnaces sold until 1996. KEL will replace more than 400 VDU cards and monitors in the furnaces with Hercules monitors in the next 3 years (due to monitor failures). The net profit is set to 60 ECU's per card, giving an amount of 24 KECUs. It is clear that even this side activity related to the AE, almost pays it back. An other 8 KECUs of net profit is expected from the VGA monitor sales.
- The average time to trim the earlier version was 0.5 hours while the new VDU has practically no need for testing (more than 30 cards/hour). The difference in cost is 10 ECU's per unit.
- Due to low production numbers, the throughput and yield improvement is not of practical interest.
- The performance of the product has been improved in almost every dimension.
 - The new VDU has a superior functionality
 - ***The speed of the FPGA is beyond the barrier of the MSI circuits' speed, which was too low for a 27 MHz VGA card. This was the main technological issue.***
 - The new VDU has no more the flickering problems of the earlier VDU version
 - Reliability has been dramatically improved as the earlier versions have had instability problems in the dusty and high humidity environment of dental laboratories.
 - The Mean Time Between Repair is expected to increase from 3.5 Years to lifetime of the furnace. As KEL guarantees the electronic parts of the furnace for 10 years, the reduction of service costs will be approximately 5.5 KECUs per year (relates with 420 furnaces equipped with CRT monitor).
 - The size, as it was expected, was reduced to $\frac{1}{3}$ of the initial size. The new VDU is comfortably housed in the new compact design of the SAT porcelain furnace. The size issue was one of the most demanding, as the compact size is key factor in the sales of dental equipment.
 - The power consumption of the FPGA design is 1/15 of the next practically available solution of a 74S TTL series MSI design. The power consumption of this design is much more than the source ability of the CPU card's power supply. A redesign of this card would be necessary.
 - The FPGA based VDU is expected to improve the compliance of the furnace with EMC standards due to shorter high frequency paths on the PCB.
- The SAT models have much friendlier interface compared to the BRAIN models, which are equipped with a 40-character LCD display. For that reason, dental technicians get used easier to the CRT version of the porcelain furnace and prefer it in a rate of 3.1/1 (1992-1994 statistics).
- The FPGA based VDU design time was significantly shorter comparing it with the one needed for an ASIC design. Additionally, the FPGA based VDU card is **on board reconfigurable** so that it can meet the future needs of the product as adding more lines to the CRT image, supporting other types of monitors such as S-VGA, or even implementation of other CPU peripherals and so on.

The Internal Architecture of the FPGA

The Architecture of the VDU and FPGA is depicted in next figure:



The Block Diagram of the FPGA

The VDU card is driven by the CPU card and generates the video signal so as to drive the VGA monitor. The building blocks of the FPGA are the Internal Control Logic (ICL), the Address Port, the Video Data Port, and the Video Generator.

The Internal Control Unit

The Address Port handle the Video Ram Address that the CPU is going to Access. This address is polled at very high rate and the data stored in the Video Ram are passed to the output latch of the Video Data Port. The Internal Control Logic (ICL) is responsible for transferring the data between CPU and VDU and vice versa. It communicates with the CPU with 5 control signal.. Each time the CPU has to assign a pixel of the VDU, should read the byte that handles the pixel, change the pixel with the proper logic operation (AND OR XOR) and store back the new byte value. To obtain this operation, the CPU should set the Least and Most Significant Address Byte. The ICL gives access to the data stored in the Video Ram and pointed by the LS and MS Address port.

LS and MS Address Port

The Address Port handle the Video Ram Address that the CPU is going to Access. This address is polled at very high rate and the data stored in the Video Ram are passed to the output latch of the Video Data Port. The Address port Requires 8 I/O pins and 16 CLBs to be implemented in the FPGA.

The Video Data Port

The Video Data Port is a bi-directional data latch. The Output latch handles the Video Ram data stored at the address specified by the Address Port. The data latched at the input latch, are written to the Video Ram at the address specified by the Address Port when a rising edge of the CPU signal WR occurs. The Video Data Port requires 16 CLBs to be implemented in the FPGA and is shared the 8 I/O pins with those of the Address Port.

The Video Port

The Video Port is responsible to convert the 8 bit Byte to a serial stream of data. The Video Port requires 8 CLBs to be implemented in the FPGA.

The Video Generator

The Video Generator is the core of the VDU and it generates all the required signals so as to drive the ILC and the Video Port. Moreover generates the synchronisation pulses required by the VGA. It replaces the ROM and most of the SSI ICs of the old VDU card. The Video Generator requires about 30 I/O pins (25 pins to Access the Video RAM) and about 50 CLBs to be implemented in the FPGA.

The end product of this AE is the SAT-4 furnace equipped with a VGA or an S-VGA monitor, which is actually an improvement of the BRAIN-3 and BRAIN-4 models equipped with an LC-Display. The choice of not modifying the existing LCD is given more detailed in following section. The advantage of the new (SAT-4) product is much more than clear when we look back to the statistics of the years 1992 - 1995 where both models were in production. KEL expects to increase its sales in porcelain furnaces by 300% in compare with the sales of the years 1996-1998.

7 Choices and rationale for the selected technologies, tools and methodologies

The VGA interface module had had to fulfill the following specifications:

- Hardware compatibility with the current CPU board of the furnaces. This requirement is a basic one as the new VGA interface must replace all the HERCULES interfaces in more than 400 devices sold in the Greek market due to the limited life-time of the monitors (5-6 years) compared to the life-time of the furnaces (10-15 years)
- Software compatibility. The company's after sales service includes software (firmware) updating. New versions of the firmware are available every year to adapt the furnaces in the latest firing cycles' procedures. This free of charge service of KEL has proved to be major factor for the successive position of the company in the market. Thus the new design of the VDU should require no software redesign, to keep this downward compatibility.
Moreover the required modification of the software to handle the VGA VDU should be kept as low as possible, since the software redesign is a **high cost** process and, moreover, introduces new undesirable and difficult to find bugs. The furnace's software has been written in assembly language for the 8085 CPU and it is **25.000** lines long. The software generates outputs to the screen in a graphical way and has the ability to affect **every single pixel** on the screen. Even the characters are generated by software using special routines and not by using look Up Tables in the VDU. The present configuration of the pixel matrix is the standard HERCULES configuration (720 pixels horizontally, 348 pixels vertically) and the possibility to migrate successfully from the 720X348 resolution to that of the standard VGA resolution (640 X 400) is out of question, since any effort related to graphics software redesign is extremely expensive. Thus the hardware VDU driver who was developed is compatible with both the 720X348 HERCULES standard resolution and the VGA screen sweep capabilities.
- The VGA interface should be **flexible** enough so that it could be easily used either in a separate board (hardware compatible with previous CPU versions), or in a new design of a CPU board but with the same size as the conventional one. The latter is required by the new mechanical design of the furnace where space is critical.
- The cost of the components in the new design is not critical compared with the overall cost of the furnace. It is expected to move slightly upwards but the assembly cost will decrease.
- KEL is known in Greece for the quality of its products. Every new design should have almost **zero defects**, or else, the long and proven reputation in the market would be affected.
- The design should take into consideration the **component availability** for the production for more than 6 years.

Here we have to mention that the use of an LCD graphical display was rejected for several reasons:

- The viewing angle is small.
- The cost of the LCD display is too high comparable to this of the CRT monitor.

- The LCD is highly sensitive to the temperature, which is increased significantly when the door of the oven opens, resulting to malfunction of the LCD display.
- The customers statistically prefer the CRT monitor from an LCD one in a rate of 3.1/1 (1992-1994 statistics) due the low price of the CRT and due to its high brightness and contrast.

7.1 Technical solutions availability

Five technical solutions were considered for the design of the VGA interface.

7.1.1 The software redesign solution.

This solution includes both software and hardware redesign. The hardware redesign will be based on a standard VGA chip, a new VDU card and reconfiguration of the main CPU board. The software redesign will adapt the display information in the 640X400 format. This will result to incompatibility to software version with the earlier models. This solution has already been rejected because of the resulting incompatibility and its high cost for the hardware/software redesign.

7.1.2 The MSI multiple chip solution

This solution was implemented as a prototype and proceeded with a small pilot production. The result was a low component cost VDU unit but big in size with costly assembly procedure and, much more, costly quality control and trimming procedure since the operating frequency actually exceeds the maximum frequency of High speed CMOS circuits. The total cost was high and the solution does not comply with previous specifications. Additionally the current consumption of the MSI based VDU using high speed logic card was too high (380 mA) and the existing power supply unit was overloaded.

7.1.3 The EPLD solution.

The EPLD overcomes some of the speed problems in the MSI version but not all of them. On the other hand, the design turns out to be even bigger in size as most of hardware remains outside of the EPLD. This solution was rejected early on and no prototype was developed.

7.1.4 The standard VGA chip or card solution.

As it is mentioned in the section 7.1.1 the use of the standard VGA Chip requires extensive software modifications. As an alternative solution, the use of an interface between the standard VGA chip and the CPU board was carefully examined. It was proved that the implementation of this interface would not ensure the proper functionality since the VGA chip can not handle the resolution 720X348 pixels generated by the CPU board. Additionally the cost of the implementation would be too high.

7.1.5 The FPGA or ASIC solution.

The use of an FPGA or an ASIC seemed to be the most convincing solution to our problem since both could be designed so as to satisfy exactly all the specifications. The ASIC solution has a very low cost per unit but requires a big initial investment and is suitable for a much larger production volume than that foreseen for KEL. On the other hand, the FPGA solution is more expensive than the ASIC but with very small initial investment. Since KEL will need not more than 200 FPGAs per year, it seemed that the FPGA approach was the most suitable one to comply with the design specifications. The implementation of the VDU fits in a relatively small, low cost FPGA **with less than 128 Configurable Logic Blocks** (CLB) (less than 2500 gates). We also have to consider for the selection of the FPGA that the on board reconfiguration would provide flexibility and that the VDU could enhanced with more options (color option for instance).

An additional factor was the great interest of our company in FPGA implementations, as it is estimated that most of the future products of the company will be hardware based on this technology.

7.1.6 Design Methodology: Design with VHDL; Implementation on an FPGA.

Concerning the design procedure, the state-of-the-art design methodologies and standards were employed at each design stage. First of all, formal analysis was followed at the beginning of the design which would analyze in-depth the whole system and the FPGA in order to come up with a complete set of exact and correct specifications. This need for a formal and systematic analysis was a very crucial one, since, if it is by-passed or done in an at-hoc and incomplete manner, it usually results in incorrect or inexact specifications leading to costly redesigns. The result of this analysis procedure would also be the identification of the “hard” (to design) components of the FPGA, such as the video unit in our case. The leading FPGA companies, such as ALTERA and XILINX support the VHDL based methodology.

7.1.7 Selection of the FPGA Vendor

There was a careful selection of the FPGA vendor since the facilities and the price of the offered FPGA and the tools that support them should be selected so as to conform to the company's future requirements. The criteria for selection of the FPGA vendor are summarized:

- The range and the price of the offered FPGAs.
- The tools and their cost that support the design of the FPGA.
- The size and representation of the vendor.

It was very important for KEL to collaborate with a carefully selected FPGA vendor, since a change by the vendor in components like the CPU or the FPGA would force the company to new costly redesigns. Actually, during the design period the selected vendor did some major changes in prices that led our company to a reselection of the FPGA device that would be used. This had as a result the redesign of the PCB and some minor changes in the design of the FPGA.

7.1.8 Testing Methodologies of the experiment.

This experiment required both an FPGA design and the redesign of the existing PCB so as to handle the FPGA solution. There are two new PCBs that were developed.

The first one will replace the old VDU card. It has exactly the same dimensions with the Hercules card and the same placement of I/O connectors as it must fit to existing furnaces. The company will produce about 450 pieces of this version in the next 3 years. This is a necessity since the replacement of the current HERCULES monitor is not possible due to its unavailability. Since the mean life of a monitor is less than the half of a furnace, our company has to replace in the next 3-4 years most of the 400 aged HERCULES monitors with VGA monitors and the new VDU card.

The second PCB has been designed for the new model SAT-4 and is much smaller in dimensions.

A third PCB will be designed in the future so as to be an unique PCB solution for all the models of KEL furnaces. Thus, using always the same PCB and a different density FPGA, the company will be able to support both the LCD and the CRT monitor equipped models.

One more PCB was developed during the AE, which acted as the test-bed for the current FPGA design and will be used in the future for new designs.

The functionality of the FPGA was first tested in the test-bed PCB. These tests gave a very useful feedback as the original FPGA design turned out to have some functional problems. The FPGA device type used in the test-bed was not the one we finally have selected.

The final PCB (both versions) was designed for another FPGA type. There is still an option to shift in the future to an FPGA from a second vendor due to economical aspects.

8 Expertise and experience in microelectronics of the company and the staff allocated to the project

KEL was founded in 1988 from 4 electrical engineers with excellent experience (an average of 8 years each) in electronic design. A second company, ELCOM pbt, owned by the same persons was founded 5 years earlier with activities in the industrial automation, upgrading of

aged industrial equipment, and construction of scientific instruments to be used by Greek research centres and universities.

During the last 20 years, the engineers of the company are continuously working on the development and production of electronic devices. The main sectors of the company's know-how covers analogue design, digital design, microprocessors design software development, power electronics, optical electronics (pyrometers) and PCB design. Except from the electronic section, the company's engineers also cover electromechanical, mechanical design, sheet steel frame design, design of dies for casting and drawing, thermal isolation and heating elements design, and the area of ceramics.

At the early years, a plain paper and pencils were the design media. Since 1986, PC based work stations are the main tool in electronic and mechanical design. Before the AE, the tools used by the company's engineers were the following:

- ORCAD for general electronic design (schematics)
- SM ARTwork for PCBs
- Spice for analogue design
- AUTOCAD 12 for mechanical design
- SHELL (by INTEL) for EPLD design
- Z80, 8085 and 8051 assemblers for software compilation.

All the above tools are used from the early 90's and they haven't been upgraded the last 5 years. The average age of the company's engineers (now 41) was the main reason for this.

During the development of the inductive casting machine (1994 -1996), KEL asked for consultant from the local university. This co-operation brought in touch the company's engineers with the "younger" and more updated area of the school of electrical engineer and initiated this AE. Apart from the economical benefits for the company from this co-operation, the benefit of the tools' upgrading will give a boost to development department for the next 3-5 years.

After the Application Experiment the following tools were added to the company's workstations:

- MAXPLUS II for FPGA and EPLD software for design and configuration (programming)
- PROTEL for PCB design
- EAGLE for PCB design

The personnel of KEL that were involved in this project along with their main functions in the project 's work were:

Mr. Ioannis Kiriazopoulos, who had the overall management of the project,

Mr. Stergios Roudis, an electrical engineer and specialist in electronic design and PCB design. He was the main link of the company with the engineers from the University of Patras and was involved in specifications, FPGA design and PCB design.

Mss. Sotiria Tsekoura, an electrical engineer and specialist in production engineering and quality control. She, along with Mr Roudis, was involved in the FPGA design and market research.

9 Workplan and rationale

In the following paragraphs the workplan that was followed during the project's execution is given. More specifically the whole project was originally organised into 6 tasks the description of which and the work performed in each of them along with all associated issues mentioned above are detailed below:

9.1 Task 1. Specifications

An in depth analysis of the design was performed. The crucial points were identified and isolated and the design strategy to be followed was established. The output of this task was a complete set of exact and correct specifications for the FPGA. Moreover, the market research for the selection of the most appropriate FPGA was started in this task. Finally, the training of KEL's engineers on FPGA technology began. During this task SC prepared a detailed presentation of the FPGA technology, a training on the design of FPGA using VHDL and deliver notes in Greek on the ALTERA MAXPLUS II. Additionally the SC had significant

contribution in the selection of the FPGA vendor and in the estimation of the size and the cost of the FPGA. The company provided to the subcontractor the functional problems that the older system faced, all the technical details of the former product, as well as the specifications of the new system.

Duration: 2 month (m1-m2)
 Effort: 2.5 PMs (FU:2.0 SC:0.5)
 Deliverables: D1.1 Report on System Specifications
 D1.2 Report on FPGA requirements
 Milestone: Set-up of exact, complete and correct product and FPGA specifications
 Work in this has been performed exactly as originally. The duration and effort followed the original schedule (given above) and no deviations of any kind were experienced.

9.2 Task 2. FPGA High Level Design

Based on the specifications of the Task 1, the appropriate tools for the configuration and the programming of the FPGA were purchased and the architecture of each FPGA component has been specified. The design was mostly developed using the ALTERA's AHDL high-level hardware description language. A high level validation cycle were followed, by performing a number of simulations to detect and correct possible design errors and ensure conformance to the original specifications. Finally, more training activity was carried out. During this task the SC provided to the company valuable assistance on methodology of design and use of the FPGA technology. The company had the chance to have its first contact with the Altera's development tool. The whole design flow was followed and all the procedure was understandable by the company's personnel. No particular problems were faced at any stage and all the design flow was smoothly performed. Additionally SC designed the prototype PCB used for the development of the project.

Duration: 6 months (m2-m7)
 Effort: 6 PMs (FU:4.0 SC:2.0)
 Deliverables: D2.1 Report on VHDL documentation and simulation results
 D2.2 Report on FPGA design
 Milestone: Validated design and optimised layout

The selection of the FPGA vendor was proved successful, since the achievements of the project were satisfactory. The training activities on the specific development tool (ALTERA's MAXPLUS II) were finalized during this task.

9.3 Task 3. On board FPGA Testing and Implementation

The output of Task 2 was a well-configured FPGA that was synthesized and optimized during this task. By that time the market research had been completed and the synthesized model had been targeted to a big FPGA that used for the development. In this way the layout of the FPGA had been assigned and the first trial PCB was ready by the end of this task. No software modifications required for the interface between the VDU and the CPU. During this task SC pointed the parts of the design that may require modification in order to fit in a smaller low cost FPGA.

Duration: 3 months (m7-m9)
 Effort: 3.5 PMs (FU:2.5 SC:1.0)
 Deliverables: D3.1 FPGA Impementation and PCB prototypes
 Milestone: First time working with FPGA.

For the implementation of the VDU, at first was selected a big FPGA that can handle easily the design. It was found that the VDU functioned properly, however, optimizing the AHDL code could reduce the required CLBs for this design.

9.4 Task 4. System Integration and Testing

This task was initially be focused on the testing of the correct functionality of the prototypes delivered by Task 3 by using the appropriate test procedures. Behavior tests on various extreme conditions were performed. A testing procedure of the whole board was followed to check the functionality of the FPGA in all the modes of operation under real operation conditions and to verify that the specifications of the electronic subsystem are met. Additionally most of the AHDL code was optimized, with the significant contribution of the SC, and the FPGA design was reduced so as to fit in a smaller and cheaper FPGA and a new PCB was designed the company for this FPGA.

Duration: 2 months (m9-m10)
 Effort: 2 PMs (FU:2.0 SC:0.0)
 Deliverables: D4.1 Report on board design
 D3.2 Report on system integration and testing results
 Milestone: Working system

As a result of this task was the new VDU card based on the 7128 FPGA. The new VDU has the on both re-configurability option, thus can be configured so as to drive either the HERCULES or the VGA or even other kind of monitors. Thus the achievements of this project can be considered more than satisfactory.

9.5 Task 5. Marketing/ Exploitation/ Dissemination

The dissemination and exploitation of the results of this application experiment was the goal of this task. This was a continuous process, covering almost all project duration and was included: internal dissemination of the design experiences to the company's engineering team to enhance its technology know-how, and external dissemination and exploitation activities like preparation of the information material (brochures and leaflets) and contacts with the advertisement companies and other possible consumers.

Duration: m11
 Effort: 1 PM (FU:1.0 SC:0.0)
 Deliverables: D5.1: Report on dissemination/exploitation activities
 Milestone: Wide awareness of the product to the target market.

The main dissemination activities are:

- The preparation of the brochure of the SAT-4 porcelain furnace with the VGA monitor. This brochure was mailed to 1900 dental laboratories announcing the production of the SAT-4 furnace at the beginning of December 1998.
- The presentation of the SAT-4 at a dental exhibition on 19th of September 1998.
- The presentation of the SAT-4 by authorized dealers in 8 major towns. The dealers visited 93 laboratories (from April till the end of September 1998) and the furnace was presented.
- The announcement of the project results at two Greek newspapers on 13th of October 1998

9.6 Task 6. Management

The purpose of this task was to ensure the smooth and successful execution of the project by coordinating the project's tasks and the associated work of the involved partners, by monitoring the correct and on-time achievement of goals and milestones and the preparation of deliverables and reports and by controlling the consumption of resources as well. The need for an efficient management scheme was more than necessary in this project since the collaboration of the subcontractor and the proposer was required in order to achieve the project's targets in a restricted timeline (11 months).

Duration: It covers the whole project duration
 Effort: 1 PM (FU:1.0 SC:0.0)
 Deliverables: 4-monthly control and montghly management reports to the TTN
 Milestones: Project on time and in budget

Work in this task has been performed exactly as originally. The duration and effort followed the original schedule (given above) and no deviations of any kind were experienced.

Duration per task in months

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11
Task 1											
Task 2											
Task 3											
Task 4											
Task 5											
Task 6											

Actual effort and labor costs per task

	KEL effort (person-months)	KEL labor cost (KECU)	SC effort (person-months)	SC cost (KECU)
Task 1	2	6.8	0.5	1.9
Task 2	4	13.6	2	7.4
Task 3	2.5	8.5	1	3.7
Task 4	2	6.8	-	
Task 5	1	3.4	-	
Task 6	1	3.4	-	
Total	12.5	42.5	3.5	13

Planned effort and labour costs per task

Task	KEL effort	KEL costs (KECUs)	SC effort	SC costs (KECUs)
1	2,0 pms	6	0,5 pm	2
2	4,0 pms	12	1,5 pms	6
3	2,5 pms	8	1,5 pm	6
4	2,0 pms	6	-	
5	1,0 pm	3	-	
6	1,0 pm	4	-	
Total	12,5 pms	39	3,5 pms	14

Risk analysis

The risk was low due to the high expertise and of the Subcontractor on the FPGA technology. From the beginning of the project FU and SC scheduled the design steps, which were followed successfully, resulting to the new product and to highly acquired experience and knowledge of the FU on the FPGA technology.

10 Subcontractor information

10.1 Subcontractor

Name: University of Patras

Size:

The personnel of the Applied Electronics Lab. of Patras University consists of 5 Faculty members (most of them have PhD degrees from U.S. universities), 20 graduate students, 5 permanent research engineers, two secretaries and two technicians.

Business

Research and Academic Institution

Relevant Expertise & Experience

The Applied Electronics Lab. has long proven research capability in the area of Electronics and Microelectronics and more specifically in microprocessor/microcontrollers and in FPGA and VLSI design with emphasis in low-level issues, such as optimised IC layout of analogue and mixed (analogue/digital) structures.

Services provided

Consulting/design/training in FPGA design with emphasis in low-level issues/ use of CAD tools and methodologies

Personnel involved

A Full Professor and a highly qualified graduate student were involved in the project.

10.2 Rationale for choosing / evaluation of the subcontractors

The reason for choosing the aforementioned subcontractor to assist in the development of the FILECUP product, is owed to the fact that the contribution of it was considered absolutely necessary in terms of its expertise and know-how in the specific areas of interest for the successful and smooth execution of the project. Within this context its role in the experiment was distinct and clear and in accordance with its specific field of expertise. More specifically:

Applied Electronics Lab's special field of expertise lies in the design of digital structures, and especially in the high level VLSI design (capture of initial requirements and formal system analysis, architecture exploration, VHDL modelling and simulation, high level system validation etc.) of digital embedded systems, and thus its contribution was necessary for the successful design of the FPGA, especially for the "hard" design of the crucial synchronisation of the VDU signals.

Beyond the aforementioned technical reasons for selecting the specific subcontractor an important role for this choice played also the following reasons:

- Ability to deal efficiently with small projects of this type, proven by the subcontractors' previous successful works in the areas of interest.
- Geographical proximity the subcontractor to KEL, a fact which facilitated the co-operation and permitted efficient and prompt interaction in case that a problem might come-up
- Application of quality procedures to its work
- Good links of the subcontractor with other European organisations, the role of some of which were important for the success of the experiment, (the Europractice, the local TTN etc.) as well as with several silicon foundries.
- Existence of no contractual problems, having defined clearly the IPR issues between the participating organisations. More specifically, it was agreed that the overall system and FPGA design data would be exclusive property of KEL while the subcontractor maintained the right to use the know-how and tools employed during the execution of the specific experiment to other works too.

10.3 Contractual Issues

FU and SC signed a contract on 15/3/1998 (however the collaboration between FU and SC had been initiated before the beginning of this AE). In this contract were arranged several issues such as the payment issues, the penalty clauses etc. The collaboration between the two parts

was excellent as it can be seen from the results of this AE. According to the FU/SC contractual agreement, the FU was highly educated on the FPGA technology and design methodology by the SC. SC deliver to the FU the following:

- Training on the FPGA technology and design methodology.
- Information on the FPGA technology of several vendors.
- Detailed information on the ALTERA FPGA technology and programming software.
- Notes written in Greek language for using the MAXPLUS II software.
- The development board of the VDU based on 8282 FPGA.
- Significant information and help on manual routing, fitting and minimizing an FPGA based design.

The company is very pleased from this collaboration that resulted to a successful AE and the adoption of the FPGA technology. The interfacing with the subcontractor was performed with regular meetings of the involved personnel and exchange of data via e-mail.

11 Barriers perceived by the company in the first use of the AE technology

The proposing company, KEL being a first time user of FPGA technology faced certain “barriers” before being convinced to adapt this new to his business technology.

11.1 Psychological and knowledge barriers

First there were some psychological factors/barriers that the company had to overcome such as the reluctance (it could be also characterised as “fear of technology”) to accept the new technology, stemming from the inherent anxiety/frustration of a SME which faces a new and unknown to it technology.

Another factor which could be categorised both as psychological and knowledge barrier was the “over self-confidence” in some extent of the proposer company to its own technological capabilities. More specifically, due to the fact that the company’s personnel consisted of highly-qualified engineers with excellent expertise in PCB designs based on discrete elements, it was believed that it would be too difficult to be involved with a new, non-conventional and unknown technology such as FPGA technology.

The barriers formed by all these factors are further increased when the target markets of the proposer are conservative, something which is especially true in the specific case of KEL. Consequently, it is evident that the company would face a great risk if proceeded in redesigning some of its products with the new technology, since in case of something going wrong, it would actually lose this market (and most of its sales). From this point of view, it could be mentioned that the current FUSE experiment came at the right moment to lower this kind of barrier. Indeed, this experiment could be considered as a pilot one, since upon success of it, KEL would actually gain trust in the new technology and it would most probably use it in its other products too.

11.2 Know-how and technology barriers

In addition to the aforementioned barriers, there were also barriers directly related to know-how and technology issues. More specifically, an evident barrier for the company was formed from the fact that although its engineers were highly qualified in electronic designs using discreet components and processors, there was a significant technological gap they should cover associated with FPGA design methodologies, a gap which beyond the technical level existed at the management level also, since the (management) procedures of developing and testing an FPGA and the overall philosophy, are at a certain extent considerably different from the conventional ones with which the company was familiarised. This need created in turn a number of other financial and technology barriers as described below.

11.3 Financial Barrier

The evident way for the proposer to eliminate the lack of Microelectronics technology barrier (mentioned above) was to transfer the necessary know-how into his company, by appropriately training his personnel and thus acquire in-house FPGA design expertise. The investment required however for introducing the FPGA technology in a company, considering the training cost and the relatively high cost of the necessary EDA tools that should be purchased. Beyond its associated risks proved to be unaffordable for SMEs with the size of KEL and this certainly formed another important barrier.

To these it should be added that training is not very easy always to be found and if it is (found) it is usually not provided in an organised way.

11.4 Technology Barrier-Difficulty in subcontracting

Another option for the company was to avoid this costly and risky investment and apply the FPGA technology to its product, by just subcontracting a suitable design house, which would undertake the whole design. However, in this case, although the company would indeed have in its hands an upgraded FPGA based product, it would never have control of the technology applied, and the company would have always to rely on third parties for every other product design or even for minor upgrades.

Concluding, it could be mentioned that it is evident that all these barriers and dilemmas had formed a deadlock for the company, an efficient solution to which has been undoubtedly given by the FUSE framework and co-operation with the local TTN for the execution of the current experiment.

11.5 Market support of the new technology

Greece is a small country and consequently a small market. KEL has experienced problems with support and purchase of relatively new technology products. KEL's strategy for adopting new technology is to ensure that the new technology will be popular, the company (ies) will support it for a long time (5 years) and the Greek representative is reliable. These three factors cannot easily be fulfilled especially in Greece.

12 Steps taken to overcome the barriers and arrive at an improved product

As presented in the previous section, the company indeed faced a number of several important barriers before deciding and committing itself to move towards an improved product applying the FPGA technology.

However, the fact that the product market it addressed seemed very promising, in combination with the understanding that with the existing product the company had no opportunity to keep the good share out that owned, forced KEL to look for alternative ways of improving its performance and if possible to lower its cost, something that it soon realized it could be achieved by only using a state of the art technology based on the FPGAs.

The first and most important step to overcome the psychological barriers was evidently to try and gain as much relevant information as possible about the new technology. This was accomplished by approaching the subcontractor who gave the company some first introductory information about these technologies, their impact and benefits and also notified them of the existence of the FUSE Framework as a possible solution to the company's problem. This had as result to get in contact with the local TTN from which more specific and additional information, especially about the FUSE Action, was drawn. These preliminary discussions (with the subcontractor and the TTN) eased somehow the company's hesitation and fear concerning the introduction of new technology to its business (i.e. psychological and knowledge barriers) and was convinced to apply for a FUSE experiment.

The prospect of having the chance of submitting and perhaps running a FUSE type project gave KEL a way for possibly overcoming the financial barrier that it faced, since such a project would eliminate the financial risk of the company by providing the necessary funding to move to the desired integration of the FPGA technology into its product.

Through regular contacts with the TTN and meetings with the subcontractor prior the submission of the FUSE proposal, a first examination of the possible benefits and implications that the introduction of the new technology would have to the company's product was conducted and a preliminary draft study took place resolving several issues, which were then used for the FUSE proposal formation. The most important of these (issues) were:

- Whether it was meaningful to apply the FPGA technology in the company's product
- Available options in terms of type of (Microelectronics) technologies to be applied (ASICs, FPGAs, Standard VDU chipsets, discreet components etc.) and suitability of them with respect to the specific application.
- Cost and benefits of these options.
- Economic impact of adoption of the new technology to the product and the associated market (payback time and ROI estimation etc.)
- Proper organisation of work to accomplish the right and smooth execution of the FUSE experiment.

All these had as result that most of the previously mentioned barriers (mainly the psychological and knowledge ones) were lowered significantly, if not completely eliminated.

The complete elimination of all barriers and especially of the know-how and technology ones were accomplished in a gradual way during the various stages of FILECUP project execution. Indeed, through the observation, awareness, provision of the appropriate training (crash courses, on-job training etc.), tools familiarisation, and the active participation in all stages of the experiment, the company managed to eliminate the existed technology and know-how gap, in the sense that it acquired the necessary expertise and capability in knowing which actions it should conduct in case of repeating a similar experiment in the future. This means that in such a case in the future the company would perform everything by its own.

Concluding, it could be mentioned that indeed the proposer perceived a number of barriers, ranging from psychological reasons to ones related directly with the proposer's market, the nature of the specific technologies, the lack of know-how etc. Most of these barriers have now been considerably lowered, if not completely eliminated, thanks to the chance that the FUSE framework offered, and the successful project's execution, due to the good name the high quality expertise and the services provided by the subcontractor and the proved capability of the local TTN in the efficient co-ordination of this action. Finally, the three most important issues that help the FU to overcome the barriers were:

- The SC contribution in convincing the FU to apply a new technology, providing introductory information and demonstrating the FPGA technology, that the use of the FPGA would be a successful and low cost solution to its problem.
- The prospect of running an EC's funded project like FUSE would reduce the financial risk of the company of applying a new technology for the first time.
- But more than anything, the falling sales was essential for the FU to proceed as soon as possible to a solution to this problem.

13 Knowledge and experience acquired

An important goal of the current application experiment was not only to apply the FPGA technology to the company's product but also to transfer to it sufficient knowledge and know-how in the areas related to the technology applied (with the help of the subcontractor and the local TTN) thus giving the company the chance to increment its capabilities in a variety of ways.

First, at the technical level, throughout the execution of the project, the subcontractors' experienced personnel provided training to the engineers of KEL in all stages of the FPGA design, ranging from formal requirements analysis and FPGA specifications set-up, to architecture exploration and VHDL/AHDL development simulation and testing. This training effort had the form of guidance, consultancy, awareness discussions, and a number of in-house small seminars and crash courses in the aforementioned issues i.e. an one-day crash course

organised by APEL regarding VHDL/AHDL-based design and FPGA prototyping. They also got familiarised with the ALTERA's MAXPLUS II EDA tool associated with the corresponding design stages (e.g. compiler, simulator, synthesis tools, etc.).

Finally, on-the-job training was provided, in the sense that engineers of KEL undertook the development of **all the parts of the design** under the close supervision of the subcontractor.

Consequently, KEL having been given the opportunity (through the aforementioned training activities) to fully observe, get awareness, participate and contribute significantly in the whole design process during the experiment's execution, it is guaranteed that the company's engineering team has acquired the capability of repeating a similar experiment in the design of its future products, **with no support at all by design service providers and using the company's design software and configuration devices.**

Beyond the technical level, significant know-how and expertise has been gained at the management level also, in the sense that the proposer has become aware (by appropriate consultancy and guidance from the subcontractor) in the impact of applying the FPGA technology in a product as well as of its possible pros and cons, so as to be able to decide when it is meaningful and beneficial to employ such technology.

Moreover, the proposer's manager through the project execution and under the monitoring and guidance of the local TTN and the help of the subcontractor got also extensive and valuable know-how in the various technical management procedures (monitoring, progress and control management reports) that are required for the smooth and correct execution of an FPGA- based project.

Finally, the company had the chance through the various phases of the project (and under the appropriate consultancy and guidance of the subcontractor and the local TTN) to acquire the necessary expertise regarding the interfacing and communication/management procedures that should be followed for the design and testing of an FPGA.

14 Lessons learned

The fact that the software of the KEL's products is written in assembly language is a significant barrier for the fast upgrade of its products. Actually, KEL would not face the VDU problem if the software was written in a higher level language. Therefore, the company is proceeding with rewriting the software in 'C' language.

The successful completion of the FILECUP project, beyond the implementation of the improved FPGA based product had also as result that the company had the chance to benefit in terms of lessons learnt through the execution of this project.

More specifically, the most obvious lesson drawn, which was owed to the enhanced characteristics of the FILECUP VDU stemming from the application of the new technology onto it, was that the company should always follow the evolution of technology and should never let itself stuck to a specific, usually obsolete, technology driven either by a "fear of technology" syndrome or by a "steadiness and safety feeling" stemming from the usage of a well-known conventional technology (in its designs in the past).

Based on this fundamental lesson the company has also learnt that when the need for the application of a new (untouched by the company) technology is required, the only actual and real problem that should be overcome is the lack of information associated with this technology and the identification of the necessary resources for accessing this information.

More specifically, it has learnt that in order to be able to cope with a new technology (like designing with FPGA in our case) and benefit out of its application to a specific product, the required info should be of the following nature:

- First of all to have this information available that will provide the company with the capability to know when it is meaningful to turn to a customised solution (an FPGA implementation in our case) and which technology /methodology /tool to apply.

- To ensure that the necessary know-how associated to the new technology exists or can be acquired (e.g. by the employment of appropriate training in combination with the suitable subcontractor scheme), if such a customised solution is proved (through the aforementioned procedure) that it is required.

In the specific case it was the FPGA-based solution that it was considered necessary and all the required know-how associated with this technology was acquired and employed for the implementation of the specific product by using an appropriate subcontractor scheme and the relevant training. In general, the company feels to have learnt that it will never have to hesitate in the future in case that a new technology has to be applied in one of its products.

Another important lesson for the company, which stemmed out of its successful and close co-operation with its subcontractor (Applied Electronics Lab. Of University of Patras) throughout the experiment's execution, was the realisation that the employment of an appropriate subcontractor scheme is many times the right solution and the way to accomplish targets which would not have been feasible by just lying on the company's know-how and expertise, (something that till now was the case for the company), and that it should put aside its inherent hesitation and difficulty in subcontracting which has been characterising the company so far.

However, in order that this (subcontracting) scheme should be proved successful and efficient, the subcontractor should be well qualified and carefully selected according to certain solid criteria. Moreover, in such a scheme it should be necessary that the company (KEL in our case) has sufficient knowledge and understanding of the technology to be applied, so as to be able to have the overall control of the project and the capability to check the quality and validity of the subcontractors' work.

Involving to a new technology there are some significant problems to be faced (hopefully at the initialisation face) such as the purchase of new products in the market. KEL faced initially an availability problem of the FPGA, which was difficult to overcome. The reason was that the KEL's components provider has never purchased FPGAs.

Another problem that has to be faced in the future is the unavailability of this type of the FPGA. KEL has to be ready to adopt this design on the new FPGA that ALTERA will provide and promote in the future. Then KEL may have to purchase new developed system so as to support the new technology.

The fact that KEL due to the non very- good understanding (at the beginning of the experiment) of the capabilities that the FPGA-based technology offered, had as result to underestimate its potential and conduct the set-up of the FILECUP specifications. When through the experiment's progress the company realised that it could indeed include into the FPGA additional features (e.g. a colour version for the VDU), there was not enough time to materialize the new specs. Anyway, these features can be still added in the future as the FPGA based VDU card includes a serial EEPROM and is easily reconfigurable. This "software reconfigurable" hardware, is actually very good news for the company, not only for the future potential of the new product (the VDU card) but also for the next project of the company, which is the redesign of a digital driver for a 2.5 kW RF module used in the casting machine IFESTOS-2, the second in sales product of the company. This driver will be optimized to increase the performance of the power module, including in the digital part trimming information for the delays of the power MOSFETs, increasing output power and decreasing the possibility of fatal conditions.

The whole project run in a smooth way with an exception in the last 3 months. During this period, the management decided to start two months earlier the production of the porcelain furnace demanding earlier the project deliverables. A second team, transparent for the FUSE AE, was organized so that at the end of the project there was arranged every detail considering the production of the new VDU module and the end product, the furnace.

Finally, based on this experience a couple of lessons have been drawn i.e.

- That indeed the careful selection of the most suitable subcontractor is of outmost importance for the success of such an experiment, since if the specific subcontractor were not so well qualified the project’s outcome would be doubtful and that
- The adoption of the new technology and tools, driven by the subcontractor’s engineers, turn out to be a much easier task than it seemed to be at the begging of the project. KEL has decided to employ at least one young engineer who will close the gap between the new technologies and the aged engineering traditions of the company.

Total 24% was subcontracted.

Specifically:

University of Patras subcontracted in training, Specs, FPGA design and PCB design and test.

The subcontractor percentage participation per task is:

Training: 80%

Specs: 20%

FPGA design: 33%

PCB design and test: 28%

15 Resulting product, its industrialisation and internal replication

The outcome of this experiment, as already mentioned in several other sections of this document, has been the development of a Video Display Unit that can generate video signals suitable for the VGA monitors. Additionally the new VDU has the re-programmability option so it is able to support other type of monitors, including the HERCULES monitor. For the proper operation of the VDU card there is no need to modify the software of the CPU despite the type of monitor that drive and this is concerned as a great achievement.

KEL has actually performed most of the steps required to promote the new product in the market well before the FUSE AE was finished. This was a necessary risk, as the market was already expecting the new series furnaces of the company. Those steps included a mechanical redesign based on a more compact hardware, three prototypes of the new furnace, promotion material and presentation of the prototypes in an exhibition in Athens, Greece.

The company has also planned all the details for the production of the new VDU and the end product, the porcelain furnace SAT-4. Actually, the pilot production has already started, the company dealers promote the product in the Greek market and the first 5 units have already been sold (end of November 1998)

Part of the final business plan prepared for the FILECUP product

The average cost of the FILECUP VDU in terms of labour, components cost etc. is analytically given in the following Table:

Description	Amount/device (in ECUs)
FPGA	10
Various Electronic components	5
Labour	5
PCB	2.5
Total cost	22.5

The net profit is set to 60 ECU per VDU card and this leads to an overall unit price of about 82.5 ECU. This is going to be the end user price, as the company has direct contact to all of it’s customers in Greece.

No significant differences have to be reported regarding this cost estimation and the one performed during the proposal formation (the total cost estimated at that time ranged around 18 ECU) This is just a reasonable difference since a time period of about 2 years has elapsed between these two estimations.

The final products

- SAT-4 model porcelain furnace including the new VDU card
- VDU card and VGA monitor for more than 400 furnaces equipped with HERCULES monitors.

The keys for product promotion

- SAT-4 has the most friendly and popular interface among the users of porcelain furnaces. The large screen interface is preferred in a rate of 4:1 comparing with the LCD interface.
- The HERCULES VDU cards will be replaced in the next 3 years because the users will simply run out of monitors.

Cash flow from development to stabilized production

First Phase: Development

- The FUSE program has already funded the Development of the VDU
- KEL has already funded the design of the new series furnaces.

Second Phase: Pilot production

- KEL has already funded with 12 KECUs and started the pilot production of 50 SAT-4 and BRAIN-4 porcelain furnaces. A total of 84 KECUs is planned to be invested for the pilot production until April 1999.

Third Phase: Normal Production

- The investment in pilot production will pay back 160 KECUs, enough for self-funding for the following production cycles.

Time schedule

Final Development: September 1998

Start of Production: October 1998

Expected availability to market: End of November 1999

Product Description

Description

1. VDU card suitable for VGA monitors, compatible with HERCULES format software drivers. The card is already used in the Series 4 pilot production of porcelain furnaces (SAT-4) and is suitable as a replacement part for SAT-II and SAT-3 earlier models.
2. Porcelain furnace equipped with VGA interface and monitor.

New, existing modified?

The VDU card for VGA monitors is a new part for the existing product of Dental porcelain furnaces.

Further research

The new VDU will not be developed further, at least till 2nd quarter of 1999. After that a colour version might be developed as at the end of the year the company intends to present new products or variation of its products in the 11th Dental Exhibition of Athens.

Internal Replication

The company has acquired extensive experience and knowledge on the FPGA technology and design methods. The VDU cards are already in production since October 1998 while the new furnace model SAT-4 will be in full production on November 1999. Here we have to mention that a pilot production of 50 SAT-4 furnaces has been already integrated and these furnaces have been distributed in selected customers for extensive tests. Therefore this AE can be considered successful since the new product is already in production. Additionally we have to mention that the company, using the knowledge and the experience on the FPGA technology acquired from this AE, is designing an FPGA based power driver module for its Inductive Casting Machine (Hephaestus). It is anticipated the new FPGA based power driver module will have enhanced reliability functionalities and robustness compared with the existing one.

Patents

KEL does not intend to patent the new product.

16 Economic impact and improvement in competitive position

First, the market situation and the existing product sales before the FUSE experiment's execution (as well as the projected ones in case of not developing the improved product) will be described.

As already mentioned in previous sections, prior the set-up of the current experiment and the development of the FILECUP FPGA-based improved product, the company's sales are divided in two periods. In the first period, 1992-1994, the SAT-II and SAT-3 furnaces, equipped with HERCULES monitors, amount more than 70% of an average of 80 units sold per year. In the second period, 1995-1998, sales declined to almost 1/3 of the previous period as at the end the only available models were equipped with LCD (BRAIN-3).

Year	1992	1993	1994	1995	1996	1997
Number of sales	76	87	79	47	32	22

The prediction for the 1998 sales is for 18-24 units. No significant change in sales was predicted for the next three years before the FUSE AE. Actually, a market decline is expected in a few years time (see in the growth potential of the market below)

Short Business Plan of the developed FILECUP product

Size of the Market.

In Greece: 160 units (porcelain furnaces)/year

In addition, the local market will absorb another 400 units of VDU cards the next three years

In the neighbour (European) countries: 3,500-5,200 units/year

Worldwide: 25,000-40,000 units/year

Growth potential

The market in Greece is not expected to grow the next years. Actually a 10-25% decline is expected after 4-7 years. Although the average life time of porcelain furnaces is expected to cut down from 11 years to 5 years, the number of porcelain furnaces will decrease to 1/3 as the average dental technicians per lab will increase from 2.3 to more than 6 with a proportional reduction of the laboratories and the number of porcelain furnaces per technician. The worldwide growth is not relevant with the economics of this AE and will not be taken into consideration. For the FILECUP products, the sales are expected to be as follows:

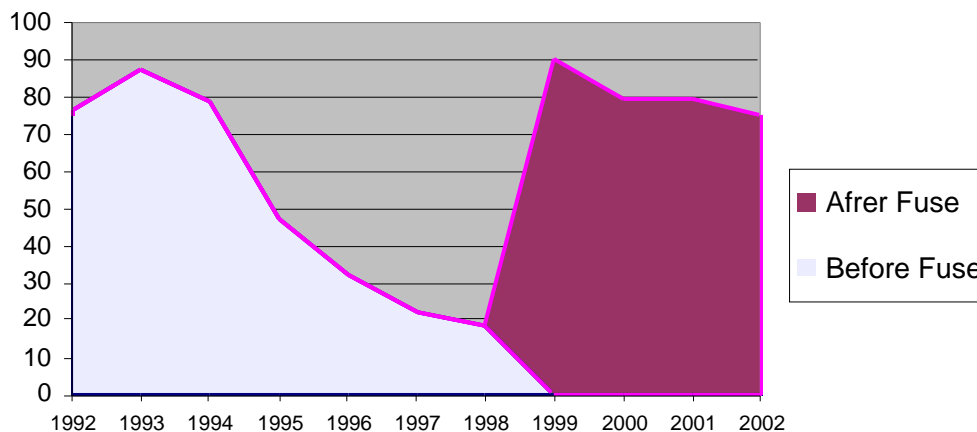
Market	1999	2000	2001	2002	2003
Porcelain furnaces in Greek Market	90	80	80	75	65

VDU cards as replacement parts	50	250	50	30	20
Exports of Porcelain furnaces	-	50	50	?	?
VGA monitors	50	250	50	30	30

The above figures are based to the company’s sales during the years 1992-1995 as the possibility for total market recapture is very strong. Actually, the new product of the company, the casting machine, will grow the number of the company’s customers by 100-150 the next 2 years having as a result the growth of porcelain furnace sales as well. It has been found from the company’s statistics that a customer equipped with one of KEL’s products will invest to a second with a possibility of 85% more than a non KEL’s customer.

The sales of the furnace before and after the fuse experiment is depicted in the next chart:

The sales of the Furnace

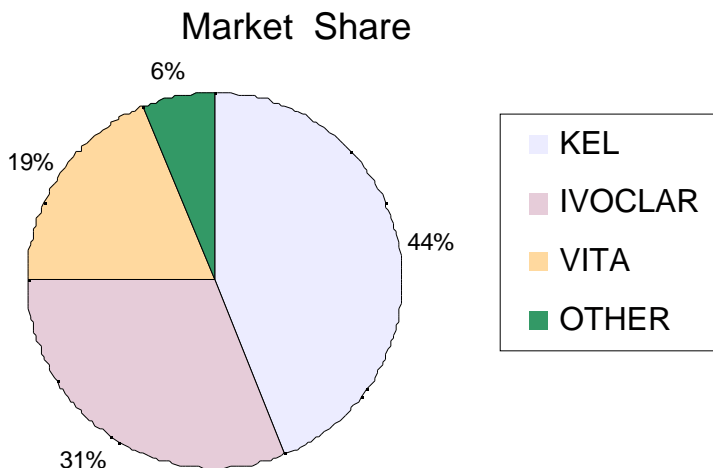


Characteristics of the market

The market requirements are, in order of importance, excellent functionality, good after sales service, friendly interface, reliability, small size and low cost. KEL’s products already satisfied the first characteristic and now with the technological improvement (PCB to FPGA) and the development of a new VDU the next five features will be implemented too in the highest extent. Market share recapture has to be supposed as certain for the next three years.

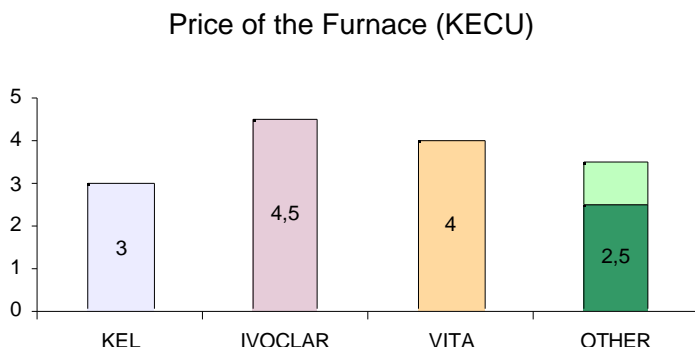
Main Competitors

The main competitors are two Greek manufacturers and two importers who represent IVOCLAR (Liechtenstein) and VITA (Germany). IVOCLAR and VITA are companies that manufacture porcelain furnaces, moreover are two of the most popular suppliers of consumables such as porcelain, dental alloys etc. Therefore they have a respectable market share. The average Greek market share of the product is estimated to settled in the next years as in the following pie:



KEL has a very rich experience from the Greek market the last 10 years. KEL’s products are considered as the most reliable and at the best price in the local market. Further more, during the ‘90s, KEL was the most technologically advanced company in Greece (in the Dental area) and had had the best services.

The two main competitors do not provide the fast and high quality of the after sales services that KEL does. Additionally the price of their product is higher that KEL's. A comparison of the price of the product with this one of the main competitors is given in the following chart:



What will make the difference?

KEL covers almost all the market demands. The porcelain furnaces of the company are the most reliable and functional devices in the Local market. The new VDU will affect the demand for friendly interface and also will prevent the damage of the company’s image in the services area as now there will be an alternative replacement part for the old HERCULES interfaces and monitors. Market share recapture through the technological improvement (PCB to FPGA) is sure.

Marketing Strategy

Who are we going to address?

KEL will target mainly the Greek market. The main categories of the company’s customers are:

- Laboratories that are already customers of the company with Porcelain furnace older than 6 years.
- New customers among the 1200 laboratories that are not KEL’s customers
- Customers with HERCULES type monitors.

KEL's systems address high quality products and thus can be successfully exportable. However the size of the company and its production capabilities just cover the domestic market and currently cannot cover other countries.

Will there be advertising?

KEL will continue normal advertising, mainly mailing all the Greek laboratories twice a year with brochures and participating in all the Dental exhibitions in Greece.

Pricing Policy.

KEL has had always used the pricing policy as an effective tool in the market. The company's low production costs along with the well-organised and low cost distribution net enable the company to offer their porcelain furnaces at almost half of the price of its competitors.

Distribution and Financing

Distribution

KEL has its central distribution and technical support office in Athens. Additionally, the production unit located in Patras supports both the distribution and the technical support in South Greece. Moreover, there are four more peripheral distribution and technical support offices that support the Greece and the Cyprus, at Thesalloniki (North Greece), Ioannina (West Greece), Heraclio (Crete) and Lemesos (Cyprus). All the above mentioned offices are well organised for the technical support and exhibition of the KEL's products.

Results: Selling Cost, Profit

The predicted sales are expected to have the following net profits (in KECUs):

Market	1999	2000	2001	2002	2003
Porcelain furnaces in Greek Market	140	123	123	115	100
VDU cards as replacement parts	3	15	3	2	1
Exports of Porcelain furnaces	-	38	38	?	?
VGA monitors	0.3	1.5	0.3	0.2	0.2
Total	143	190	176	117+	101+

The difference in the net profit due to the FILECUP products will be (In KECUs):

Market	1999	2000	2001	2002	2003
Porcelain furnaces in Greek Market	115	100	100	85	75
VDU cards as replacement parts	3	15	3	2	1
Exports of Porcelain furnaces	-	38	38	?	?
VGA monitors	0.3	1.5	0.3	0.2	0.2
Total	118	155	141	85+	75+

The net profit due the FILECUP project for the next three years is 414 KECUs and thus the FUSE Return of Investment ratio is 672%. The increased sales of the SAT-4 and the recapture of the market anticipated for the 1999 will enable the company to recover the cost of this AE (61.6 KECUs) in 7 months from the end of the AE. Of course the participation of the FILECUP project to the whole project 'new porcelain furnace SAT-4' is estimated to be about 15-20%, since a lot of effort was given for the mechanical design of the new product.

17 Target audience for dissemination throughout Europe

The company has been introduced to the FPGA design methodology. The new FPGA based VDU is hardware and software compatible to the old Hercules driver of our dental furnaces. It has replaced a lot of discrete components used by the earlier version of the VDU card. The size of the new product is actually 25% reduced, while it does not suffer from flickering problems that had been occurred at the previous one. It is believed that the experiences and lessons learnt through this experiment will be of interest and benefit for a wide target audience throughout Europe owed to:

- a) The specific technological subject addressed within this experiment which regards a large number of companies with similar type of technological problems.
- b) To the technological capabilities of KEL which are common to a large number of companies also
- c) To the fact that there is a considerable number of other SME companies exhibiting similar profile characteristics (in terms of size, volume production, economic capabilities etc.)

More specifically:

- a) The product requirements are always increased and is required by the companies to invest on new technologies that correspond to these requirements. The FILECUP project proves that applying the new technology (FPGA), a company can easily give a solution to problems that can't be solved using conventional technology.
- b) Additionally, the FILECUP project proves that it is not too difficult or costly to a SME company to be adapted to new technology. Actually it was proved that a company like KEL with conventional capabilities on microelectronics can improve them easily by the proper selection of an assistance or a subcontractor that already knows this technology.
- c) Finally, companies that have low volume production, like KEL's, is meaningful to use the FPGA technology due to its high capabilities and to its reasonable cost.

In terms of PRODCOM codes this AE results will be interested for other small companies specializing in the areas of medical and surgical equipment (PRODCOM 3310) and in the development of precision instruments (PRODCOM 33).