

ESPRIT Project 21963: FUSE

Application Experiment no. : 2179

Advanced multifunctional FIR filter device

Small digital ASIC replaces huge analogue board

“DEMONSTRATOR DOCUMENT”

(The Application Experiment Report)

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Name of Organisation: Esaote S.p.A.

Role: Associated Contractor

Associated TTN CESVIT S.p.A

Project: **Advanced multifunctional FIR filter device**
 Small digital ASIC replaces huge analogue board
Duration: **12 months**
Cost: **88 KECU**
Project Manager: **Ing. Marcello Mazzarella**

Abstract

Esaote is an enterprise with 579 employees and a turnover of 124 MECU that, since 1950, develops, produces and markets non-invasive medical diagnostic systems. In ultrasound imaging, Esaote is the 9th manufacturer at world level (and 1st European) with 4.8% world market share in 1995. The Company is experienced in electronic project on both analogue and digital techniques using PCB and SMT; programmable devices are used in the company's products as well.

In 1996, Esaote planned to develop its first all-digital ultrasound system within following three years. One critical point of this project was availability of an high speed multifunctional digital filter, for the acquisition front-end, having same level of performance of existing one in analogue technology. Although the present filter could be considered well working, it required many components, space on board and power consumption. As well, it suffered of drift of the components in the long time period and the trimming activity was time consuming.

A new filter was conceived to be realised using digital technique; in particular, this very innovative filter was realised adopting the 0,7 μ CMOS digital ASIC technology. It allowed to reach many results as a high integration level, high performance level (clock cycle @ 30 nsec, reconfigurability, decimation, one clock cycle multiplication, and more) and cost saving on components of 30% with respect to the old analogue solution. The project duration took 12 months, starting on 1/7/96 and finishing on 30/6/97; the cost of the project has been 88 KECU.

The new diagnostic ultrasound equipment is expected to produce an economical competitive advantage for the Company of 10% yearly increase in turnover for the next 3 years, instead of stationary or slow decreasing turnover as it would have been without the technological innovation. The payback period for invested money is foreseen in 12 months; the return of investment – ROI - evaluated for the ASIC prototype development only has the value of 614% in a period of 5 years (product lifetime).

Esaote got from this AE a specific ASIC design inner capability to be used in future applications to overcome actual restrictions of discrete logic, free from any economical and technological constraint due to an ASIC design committed outside. As first internal replication in the use of the new technology, an ASIC is now under development to replace, with higher economical benefits and efficiency improvements, the actual discrete logic devoted to manage function of ordering digital data acquired in an ultrasound system (the so-called FI-FO function). Future further application of ASIC technology will be the innovation of the ultrasound pulser section (with at least 3 ASICs to be integrated in a very complex and sophisticated MCM structure) or the upgrade of the receiving pre-amplification section (to be integrated directly with piezoelectric transducer and requiring an ASIC technology different from one employed with this AE).

The possible general interest for the developed filter from side of other customers leaded prototype manufacturer to get licence for sharing these results.

Keywords

Technical

ASIC
Digital filtering
FIR filter
ASIC Design process

Application

Communication
Radar
Medical
Image processing

Best Practice

Successful workplan
In-house ASIC design centre set up
Right Subcontractor's role

Signature

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1. Company name and address.

Company: **ESAOTE S.p.A.**



Head office	Registered Office	Operational Site	Operational Site
Via Siffredi 58	Via Ruffino Aliora 32	Via Siffredi 58	Via di Caciolle 15
16158 GENOVA	15033 Casale Monferrato (AL)	16158 GENOVA	50127 FIRENZE
ITALY	ITALY	ITALY	ITALY
	CCIAA Alessandria 0173229	Tel +39 10 65471	Tel +39 55 42291
	P.IVA 01622780060	Fax +39 10 6547275	Fax +39 55 434011

Project Manager: Ing. Marcello Mazzarella

2. Company size.

Size: Large Enterprise

Employees: 579 at 31/12/199

Turnover : 124 MECU

Number and functions of personnel involved in electronics:

Area	Function	Total number	Involved in electronics
Research & Development	Researcher	69	42
	Technical staff	62	28
	Others	10	-
Manufacturing	Technical staff	48	28

3. Company business description.

Esaote is the major Italian company which develops, produces and markets non-invasive medical diagnostic systems.

The three main product lines are:

• Diagnostic ultrasound imaging systems

This Esaote's product line is the company core business and includes equipment and probes covering all ultrasound medical imaging applications like cardiovascular, internal medicine, obstetrics, gynaecology dermatology, etc. These equipment provided B-mode, continuous and pulsed Doppler and Colour Flow Mapping representations with biometrics calculation on detected signals. Through these equipment it is also possible to perform special ultrasound imaging application for stress-echocardiography, biopsy, laparoscopy, etc.

Since 1992 Esaote is the major European producer of diagnostic ultrasounds: between its two plants in Firenze and Genova more than 2000 equipment and 5000 probes of different ultrasound system

models (AU4 Idea, AU3, Challenge), based on proprietary technology, have been manufactured and sold in 1996 for a market value of approximately 80 million ECU (75% of which from export).

- Magnetic resonance imaging (MRI) systems

Esaote is acknowledged world-wide as the market leader in "*dedicated*" (i.e. developed for specific clinical applications) MRI systems, distinguished from conventional "*whole-body*" MRI systems.

The product "ARTOSCAN" was developed by Esaote for imaging joints and limbs. Unique, proprietary Esaote technology makes ARTOSCAN much smaller than traditional whole-body MRI systems and, therefore, markedly easier to install and significantly less costly to operate.

- Cardiology and neurology non-imaging diagnostic instrumentation.

Esaote efforts in non-imaging cardiology diagnostics are currently focused on developing cost-effective products that contribute to the efficient management of the clinical (resting and stress electrocardiography - ECG) and administrative (patient data management) functions of hospital cardiology departments.

In non-imaging neurology diagnostics, Esaote has completed the conversion of its entire electroencephalography (EEG) product line to fully digital technology. The SIRIUS product family is now available in modules that can be expanded from a single digital EEG console to an integrated, multi-purpose system that includes multiple EEG stations, evoked potential and quantitative analysis.

Through its Italian sales division, Esaote also supplies turn-key hospital instrumentation systems and distributes biomedical instrumentation manufactured by other major international companies.

Esaote also provides the complete range of services required by international customers, including technical and after-sale assistance, and physician and technologist education, including basic training, follow-up courses in addition to courses and seminars on advanced topics and new applications.

4. Company markets and competitive position at the start of the AE.

COMPANY MARKETS

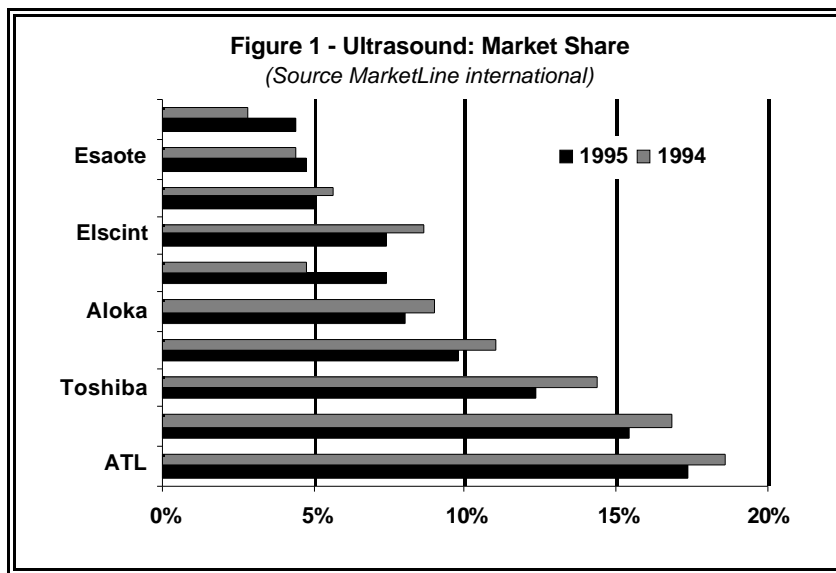
Medical diagnostic ultrasound imaging is the core business of Esaote with 60% of company total revenue coming from this specific segment of world healthcare market, both for public and private customers. Esaote is also involved (11% of total revenue) in the mature segments of cardiology and neurology non-imaging diagnostic instrumentation (mainly from its position of domestic leader) and in the new small but fast growing segment of magnetic resonance imaging systems for dedicated applications (10% of total revenue). The remain 19% of total revenue comes from service and turn-key supplies.

The ultrasound market sector, the market segment of specific interest for this application experiment, has been born in the second half of '60s as biomedical application of technologies developed in other industrial areas (military, computer, electronics and other). Its technological origin produced the effect of a market dominated still today by American and Japanese companies, frequently represented by the divisions of big multinational companies (Siemens, Hitachi, GE, Toshiba, HP). Among the independent operators the most successful are the American ATL and Acuson.

For many years, this market segment had no barriers to new operators entry. Recently the increased technological level of products and their more and more advanced specialisation make more complex production and sales of medical ultrasound systems. On the other side, the constraints in public health expenditure introduced a strong competition on price in this sector and it got, as first effect, a concentration of operators through acquisitions and mergers. This is because a sufficient critical mass, as from productive as from commercialisation point of view, is more and more an important competitive factor within the sector fragmentation of operators.

Today, only 10 companies (source Market Line international) control 93% of the market. Esaote is the 9th company in this sector at world level with 4.8% market share in 1995, a growing share respect to 1994 (see Figure 1).

Many small operators control the remaining 7% of the market. Such manufacturers, Medison (ROK), Kretz (A), Kontron (F), Pie Data (NL), B&K (DK), AI (US) and others, could be subject to a merging by major operators.



In the next table (Figure 2) some significant data are reported about value, composition and medium range forecast of diagnostic ultrasound market.

Figure 2 - DIAGNOSTIC ULTRASOUND MARKET COMPOSITION
(Sources: Frost & Sullivan, Databank, Marketline international)

By value	1995		Growth rate	2000	
	Value	%		Value	%
European Union	560 MECU	33%	3.0%	650 MECU	32%
USA	700 MECU	41%	2.5%	790 MECU	40%
Others	440 MECU	26%	5.0%	560 MECU	28%
World Market	1700 MECU	100%	3,5%	2000 MECU	100%

By demand of product level	1995		2000	
	Top	Medium	Top	Medium
European Union	10%	90%	30%	70%
USA	25%	75%	25%	75%
Others	5%	95%	20%	80%

A particular aspect of this market is that, being the major competitors from United States and Japan, the important European area is covered for more than 75% by imported product.

The trend of top level products shows that they will be based soon on all-digital technology instead of all-analogue as offered in 1995. The importance of all digital products could be estimated to arise to a 30% of market value in year 2000. Today (1997) the first all-digital diagnostic ultrasound systems are coming on the market (by ATL, GE, Toshiba) and their success is a demonstration of the trend.

Then, for the European industry in general and for Esaote in particular, it is mandatory to extend its target by offering top-level systems in a way to enter in the high segment of the market with the technology today requested and to consolidate and strengthen its present positions in the low and medium segments of the market. Failure to compete and to innovate in such competitive market will lead to a market loss and decreasing turnover.

During years 1994-95 the Company hadn't available ultrasound equipments for the mid-high segment of the market. Mid-low-end echographs were sold in 1000 units during the year 1994. and just in 1995 it launched the AU4 IDEA medium-end product, which was sold in 420 units during the same year. Sales of AU4 IDEA rose to 500 units in 1996.

COMPETITIVE POSITION

Within Italy, Esaote is the largest provider of electro-medical systems and instrumentation, with sales exceeding 60 MECU in 1995. Esaote is the domestic market leader for cardiology and neurology non-imaging diagnostic instrumentation (with more than 30% of market share).

In the diagnostic ultrasound market (i.e. the reference market for this application experiment) Esaote controls a 35% share of Italian market.. The company sells an unusually broad product line, which reflects its own product diversity and its long-standing, complementary relationship with Hitachi Medical Corporation (Hitachi products are sold in Italy only and take account of only 20% of revenue from Italian market).

In the international market Esaote has achieved a strong position in specific ultrasound segments and holds significant market share in the cardiovascular, radiology and internal medicine echography sectors. In the United States, for example, Esaote is one of the main competitors in the private practice market for cardiac ultrasound equipment with a market share exceeding 16%. Similarly, the Esaote's European market share (about 9% including Italy in 1995) is demonstrating consistent growth, particularly in Germany and France (Figure 3).

Figure 3 - Diagnostic Ultrasound: Esaote market share in 1995			
	Esaote turnover (consolidated)	Value of Market	Market share
Italy	34.0 MECU	96.8 MECU	35%
Europe (Including Italy)	50.7 MECU	560 MECU	9%
United States	13.3 MECU	700 MECU	2%
Others	17.0 MECU	440 MECU	4%
World	81.0 MECU	1700 MECU	4.8%

Typical Esaote's sales volumes go from the order of 1000 units per year for the mid-low end product class to the 300-400 units per year for the mid-high end product class.

Main competitive strength for the existing AU4 IDEA product, which was going to be improved thanks to ASIC technology, was in the exceptional image resolution. It was technically got thanks to the joint adoption of annular array – composite transducers for probes and of an advanced beam focusing technique for the front-end of the equipment, that of multi-channels dynamic phasing and variable aperture for continuous dynamic focusing and variable transmit focusing. The higher is the number of channels for image acquisition the higher resolution is. Multi-frequency techniques and proprietary dynamic filters were employed as well in the existing product.

With AU4 IDEA, from 96 up to 128 channels were available; 256 channels will be available in the new generation digital product.

Actual trend of diagnostic ultrasound imaging systems is toward the all-digital technology respect to the present all-analogue. This is the reason for which Esaote needs to renew its ultrasound diagnostic systems.

5. Product to be improved and its industrial sector.

The product to be improved is a biomedical instrument for ultrasound diagnosis.

This platform acquires clinical data through probes with different scanning methods (Annular Phased, Linear and Convex Array) to feature high-resolution imaging, Colour Doppler and Spectral Doppler.

Ultrasound technology meets the clinical needs like those required in a variety of different situations i.e. low velocity colour sensitivity for venous flow detection or crisp continuous wave Doppler spectra, mandatory for cardiac jet quantification.

The main technical characteristics and specifications for existing product are:

Technology:	Analogue
Scanning methods:	Annular Phased, Linear and Convex Array
Monitor:	12" RGB
Imaging Modes:	2D and M-Mode
Imaging Frequencies:	from 2.5 to 10 MHz
CFM Modes:	velocity, velocity-variance, and intensity
Doppler Modes:	Pulsed, HPRF and continuous wave
Doppler Frequencies:	from 2 to 6.6 MHz
Formats:	Single, Dual and Quad screen
Zoom:	variable magnification
Cine Memory:	up to 48 Mbytes
Physiological channel:	ECG
Biometry:	multi-application report generators
Dimensions:	about 46 (w) x 130 (h) x 50 (d) cm
Safety:	EN60601-1 (IEC601-1), EN60601-1-2 (EMC compatibility), IEC1157 (Ultrasound safety)

In Figure 4 the schematic functional block of a diagnostic ultrasound system is reported.

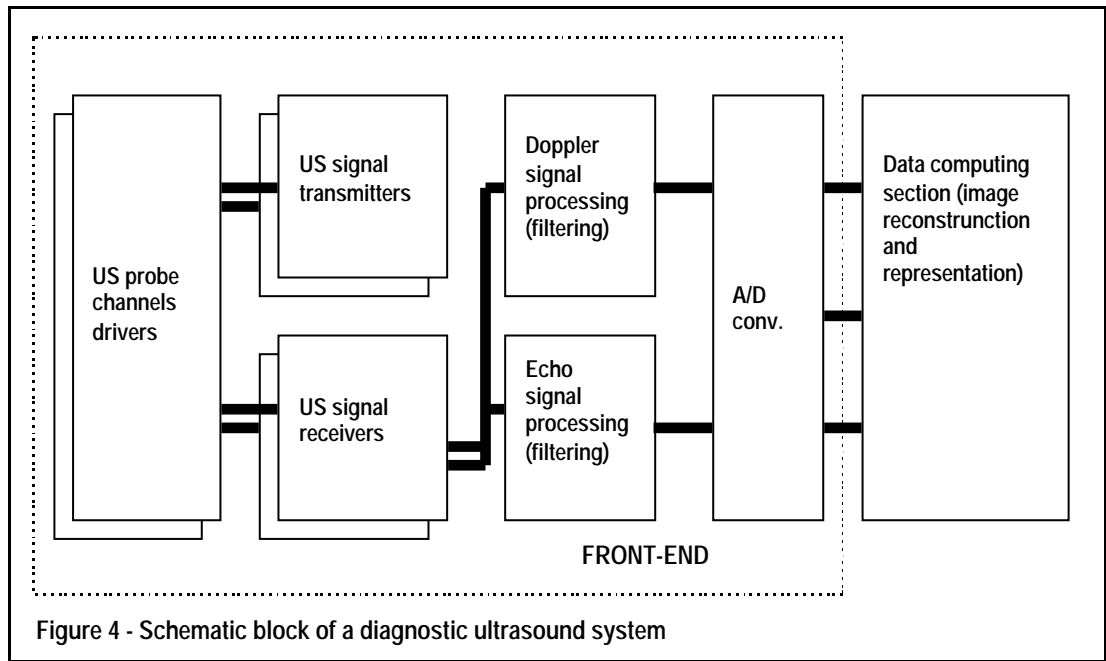


Figure 4 - Schematic block of a diagnostic ultrasound system

The terms "*all analogue*" or "*all digital*", used to indicate the echograph technology, are related specifically to the technological structure of the front-end block where the ultrasound signal is received, filtered and converted in digital forms for next processing of image reconstruction and representation. The data computing section is composed by a dedicated computing platform in digital technology, because of the high quantity and speed of information to be processed (in the future these platforms will be replaced with commercial ones).

In the "all-analogue" systems the ultrasound signal is processed in analogue form within the front-end section and consigned to the A/D converter. The major critical element of this architecture is the signal filtering process to extract the diagnostic basic information, in both Doppler and Echo signal processing front-end sub-assemblies, before to be converted in digital form. Examining the functionality of one of the two sub-assemblies, the signals acquired and pre-amplified in the US signal receiver channels blocks are undergone to a demodulation driven by sine and cosine generators. Then they are filtered through low-pass analogue filter in a way that only the diagnostic information is retained before to be converted in digital form (see Figure 5).

Until today the advantages of this analogue technological solution, when compared with the digital one, was concerning the level of filtering accuracy, which requires a real time processing.

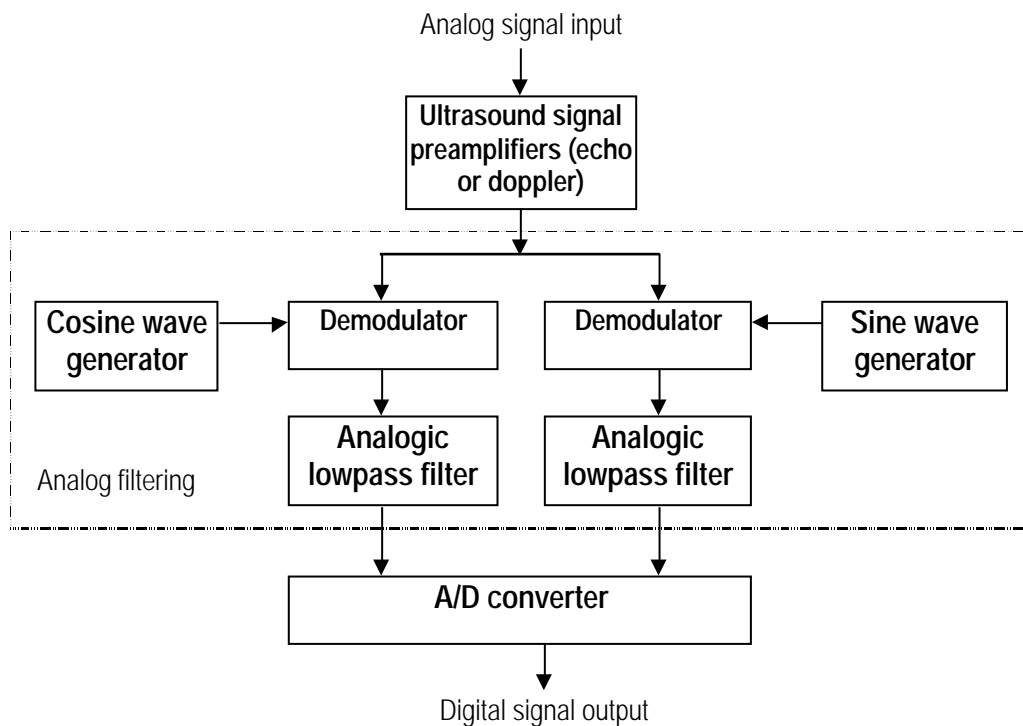


Figure 5 - Analog diagnostic ultrasound acquisition filtering process

Today this problem may be overcome thanks to the performances offered by new technologies and the “all-digital” solution obtained with this application experiment aimed to get many advantages, namely:

- reduced cost of material (no more need for reference waves generator, demodulators, analogue filter, ...)
- reduced manpower for calibration and testing activity (due to the critical nature of the tuning and check of this specific part of the equipment during the manufacturing process)
- absence of drift during the lifetime of the product (typical of analogue components) with no service activities for re-tuning the filters.
- Reduced PCB surface and power consumption

In addition, an all-digital ultrasound echotomograph realisation was mandatory for Esaote to be still competitive for the next future in a market dominated for over 80% by American and Japanese companies, who are proposing all-digital ultrasound systems.

6. Description of the product improvements

In the classical all-analogue systems the ultrasound signal is processed in analogue form within the front-end sections up to the A/D converter. The all-digital systems request to move the A/D conversion as nearest as possible to the receiving source and, from there, to start the signal processing in the digital form.

The use of the all-digital technology allows to address the main features for such equipment, obtaining:

- increase in the focusing precision,
- increase in the contrast level (dynamics)
- capability to store and process data in more flexible way.

A specific critical point of the global project of the all-digital ultrasound equipment is the availability of high speed, advanced multifunctional digital filter. It is a fundamental requisite in order to realise an acquisition front-end of the ultrasound system with higher performance, reliability and cost saving in comparison with the analogue technology.

The objective of this AE has been that to innovate filtering process, performing replacement of presently analogue demodulation and filtering circuit of the data acquisition section with a digital version having the same level of processing time and accuracy. This can be regarded as a basic step toward the realisation of an all-digital echotomographic system with benefits as mentioned before.

The item to be realised was an electronic component whose function is that of an advanced multifunctional digital filter to be used in echotomographic medical systems and more specifically in the data acquisition section of such equipment. The same functionality was previously performed with analogue technology, with circuits composed by demodulator devices and related sine and cosine wave generators having the purpose to extract information and then converting it in digital form with an A/D converter section.

The most suitable technology for such filter is the ASIC one, as it will be more detailed and analysed in the next paragraph. Nevertheless, ASIC technology will play a fundamental role as basic technology to work out future digital products with improved functionality and better economical and performance solutions. It will be necessary, for Esaote, to have the necessary expertise to control this technology in house.

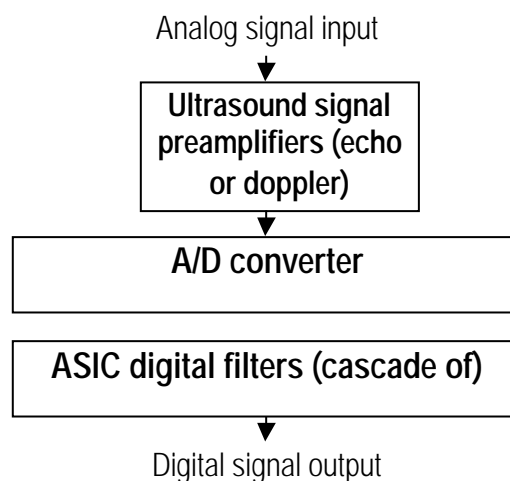
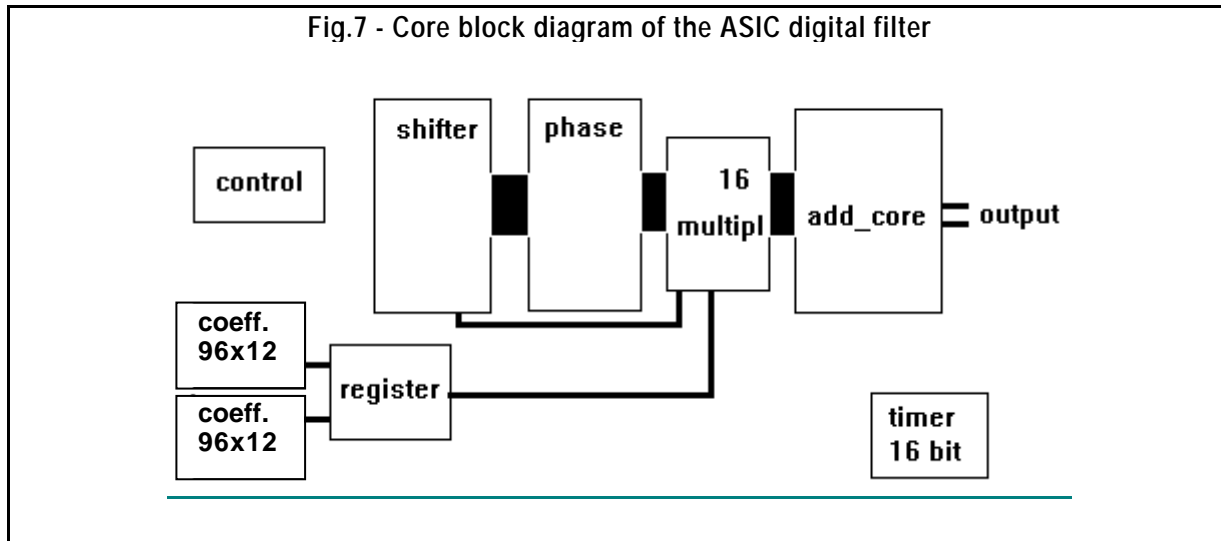


Figure 6 - Digital diagnostic ultrasound acquisition filtering process

The realised component (see Figure 6) is a decimator **FIR** (Finite Impulse Response) filter that extracts, from the digitised acquired signals, the necessary data to be passed next to the processing and presentation stages of the echographic scanner.

The resulting filter is then used in cascade chains to implement the filtering functions of the acquired ultrasound signal to extract the basic information before to be processed for reconstruction and representation of the diagnostical meaningful image.

Such component for digital filtering has been realised using ASIC technology (see Figure 7 for block diagram and next paragraph for rational for choice).



FIR filter: General requirements

From the functional point of view, functionalities specified for the new filter were:

1. To implement a decimator FIR filter containing 16 multiplier-accumulator which permit to realise a 16th order non symmetrical FIR filter or a 32nd order symmetrical FIR filter @ 33 MHz.
2. The incoming samples are 16-bits coded, the coefficients are 12-bits coded, the internal accuracy is 32 bit
3. The filter includes a 16-bits microprocessor interface that can be configured to be INTEL or MOTOROLA compatible
4. Decimation: The decimation by 2, 4, 8, 16 allows an output rate being 2, 4, 8, 16 times lower than the input rate. Using an internal configuration register, interfaced to a microprocessor, programs the value of the decimation. This function uses 16 banks of 12-bits coefficients. The 12-bits coefficients are loaded using a 16 bits microprocessor (12 LSBs for the coefficient, 4 MSBs to address the bank)
5. Cascadability: The decimator FIR can be cascaded in order to implement long high-rate FIR filters. Even in cascaded structure, the FIR filter has to keep symmetry advantages.

Particular needs for the project were:

- A digital device able to compute long particular Hilbert filters up to 64 coefficients with only one device in real time. This is possible using the condition symmetry zero-interleave.
- To tune the dynamics properly, via the block gain
- To have low consumption (less than 1 W) at highest frequency
- To be able to decimate data, also working at lowest frequency
- To change the coefficient at each clock cycle, having always output valid data
- Critical path: it is a problem to maintain the cycle under 30 ns using multipliers that have access time of 28ns, and the hold+setup time needed by the flip flop are -3ns. This makes the MSB, which is the last bit computed by the multiplier when the result arrives to the final status, to be computed apart with an extra logic. The lowest bits are computed in time lower than 26ns, so the result is guaranteed in less than 30ns. The layout design for this part needs a particular care.

The resulting new chip is an ASIC in the order of 40K gates, 208-pin QFP packaged, based on the 0.7 μ CMOS technology performing the functionality of a FIR filter having:

- 1) RAM with separate buses of I/O to store up to 16 sets of filter coefficient represented by 11bits+1 sign bit ;
- 2) multiplication realised in one clock cycle by 16 multipliers 12*16bits;
- 3) minimum clock cycle of 30 nsec;
- 4) decimation for the coefficient (2, 4, 8, 16)
- 5) reconfigurability passing from a 16 taps into a 32 taps with coefficient symmetry;
- 6) internal timer for timing requirements, presettable by master microprocessor.

FIR filter: benefits from ASIC

Thanks to the introduction of the ASIC technology, following benefits have notably been achieved for the new product:

- *Cost reduction:*

It has been due mostly to

1. Direct reduction of cost of the components involved in the signal filtering, reduced of 17,4% per piece, with a value of 260 ECU.
2. Reduction of cost for manufacturing setup and test process. Demodulator devices and the related sine and cosine wave generators disappeared from the circuit (see Figure 6). This way all critical and time-wasting needs to regulate the synchronism of the demodulator devices have been eliminated, the A/D converter starts to digit signal straight from the acquisition stage. In particular, the trimmer activity carried out at the end of the old production chain required about 4 personhour with a cost of 100 ECU per piece. This cost has been eliminated adopting the ASIC solution.
3. The on field maintenance operation is simplified too, as all the demodulators trimming procedures are avoided (This operation take only the 3% of the whole "on field" operations)

- *Performance improvement:*

1. The PCB area is reduced of 30%, and the power consumption is reduced, too.
2. Enhanced possibility to calculate with the same process more different kind of data for the Doppler and imaging signals. Current analogue technology requested separate demodulation circuits for that.

To summarise, the advantages of this digital solution based on ASIC technology respect to the analogue actual version are:

- less cost of digital component (30%) respect to the material involved with analogue version (duplication of circuitry having reference waves generator, demodulators, analogue filter,....., for each filtering chain involved);
- eliminate the critical need for synchronisation of circuitry during manufacturing and product lifetime, allowing to avoid the operative cost of the analogue version - some percent of the whole system cost - with a major reliability and this is a point granting a qualitative and quantitative factor of improvement of product competitiveness;
- allows to achieve the same level of precision and performance of the analogue solution;
- open the way to future enhancements derivable from an all-digital architecture of the signal processing in the diagnostic ultrasound equipment .

7. Choice and rationale for the selected technologies and methodologies.

Why the ASIC technology ?.

Until today the analogue technology has been the only one selected for this kind of applications, thanks to the precision, filtering accuracy, speed and reliability of the extracted information that it ensures with respect to a possible digital solution. In medical care context, accuracy of diagnostic information is crucial.

The availability of high speed, multifunctional digital filters is then mandatory to realise such sophisticated process in digital way with the same level of precision and quality you can get today with analogue technology. But, when this experiment started (and still today), manufacturers are selling components very similar each other which don't match the required performance (large number of taps, programmability, overall dynamic of 32 bits, reconfiguration capability).

Actual digital filter market can be split into 3 groups: communication filters, versatile FIR filters, video processing filters.

Within the first group, there are components with a very large number of taps but the precision of data representation is usually limited to 16 bits and does not match the required filter programmability, which is mandatory to cover the image processing stage. Among the second group, there are components that can operate at high frequency (up to 50 MHz) and, using decimation techniques, can work with a large number of taps, but this reduces the work frequency and many times the overall dynamic is restricted to 16 bits. Furthermore such components are very limited in data precision and can be used only in typical configuration. Current image and video processing components are very limited in data precision, since image applications are usually based on 8 bits input data (pixels and coefficient) with an overall dynamic range up to 16 bits.

A solution of the digital filtering for the diagnostic ultrasound acquisition won't be so satisfactory with the use of commercial components. An integration of commercial components with other discrete electronics to achieve the requested performance is quite complicate and could be more expensive than the analogue one and it is not granted that precision and performance will be adequate. For example, an eventual integration of a commercial component like DSP with other discrete electronics to try to achieve the requested performance (high number of acquisition line per images - up to 256 in the new echograph - real time processing, high accuracy of data processing) will be quite complex, with higher cost also of the analogue solution and not so performing.

Other solutions like the integration of a DSP with other electronic components, needed to reach the performance required, resulted to be not cost effective even if compared with an ASIC solution for a 3000 units/year production.

FPGAs were not the most suitable solution due to the specified complexity and operative frequency of the system, which would require too many devices that did not fit on the board. So the advantage of lower cost for FPGA on volumes would be lost because of the low integration level allowed.

A solution based on multiple devices was again not cost effective.

It has been then individuated the ASIC technology as the most suitable approach for realising a filter with wished requirement in a way that it could be grant economicity and reliability of the solution.

Previous considerations concerning the best technology to be applied in the application experiment can be summarised in the following table.

	Multifunctional digital filters MDF	Digital commercial components + discrete electronics	FPGA	Multiple devices	ASIC	Evaluatio
Precision	2 nd (16 bit)	5 th (8 bit)	4 th (10 bit)	3 rd (12 bit)	1 st (32 bit)	ASIC
Performance	2 nd (20Mhz)	3 rd (15Mhz)	4 th (10Mhz)	4 th (10Mhz)	1 st (33Mhz)	ASIC
Cost	4 th (90 Euro)	3 rd (85 Euro)	2 nd (80 Euro)	5 th (100 Euro)	1 st (70 Euro)	ASIC
Complexity (realisation)	1 st (buy ready)	3 rd (block assembly project)	2 nd (only SW)	4 th (HW block assembly project & SW)	5 th (SW project and silicon foundry necessary)	MDF
Complexity (utilisation)	1 st (single comp.)	5 th (multiple comp. & tuning)	1 st (single comp.)	4 th (multiple comp.)	1 st (single comp.)	MDF - FPGA - ASIC

The methodological approach to ASIC design.

The methodological approach selected by Esaote for this ASIC design execution was to proceed with its own personnel for the design, with support of an experienced subcontractor in the role of trainer for both the managerial and the technical aspects. The ideal choice for this revealed to be that the subcontractor trained "on the job" Esaote's personnel on ASIC design methodologies as well as on ASIC management.

Subcontractor helped the work team and monitored their results at each stage of activity, preventing any wrong project approach.

The manufacturing process (data preparations for foundry, silicon manufacturing and static test procedure) of the component was a service given by ATMEL-ES2 silicon foundry. A minimum number of components was realised just to be sufficient

- to cover the need for a first complete functionality test in the real operative condition of the new ultrasound equipment
- to put the work team in the condition to follow all the cycle of production and to verify the results through a predefined validation test, in a way to acquire a fundamental know-how on the complete ASIC design process and be able to repeat the process in the future.

The main rationale for the choice of this methodology to carry out this application experiment was that to acquire as much expertise as possible in developing an ASIC. This way ASIC design would become an internal know-how of ESAOTE, to be used in future products development. For this reason, role of external subcontractor has been more limited to on job training for ASIC design rather than to the design of ASIC itself.

The selected design tools, ASIC manufacturing technologies and test methods.

At the start of the AE Esaote chose to design the component using ViewLogic schematics because of their portability in every developing system today in use. This could allow Esaote work team to re-use such tool for new future ASIC design, without being bound to the tool for placement and routing.

Later on, the actually selected design tool was Cadence ES2 Design Kit and Viewlogic schematics were ported within the Cadence environment passing through the design kit facility. This choice was due to the

silicon foundry selected for prototype manufacturing (ATMEL-ES2); with this tool it was in fact granted that the resulting ASIC design transfer package would have been compatible with the silicon foundry requisites for fabrication.

For manufacturing it has been selected to fabricate the component in a 2 metal layer 0.7 μ CMOS process. The reason for choosing this technology is that it is consolidated and it will be supported for other 10 years by the silicon foundry. All other consolidated processes won't be supported so far and processes having longer expectancy of support are not so consolidated as technology.

About testing, the component has been tested by the manufacturing service provider with a static test according to fault grading testing sequences implemented during the component design. This was to ensure and adequate screening of manufactured component so as to obtain a higher reliability and to make effective testing of component. Then component was undergone to a speed functional test carried out by Esaote personnel. A specific validation plan has been defined, including tooling definition, creation of test bench and indication of test procedures, to ensure that prototype will meet and perform the functional specification expected for the component in the real environmental.

8. Expertise and experience of the company and staff allocated to the project

From its historical roots in the medical instrumentation field, dated back to the 1950's, Esaote has always developed and manufactured only products with own proprietary technology.

Esaote's R&D activity involves now more than 120 people (20% of total company staff) and it is split into 5 units located in the Genova and Firenze labs, each of them dedicated to the basic research and development of new products for the related sector or product division they report to.

The Technical Department support all R&D Units for every aspects related to engineering, product papers, components standard, CAD/CAE and test processing.

The main experience of Esaote's R&D structure for developing medical products is in the fields of:

- materials technology to study ceramics for US transducers and magnets for MR systems, with related technical problems for system integration and installation;
- high-integrated electronic components to project chains of acquisition, amplification, filtering, A/D conversion of physiological signals;
- hardware data processing dedicated platforms and high-definition representation systems for acquired signals;
- software package of acquired signals data processing
- informatics systems, based on commercial platforms, for networking and database of acquired signals and processed reports.

In particular, as manufacturer of electronic products, Esaote has microelectronics expertise in the area of hybrid amplifiers and filters of bio electrical signals, in the area of project and development of PCBs (based on the use of discrete logic at the most different level of complexity), FPGA (particularly for specific application in medical ultrasound scanner systems), Microsystems (design and manufacturing of piezoelectric transducer for echographic applications) and electronic design of RF coil systems for MRI equipment.

The Unit involved in this AE has been the R&D Ultrasound Unit of Genova that started its activity in 1982 and today has a staff of 30 people.

This Unit is particularly addressed to research and development of echographic systems for the mid-high range of the market. During its activities it has acquired relevant expertise in HW/SW beam focalisation, acoustic beam and transducer simulation methods, images processing techniques in the field of medical ultrasound application.

Right now the Unit is developing the AU6, the innovative product using the results of this AE based on the digital beam forming technology.

Two people involved directly in this AE are in staff to the R&D Ultrasound Unit of Genova. Both graduate in electronic engineering, they have a cultural background in digital electronics and relevant expertise in design of acquisition front-end for diagnostic ultrasound system.

Joint expertise of needs of diagnostic ultrasound systems design and some previous experience in digital electronics design have made them as the most suitable people to get the maximum advantage from an on-job training on ASIC technology to be next applied by themselves in other applications.

9. Workplan and rationale

Rationale for activities breakdown and resources allocation

At time of the definition of the workplan for this ASIC project, Esaote decided to play the role of “maker” of all ASICs developed for its internal purposes. This strategic decision can be motivated by the high technological level more and more required to their manufactured products, which could generate, in short times, needs for several different ASICs to be used on different Company’s products.

An inner work team owns the best knowledge and sensibility about needs of products to be developed or innovated. This is thanks to the day by day work integrated in the research structure and this know-how could not be easily reached by any other outer design team. Due to this condition, an inner ASIC design team will have the most proper expertise to define and work out the most suitable solutions and specifications in developing dedicated ASICs.

Besides, an ASIC expert inner team may grow in such a way that any further modification of the projects could be done internally, with minor resources and, consequently, development or modification costs may be further optimised. This perspective of further cost reduction could open the Company to an enlarged application of ASIC technology since it could be even more convenient (and better in performances) when compared with discrete commercial components.

This is why Esaote decided to invest to train and maintain an internal ASIC design team. In particular for the FIR filter design the availability of an internal capability granted the best fitting with the specific internal needs and avoided to disclose confidential data and procedures to the exterior.

Resources - Roles and responsibilities

Esaote, the proposer of the AE, managed all project operations and executed, on the basis of the received on-job training, the complete cycle of ASIC FIR filter development. Esaote was also the End User of device coming out from this AE as embedded chip in its marketed diagnostic ultrasound equipment.

CESVIT, as sub-contractor, supplied on-job training during all phases of the design activity and monitored Esaote results at each stage, with intervention for correction of wrong projectual approaches. CESVIT supplied a service for schematics translation and simulation and a service for the realisation of the placing and routing for the device design as well. The subcontractor is experienced in technology know-how transferring, in developments using high technology (key expertise is in digital ASICs) and in furnishing components.

ATMEL-ES2 is the silicon foundry providing the manufacturing process (data preparations for foundry, silicon manufacturing and static test procedure) of the component as contracted service.

Activities

Project activities were split into six workpackages:

- 1) technical management,
- 2) on job training,
- 3) specification,
- 4) design

- 5) prototype manufacturing
- 6) testing.

Figure 8 depicts the workplan, giving a representation of project flow and timing.

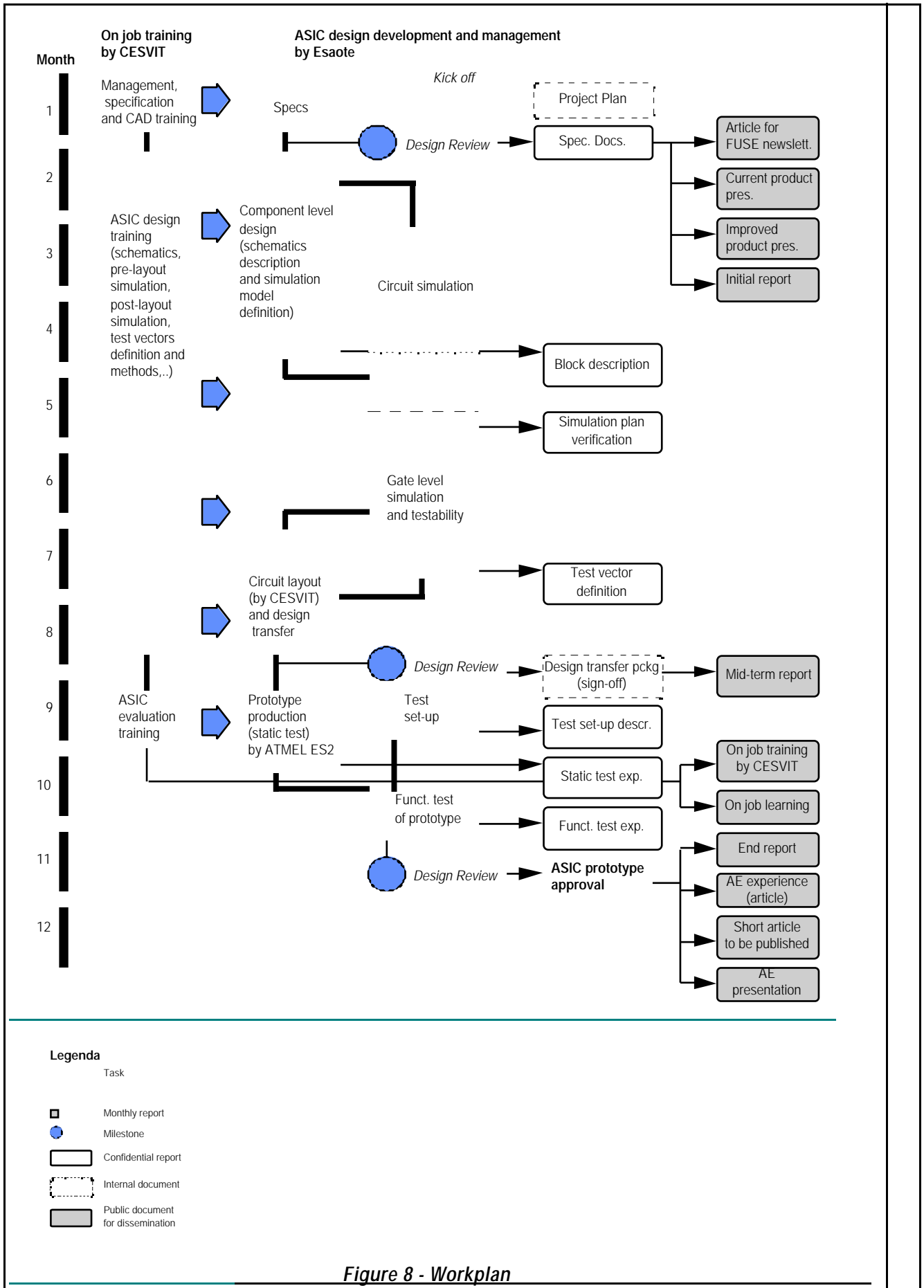


Figure 8 - Workplan

No deviations occurred from this workplan, since the application experiment has been successfully carried out within planned time schedule and budget.

Activities carried out under each workpackage are detailed in the following:

1. Technical management was a transversal activity of project control to make the experiment a success, to fulfil the ESPRIT reporting regulations and to prepare the ground for proper dissemination action. Appropriate training on technical management methodologies was done, especially during the initial phase, to elaborate the Company first ASIC workplan, risk assessment and to select the silicon provider. This task was a very important one since the FU should become an ASIC "maker": the Company's expertise had lacks in these fields, although ESAOTE management had a very relevant knowledge and capabilities. The supporting TTN spent 5 person days to make the Company confidential about all these issues and to elaborate a proper plan in order to reach a "first-time silicon success". The Company spent 10 person days in this training task.

The total effort spent on this workpackage was 37 person days.

2. On job training While the on job training was planned as a self-standing workpackage, mainly for reporting convenience, actually it affected all the workpackages, from the management to the ASIC evaluation strategy definition.

The total effort spent on this workpackage was 63 person days, 42 of which spent by the Company and 21 spent by the subcontractor.

3. Specification The subcontractor trained ESAOTE in the activity of specification definition, in order to produce detailed and finalised definition of:

- technological and technical characteristics of the device,
- its functionality,
- acceptance level of performance and reliability.

In these tasks, the subcontractor spent 2 person days and ESAOTE 4. Total effort spent was 8 person days.

4. Design was the effective development activity made of the following tasks:

Component level design. Subcontractor trained the Company in using CAD for ASIC design. In this task, the person days spent were 2 for the Subcontractor and 4 for the Company. Two main subtasks performed by the Company were:

- functional partitioning of the general device into sub-modules, each defined as stand alone with input and output signals, in a way that it could be easily described through the identification of the necessary basic functions
- schematic description and the translation from Viewlogic to Cadence, in order to obtain a VERILOG netlist of each module.

Then a simulation method has been defined to validate the same modules and the simulation model has been written. Once that all modules have been validated, the top level architecture has been assembled in order to describe the global device. At this stage the testability strategy was selected with the help of subcontractor CESVIT, taking care of device architecture as well as of the fault coverage goal. The Subcontractor spent in this task 2 person days.

Circuit and gate level simulation and testability. The simulation model has been converted into simulation procedure. Each block has been individually simulated taking into account that behavioural simulation doesn't care about layout implementation details, so that the model keeps on being portable during all its validation phase. After validation of all sub-modules the functionality of the global device was simulated. ASIC circuit libraries were used, the clock tree structure was implemented and all constraints relating to the specific technology were taken into account. Simulation were done, exploring the best and worst

cases, in order to validate that design has been successfully completed. The scan chain for a full scan testability was introduced.

Circuit layout and design transfer. The device was then placed and routed as per standard ASIC P+R flow: placement of the I/Os according to the pinout required by the application, placement of blocks and standard cells, routing of supplies and critical nets, routing of all other nets, extraction of parasitic information for accurate post-layout simulation. The placing and routing activity was carried out by subcontractor CESVIT in 5 person days, basing on a specific agreement for external service. All functional simulations were processed again, checking that no difference occurred. Fine adjustments have been made on circuit layout to ensure the best performance of the circuit. Then a final check has been carried out to verify that all state-of-the-art methods have been respected, in order to guarantee the success of the manufacturing operation. Preparation of documentation (design review) and design transfer package (sign-off).

Design workpackage required a total effort of 129 person days for ESAOTE Company.

5. Prototype manufacturing this task has been carried out by the silicon foundry as service. Design transfer package has been converted into formats suitable for mask making and related masks for manufacturing were produced. Silicon wafers were manufactured and assembled into selected package. Only prototypes that passed static test according to the implemented test sequences were supplied. 20 person days were spent by the foundry to carry out the chip fabrication.
6. Testing Test activity was carried out in two tasks respectively related to:
 - the implementation of the validation plan (at speed functional test in real environment), including tooling definition, test bench creation and lab test indication
 - the prototype functional verification with a such plan.

The subcontractor trained the FU with continuity during all the project phases long, by close working with and monitoring of the Company.

The resources allocated by Esaote in the project were involved for an overall of 13 person months, of which about 2,5 person months (2 people) spent for on job training. External subcontractor CESVIT people (1 person) has been involved in on job training for half of time of Esaote personnel.

The Esaote personnel allocated to the project was:

- 1 Senior scientist engineer specialist in digital electronic design.
- 1 Scientist engineer specialist in digital electronic design

In Figure 9 the participants in each task and the percentage of resource allocation are reported.

Resources percentage allocation	
Internal resources	57%
External resources	43%
Of which:	
CESVIT training	11%
CESVIT service	1%
ATMEL-ES2 foundry	31%

Figure 9 - List of participants in each activity and percentage of resources allocation

The total cost for the application experiment, including a small lot of ASIC engineering samples, was of 88 KECU, whose breakdown is as follows:

	ESAOTE		CESVIT		ATMEL-ES2	
	Labour (person-day)	Total cost (KECU)	Labour (person-day)	Total cost (KECU)	Labour (person-day)	Total cost (KECU)
Management	37	9.20	-		-	
Training	42	10.45	21	13.50	-	
Specification	8	2.00	-		-	
Design	129	32.10	-		-	
Fabrication	2	0.5	-		20	16
Testing	17	4.20	-		-	
Total	235	58.50	21	13.50	20	16.00

To better understand interactions that the Company conducted with the Subcontractor, it has to be reported that for each fundamental step of the ASIC design and development, the subcontractor gave Esaote personnel the basic methodological approach to execute such step. It was analysed how to carry out the activity and which parameters could be defined as reference points to evaluate the results of execution as well as possible alternative implementations. The activity was then execute directly by Esaote personnel and the outputs revised and commented, step by step, with trainer to give Esaote personnel the opportunity to understand if the methodology was correctly applied or not and why. Through such constant review, Esaote personnel learnt how to approach correctly the design problems and it was able to face trouble and work out the most satisfactory solution in each step.

The following table reports a brief description of knowledge transferred during key-tasks, person days spent by the subcontractor and the FU and description of the rationale to subcontract activities carried out.

Please note that FU spent more time to carry out the remaining tasks for the project or to complete the ones reported with other activities not directly relevant to the knowledge transfer process. For example, whole the Management task required to the FU an overall effort of 37 person days.

Activity	Person/Days Spent by:		Description	Rationale for subcontract
	FU	S/C		
Technical Management	10	5	Support on the first FU ASIC workplan; risk assessment evaluation; silicon provider selection.	Due to the first use of ASIC technology the FU required training on managerial issues, even if was already skilled on general project management aspects. A proper risks evaluation and interface with Silicon Vendor was crucial for the right ASIC development.
System Specification	4	2	Support on definition of ASIC operational specification, in order to state the technological and technical characteristics, functionality, acceptance level of performances and reliability of the new device.	The company didn't know how to specify ASIC and required subcontractor training for this task. Again it was essential, especially considering that the Company's aim was to become an ASIC maker in future.
Design	42	14	<u>Component level design</u> Support on using CAD ASIC design tool. Functional partition of the device in order to define all the sub-modules; schematics description and its translation; netlist extraction of the all sub-modules; simulation method definition; testability strategy definition <u>Circuit and gate level simulation and testability</u> Conversion of the simulation model into simulation procedure; validation of the all sub-modules and of the global device; Simulation of the best and worst cases.	Technical issues on the whole ASIC design flow obviously required subcontractor's assistance, since the FU had no experience on it. Tasks of simulations as well as testability strategy definition were specially cared. Special FU's requirement was that to be able to use subcontractor's EDA facilities.

Risk analysis and contingency plan

The whole workplan was jointly fixed by the Company, the subcontractor and the foundry, so it already took into account scheduling contingencies of typical risks and problems that could occur while approaching this kind of projects.

For the evaluation of the duration of the different phases, it was to be considered that being at the first experience, times are not the same as for an expert in this sector. The main risk was a potential wrong designing approach of Esaote designers, due to their first time use of ASIC technology, not timely corrected by the trainer subcontractor with needs to repeat the step. In this sense, the subcontractor should give the specific indications.

Another aspect that surely could increase time is the familiarity of the subcontractor with the chosen foundry. If this is not good, there must be an initial period for co-ordination, not always easy, given the complexity of the theme.

The proposed and the actual budgeted time span for this AE has been one year. Monthly progressive review reports for the technical management have been introduced to better control the project.

The internal need to speed up diagnostic ultrasound equipment realisation, giving top priority to this AE, as well as the good support of trainer that avoided critical mistakes by Esaote designers, made to achieve the ASIC resulting from this AE about 10% of time ahead of planned.

Detailed risk analysis and contingency planning is provided hereafter:

RISK	Risk Level	Contingency Plan
Management Workpackage		
Personnel change	Very Low	Selected a suitable staff of company people to be involved in the project A back-up designer to be continuously well-informed on the content of the job.
Training Workpackage		
Insufficient training planned	Low	An additional training to be made with cost supported by the Company
Insufficient designers' skill	Low	Company designers were selected jointly with the subcontractor on the basis of their capacity. Qualified subcontractors would have helped in replacing people if needed.
Design Workpackage		
Change in specification	Low	A dead line for specification change was defined. Qualified subcontractor involved for helping in providing system specifications
Delay due to complexity under-estimation	Medium	A back-up designer to be involved in the job. Workplan would have been modified trying to maintain milestones.
Insufficient performance for the ASIC part.	Low	ASIC to be integrated with cell blocks already characterized and available by the Foundry
Budget out of bound	Medium	The Company would have supported additional costs.
Fabrication Workpackage		
Delay in chip fabrication	Low	Possible delays may occur. Negotiation with the Foundry which has the interest in the production.
Test Workpackage		
Test points out fabrication problems	Very Low	Another prototype fabrication would have been required.
Test points out design problems	Medium	To be evaluated: external patches would have been done in order to proceed with the AE.

Product functionality not satisfying	Very Low	Problem analysis would have been done in order to decide if to repeat the experiment.
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10. Subcontractor information

Selection process

Due to the strategic decision of setting up an in-house ASIC design centre, it was important that the subcontractor to be chosen could follow the Company staff very closely. Hence it had to be located in a place easily accessible from company operational site (Genova - Italy). These logistic reasons excluded any potential foreign subcontractor and most of Italian located too far from Genova.

Among possible accessible subcontractors, some university centres (and among them specifically the Electronic Engineering Department of Genova University) were more than adequate in technical competencies for the project as for the ASIC development as for on job training. But they were not adequate, for their itself cultural background, to give support on managerial aspect as it could be in the spirit of industry (times and costs).

Alternatively to this some silicon foundry development centres were considered. They were adequate as for technical as for managerial aspects in the full respect of industrial requisites, but it is hard to obtain suitable on job training for knowledge transfer. They want to have the full job committed.

The subcontractor has been selected in accordance with the following criteria:

- Relevant expertise & experience regarding the design of ASICs
- Accessibility and flexibility
- Links with other suppliers
- Average hourly cost ranging within 50-60 ECU

The optimal solution has been found with CESVIT S.p.A.. Its Microelectronics Centre has a strong expertise for all management and technical aspect for ASIC development. Furthermore, CESVIT operates with industrial criteria suitable for Esaote purposes and, in particular, is a public structure with mission to stimulate diffusion of high tech know-how to industrial reality, i.e., it was more than appropriate for supplying the necessary on job training.

CESVIT

The expertise of CESVIT - Microelectronics centre in the ASIC field is focused on both project management and design. Its competence ranges from feasibility studies, specification and project planning, through design activities to the final layout and procurement of devices.

During the project development, the Microelectronics centre gave a fundamental contribution to the management with regards to planning and monitoring of activities and risk assessment. Subcontractor provided also a qualified support about the feasibility study, specification and component development. Special support was offered during the design phase for what concerns design methodologies, ASIC EDA tools and testability issue.

Moreover, it has provided a support to the FU about the interface management to the Silicon Vendor. The Microelectronics centre has a good experience rising up from contacts with several and different Silicon providers and complementary suppliers for accommodating both small volume and large volume production, and it helped in an unbiased selection of them.

The subcontractor offered a very flexible interface, for what concerns both the accesses to its services and the accommodation of company's requirements.

Contractual Issues: Esaote implemented a project using ASIC technology. The subcontractor role was mainly devoted to provide on job training to the Company. The IP concerning the implementation of the filter (that was the AE object) was covered with a non-disclosure agreement between the FU (ESAOTE) and the subcontractor : the subcontractor declared its commitment to not use the developed filter for commercial purpose. The contract was a simple one based on a standard offer describing the cost and time allocated to

the work and then on the respective order. This kind of contract revealed to be really effective and adequate with respect to the project characteristics. Cesvit carried out activities within time and costs as reported in the offer/order, both relating with the technical and managerial aspect of the project.

Internal Review:

In order to define the subcontractor performance, the efficiency was estimated calculating the ratio between the effort budgeted and the actual effort spent on it. Figure resulting from this ratio quantifies, more than simply the performance, the quality of the knowledge transfer process between subcontractor and FU. The efficiency ratio was high: the interaction between subcontractor and FU was very good. The total yield of the project can be assessed as positive, since ASIC development has been carried out within time and within budget. The following table summarise this information:

Training Issues	Person Days		Efficiency	Description
	Budgeted	Actual		
Technical Management	5	5	High	Support on the first FU ASIC workplan
System Specification	2	2	High	Support on definition of ASIC operational specification
Design	14	14	High	Component level design, circuit and gate level simulation and testability

ATMEL-ES2

ATMEL-ES2, acting as silicon foundry service provider, is an established, experienced ASIC supplier with worldwide clients from start-up to industry leaders. ATMEL-ES2 satisfies a number of international quality standard, including ISO 9000 and CECC and it is in final stages of QML qualification - the first European ASIC manufacturer to achieve this status. The contract followed the ATMEL-ES2 standard. No problem was encountered on this contract form and no one project or manufacturing activity required special contractual conditions.

11. Barrier perceived by the company in the first use of the AE technology

Even before starting this application experiment, Esaote recognised needs to innovate its ultrasound products by the introduction of new technological approach with digital electronics.

The major barrier preventing from this innovation was due to the conservative attitude of the Company management.

A first attempt to innovate was limited for economical reasons, like the needs of cost efficiency in the short term, due to the limit of budget available in relations of global R&D actions. As a matter of fact company management preferred, at fist, to approach digital solutions by the use of discrete commercial components instead of ASICs to realise the same functionality also if with less but acceptable performance.

This kind of strategy failed, showing, in any case, lacks in terms of security (circuit realised using discrete components is well understandable by others, then it can be copied), low integration, higher direct costs (more PCB and power consumption, lower reliability) and non direct costs (warehouse costs, maintenance costs, obsolescence risk).

On the other hand, the technical staff thought that the ASIC represented the best solution for the company, due to the similar signal analysis for the low-end and high-end product and the reachable integration level.

For a such achievement **other barrier was anyway in the lack of in-house technological knowledge both concerning managerial and technical issues**: neither the managers nor technicians were able to conduct a proper feasibility study and construct a workplan (personnel planning, financial planning, selection of silicon foundry, risk assessment, ...). Furthermore the Company was **lacking of skills and knowledge in the specific ASIC development areas**: design tool selection and use, architectural definition, design development, test definition, etc. It was then necessary to be trained by an experienced consultant, and maintain an internal ASIC design unit as part of company normal investment in R&D know-how innovations.

Once that methodological approach for training internal ASIC team was recognised and defined, again the main barrier of Company management reluctance arose. The management felt afraid for the investment peak and payback in the general economic terms of R&D ESAOTE investment, looking also to the other important priorities that the company had to realise.

Management conservative attitude can be understood if considering the whole scenario of the innovation in the diagnostic ultrasound equipment sector.

	1994		1995	
	R&D 1994 (MECU)	R&D 1994 (% of turnover)	R&D 1995 (MECU)	R&D 1995 (% of turnover)
ESAOTE	7.9	6.5%	8,7	7.2%
ACUSON	59	17%	55	15.8%
ATL	47	16%	41	13.7%

Figure 10 – Esaote's R&D expenditure versus major extra-European competitors (Source IMI SISE CO)

Esaote invests 7.2% of the turnover realised with its own products (i.e. excluding the turnover coming from third party product commercialisation). In absolute value this amount is little less than 9 MECU. Considering that mean European expenditure in R&D is about 5%, this percentage appears quite relevant and it is indicative of the noteworthy efforts that Esaote dedicates to product innovation.

The high, for European standard, but lowest amount of R&D investment compared to its Americans and Japanese major competitors (see Figure 10 as indicative example), is balanced by the major efficiency of the R&D approach used by Esaote as an essential parameter to survive in this framework. Esaote was born as mid-low end products manufacturer and it has always taken in account projects with specific limits: only products with market interest, reasonable development cost and with defined time-to-market can be realised.

The high, for European standard, but

The innovation factor is surely regarded as a risk element of the diagnostic ultrasound sector (and of the electromedical sector in general) with its criticality in the R&D process: lack of innovation or failure to innovate are decisive negative factor for the survival possibility of the company. During 1995 over the 80% of Esaote's ultrasound turnover was originated by diagnostic ultrasound product not more than two years old. In Esaote, the realisation of a new diagnostic ultrasound system lasts from the 18 months (with a commitment of about 20-25 person years and 1-1.5 million of ECU) for the simplest low-end product up to the 36-40 months (with a commitment of about 30-40 person years and 2-3 million of ECU) for the most sophisticated and innovative high-end product. The mean lifetime for such product is about 5 years but product becomes old and mature with strong loss of margins (more than 50% reduction) after 3 years. Typical Esaote's sales volumes go from the order of 1000 units per year for the mid-low end product class to the 300-400 units per year for the mid-high end product class.

Considering that ASIC needs in Esaote could request about 2% of total R&D investment, incremental investment for intensive training will request to almost double this investment in first years and a further 1% additional investment in second years with an economical break even point only after 5 years from beginning. Looking at the global situation, the management has to have to subtract resource to some other critical R&D activity, lowering its efficiency, to satisfy this investment peak and this constitute the financial barrier to proceed.

The FUSE action represented for the Company the better way to overcome this psychological and economical barrier, achieving in the same time many other goals, like the technological and technical improvement of the technicians involved in the ASIC development and, moreover, the improvement in the ASIC managing.

12. Steps taken to overcome barriers and arrive at an improved product

To solve the barrier of lack of technological knowledge Esaote looked for experienced people able to support Company staff for both the managerial and the technical aspects related to the ASIC technology. Luckily it came in contact with the local FUSE TTN, which was also skilled about ASICs.

This contact with the TTN revealed to be a key-action in order to:

- clearly define Esaote role in the ASIC design process in relation of the specific needs and purposes of the company;

- clearly understand the procedure for risks assessment definition to have the best chance of a successful achievement as for economical as for technical aspects;
- clearly define needs to be satisfied to be able to reach the proposed objectives, with particular reference to what it had to be the instrumentation (hardware and software) that Esaote personnel had to have available in house and what to be selected, time by time, outside for playing its role in ASIC design with the major efficiency.

The preliminary activity carried out with the TTNr's help was the individuation of Esaote personnel suitable to be involved in ASIC design and the realisation of the feasibility study of the project, starting with the definition of the ASIC general characteristics (functional and constructive) and the related risk analysis.

On the ground of this evaluation, a preliminary selection of the development tools and of the silicon foundry were made. As far as concerns former issues (tools), the final decision was delayed to a more advanced stage of the project when the company would have got enough know-how to have clear what it has to be its role in the ASIC design process and at what extent.

For silicon foundry instead, it was preferred (at substantially equivalent economical and technical conditions) a company already having business and personal relationship with Esaote to make easier the interfacing operations and, for more, potentially interested to an exploitation of the AE final results.

At end of this preparatory activities, the ASIC workplan (inclusive of forecasted cost and timing indication) was realised. Esaote personnel was allocated to perform the job receiving the necessary know-how to operate via an on job training supplied by the subcontractor. **The workplan resulting from the best practice approach has been then submitted to Esaote management for approval. It was the key to overcome the barrier of the management reluctance**, for finally convincing the management to support this investment. Business and personal risks involved in technological innovation were overcome by best practice planning and risk analysis.

The financial barrier for extra investment, also if the project was considered highly interesting, limited its full clearance execution by the management. Considering only the ASIC design needs in Esaote (2% of the total R&D budget), this investment requested to double investment in the year of execution with a payback three year after its conclusion.

Esaote management tried to proceed with a more dilated investment (24 months instead of 12 with a 50% of forecasted activity leading to 50% increase in ASIC investment per year for two years). In this case availability of FIR filter solution would have been delayed of 12 months with a general sufferance condition for the echographic product development.

Esaote decided then to apply FUSE funding for this AE. Proposal was positively accepted and Esaote was able to receive a technology transfer training and develop the ASIC performing the specific digital filter functionality with the most optimal time forecasted by original workplan (12 months) and with additional advantage to have a payback in one year after project end.

13. Knowledge and experience acquired

Objective

Main Company aim was that to gain as much expertise as possible about ASIC technology so that to be able adopt it autonomously in the future on a number of different Company's products.

Actions and knowledge acquired

In collaboration with the subcontractor, ESAOTE pointed out the methodological approach to train an internal ASIC unit whose first goal were to develop the ASIC FIR filter as case study.

Thanks to this application experiment Esaote gained knowledge in the field of design and development of digital ASIC devices, performing directly the experiment in a way to realise the specific device and, at the same time, to acquire the necessary expertise to autonomously reuse the technology in the future.

Main managerial and technological achievements were:

- Learning of how to define the specific management plan (steps definition, content of activities for each step, kind of necessary tool and service, supplier of tool and service, design review methodology for each partial achievement).
- Learning on how to pay attention and weight the major factors that has to be considered, by themselves and in relation to the globality of the project, for the complete ASIC specification definition: board space, performance, cost and reliability, selection of manufacturing technology and manufacturer, CAE tools.
- Learning of the model for the appropriate logic flow of necessary steps and useful sequences to carry out an ASIC project. This general model can be used as reference for the application in whichever future ASIC project to be developed. A reference guide to make up the specific ASIC requirements documents, like ARS (ASIC requirements specifications), ADS (ASIC detailed specifications), ADD (ASIC detailed design) and VTP (Validation Test Procedures), has been supplied to Esaote by the subcontractor.

Specific technical knowledge has been acquired on following main topics related to ASIC design:

- design for testability to ensure an appropriate degree of fault coverage through the analysis of the architecture and insertion of necessary test circuitry;
- conversion of the simulation model into simulation procedure; individual behavioural simulation of each block without care of hardware implementation details and constraints; simulation of the global device functionality;
- utilisation of specific CAD tools (Viewlogic and Cadence) for ASIC design. The validity of acquired experience has been verified through their use to develop the component subject of this application experiment.

In the original approach of the proposal, Esaote technicians had to execute all the work in-house with a CAD workstation able to support simulation functionality of design (schematics) in ViewLogic environment and design development under Cadence Design Kit (placement and routing).

The purpose for that was to have an in-house set of development tools valid both for the AE project and for further replications of the experiment at the most large extent, with the results ready to be simply given to a silicon foundry for production.

The analysis about requisites for simulation tools, performed jointly by Esaote and its trainer CESVIT, indicated that the ViewLogic EDA, already existing in Esaote, was suitable for the needs of the project and also for the foreseeable use that Esaote could have needed in the future. Furthermore choosing to design the component using ViewLogic schematics would have allowed its portability in every developing system today in use. This was very important for the Company since it would allow the workteam to develop new ASIC design or to modify an existing one without to be bound to the tool for placement and routing.

As a matter of fact Esaote interest is to have the know-how for designing the component, reserving to choose time by time the most suitable manufacturer, in consideration of the most suitable fabrication technology for the component and of the number of devices to be produced.

- complete Viewlogic Viewsim command set for simulation utilised to do command files for generating pattern vectors.

A major attention has been put to evaluate the restricted commands set that it could be used to create these command files in relation to the silicon foundry manufacturing process, because each foundry recognises only some subset of this command. For example, some foundries request that all input/output data in the command file have to be written in radix binary form instead that in the most common decimal or hexadecimal form.

Esaote project engineers have been driven in their work by the external support of the subcontractor and by several software information provided by the ATMEL-ES2 technicians, in order to acquire a basic

expertise to fit, without any understanding doubt, the command files software for test vectors as the foundry required.

This ASIC design has produced in Esaote a fundamental internal know-how useful for new applications in future replication of ASIC developments.

14. Lessons learned

General considerations

Before to start with a project using a new technology it is necessary to have clearly assessed the complete feasibility of the ongoing experiment.

The success of an AE project depends only partly from the technical content of the experiment. One of the key-actions to be done is to evaluate risks associated with each activity and therefore to define the time and the costs necessary to carry out the project with the expected results.

The presence of an external skilled organisation involved in the project, with technical and managerial role, is also very important: on one hand it forces the Company's technicians to an additional effort because, but on the other hand a continuous exchange of information and a confrontation with different experiences produces good results; especially during the contract definition i.e. with silicon providers, this could give additional benefits to the FU.

ESAOTE experience

The following are few more items that comes out from the Company experience and may be assumed as useful rules for anyone who wants to apply to similar projects:

1. The first learnt lesson is concerning the correct economic evaluation of the convenience to use a new technology to improve a mature and stabilised product. These new experiences require methodologies, skill, documentation, new product configuration whose costs are not often considered, since they don't seem to be strictly relate to the technological and technical issues..
2. Since the sector of ASICs has been constantly evolving, our acquired experience is that it is important to follow the technical trend through the contacts with the subcontractor and foundry, by participating in seminars, training workshop etc.
3. In the application experiment it has been stressed that a clear definition for needed CAD workstation and software tools would be defined only after an analysis on the results of CAD training and of ASIC specifications.
4. When a Company plans to get ASIC development process in house, the limitations of the tool risks to be a limitation in the choice of manufacturer or to have a design kit over dimensioned respect to its real utilisation to cover the maximum flexibility in foundry selection. It is also important to choose a development tool that allows not to be bound to any tool for placement and routing.
5. Every time that an ASIC is developed, a specific manufacturer has to be selected, in relation to the complexity of developed component and to the number of components requested for production. For instance the same ASIC produced by modification of an already existing one to be adapted in a new product could request so different production numbers that it could be not convenient to use the same manufacturer as for the original one.
6. It is worth to estimate if all functions regarding the steps from circuit placement and routing up to production could be better and more cost-effectively performed through external services. The necessary expertise to have control also in these operations is that o have a sufficient know-how of the technology and the methods of implementation just to select the most proper suppliers.

7. As last issue, Esaote learnt that a fundamental aspect is to select a silicon vendor ready to follow the Company's technician people concerning all the requests they can do. Direct and personal relationship has been found very important to speed up time and to minimise or avoid misunderstanding effect.

15. Resulting product, its industrialisation and internal replication

Industrialisation

The production of a small but meaningful quantity (200 unit) and the test performed in the real environment of board to be used in the ultrasound system have demonstrated the reliability of manufacturing process, the successful degree of device performance and the economic advantage of such solution. The same silicon foundry (ATMEL-ES2) that fabricated the prototype will realise also the industrialised production. This will give the advantage that no other work will be necessary to be done by Esaote on the ASIC project to adequate it to foundry requirements. The industrial production will start in the silicon foundry as soon as Esaote will request such production, i.e., when diagnostic ultrasound system project using such ASIC will be completed and transferred for industrial production (estimate mid 1998).

But the industrialisation interest of this AE is more general than the specific case of Esaote as demonstrated by the fact that the silicon foundry ATMEL-ES2, manufacturer of prototype, requested to have a licence for producing and commercialising abroad the result of this AE and is now proceeding with industrialisation of a version of developed FIR filter to be made shortly available as commercial component of its product catalogue.

In the table below the tasks with efforts and costs of FU and Subcontractor and time schedule relating to the industrialisation phase are reported:

TASKS	EFFORTS (PERSON/DAYS)		COSTS (EURO)		Schedule
	FIRST USER	SUB CONTRACTOR	FIRST USER	SUB CONTRACTOR	
<i>ASIC Project review and analysis for real application</i>	20	5	5K	5K	June 1997 – October 1997
<i>ASIC production commitment (only for technical co-ordination of process)</i>	5	1	1K	1K	December 1997 - June 1998
<i>US Digital front-end project definition with ASIC</i>	1250		450K		July 1996 – June 1998
<i>Product on the market</i>					@ September 1998

Internal replication

First aspect of internal replication is the different use that can be made for the developed component, thanks to the ASIC FIR filter flexibility (coefficient programmability, decimation, cascade utilisation to enhance filtering precision, ...). These features could allow its utilisation for most of digital filtering needs in other diagnostic equipment (not necessarily diagnostic ultrasound ones) under development or to be developed by Esaote.

Second aspect of internal replication is that Esaote got from this ACE a specific ASIC design know-how. and then it will be also able to replicate the experiment to design further ASIC circuits, mainly based on 3 metal layer 0.7µ CMOS process but, with some adjoin specific support, also with any other ASIC realisation process, overcoming actual design restriction of discrete logic for realising specific application in its new products development and free from any other economic and technological constraint derived from outside commitment of ASIC design. As first consequence of this, an ASIC realising the manager function for ordering digital data acquired in an ultrasound system (the so-called FI-FO function) is now under development to replace, with major economics and efficiency, the actual discrete logic. Future further application of ASIC technology could be the innovation of the ultrasound pulser section (with at least 3 ASIC to be integrated in a very complex and sophisticated MCM structure) or of the receiving pre-amplification section (to be integrated directly with piezoelectric transducer and requesting a different ASIC technology respect those of this AE).

16. Economic impact and improvement in competitive position.

The diagnostic ultrasound (echography) sector is very fragmented. In effect, the echograph can be specialised for different medical application (radiology, internal medicine, cardiology, gynaecology, vascular and so on). Each of these segments is characterised by products differently configured and from different "users". Esaote's product range (by its own production) covers today more than 50% of market demand. On the domestic market, this coverage reaches up to 90% through the complementary coverage with Hitachi products range for the very high-end of the market.

Furthermore, Esaote recognised that the future of electromedical diagnostic equipment is based on digital technology allowing innovative performance not possible with the classical analogue technology. This means to design new equipment fully based on digital technology and on the techniques for its applications. In particular, utilisation of ASIC could become more and more a technological and economical ideal solution in the next years to solve many complex circuit functionality.

The company experience has also demonstrated that development of a product destined to a high competitive market, as it is the medical market in general and the diagnostic ultrasound in particular, is effective only if based on company proprietary know-how to control its application in the most convenient and flexible way.

External commitment of technology could be only temporary and in long term won't grant a sufficient flexibility and economicity to be competitive. From this, the Esaote consciousness to have in house the necessary expertise to design ASIC for covering the company ASIC technology demand.

In this context, to maintain a competitive strategy, the development of new and improved product is an essential element for Esaote. During 1997 Esaote renewed its product for mid-high market segment (an enhanced version of actual AU4 to be named AU5) and, in 1998, Esaote launch on the market a diagnostic ultrasound innovative platform for the very-high end market segment (its first all-digital echographic system)

and a new diagnostic ultrasound equipment for the low-end market segment. With this new product Esaote can enlarge its market coverage up to 70%. In Figure 11 is schematically reported Esaote's product coverage.

The continuous product range innovation is very important also in term of margins: the competitive dynamic pushes to price reduction and product innovation. For this, two years ago, just before this FUSE project were submitted, Esaote worked out a three-years plan to develop a sophisticated all-digital echographic system, based on electronic phased-array

technology for top-level scanners, and to improve the low and medium systems, based on mechanical sector technology, with a massive introduction of all-digital technology instead of the present all-analogue technology. Such introduction means not only a product cost saving but also an increase in product performance (like the new 3D imaging and the contrast media analysis) and in quality product standard, a very important condition because in medical care context it is not possible to accept any diagnostical instrumentation failure chance without risk for quality and accuracy of the care.

Esaote market coverage today				
Market segment	Radiology	Cardiology	Gynaecol.	Vascular
High (>100.000 US\$)	OEM		OEM	
Mid-high (>70.000 SU\$)	Esaote	Esaote		Esaote
Mid-low (>50.000 SU\$)		Esaote		Esaote
Low (<50.000 SU\$)	OEM	Esaote	OEM	Esaote

Esaote market coverage by the end of 1998				
Market segment	Radiology	Cardiology	Gynaecol.	Vascular
High (>100.000 US\$)	OEM		OEM	Esaote (*)
Mid-high (>70.000 SU\$)	Esaote	Esaote	Esaote	Esaote
Mid-low (>50.000 SU\$)	Esaote	Esaote	Esaote	Esaote
Low (<50.000 SU\$)	OEM	Esaote	OEM	Esaote

(*) All-digital echographic system destined also to perform 3D and Contrast Media functionalities, first a family of all-digital equipment for different applications and subject for its acquisition section of this FUSE application.

Figure 11 † - Esaote presence in diagnostic ultrasound market

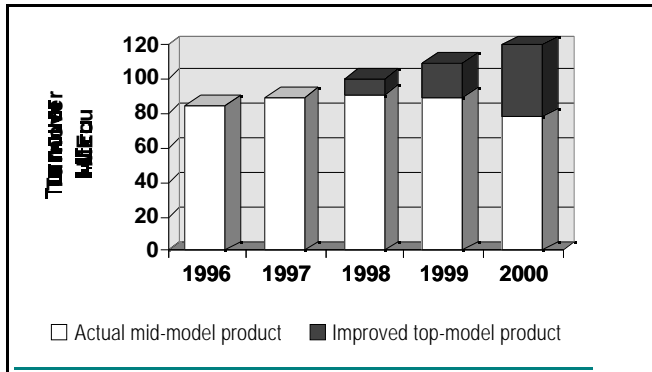


Figure 12 Esaote's diagnostic ultrasound expected turnover

straightway of the ASIC solution, with no further necessity for intermediate, more expensive and not so satisfactory solution that could limit the potentiality of the product in the market.

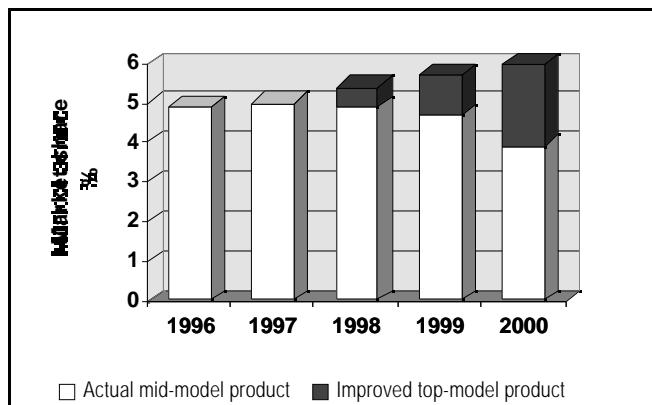


Figure 13 Esaote's diagnostic ultrasound expected market share

Core of this product innovation is the realisation of an all-digital diagnostic ultrasound system. Today, in 1997, looking at the success of the first all-digital echograph coming on the market, it could be tell that not only this plan forecast was more than appropriate but looking to the market it is necessary to speed up as much as possible its realisation.

With the realised ASIC component Esaote will be able to solve the problem of digital filtering for this top level all digital ultrasound systems to be marketed in 1998. Realisation of Esaote's new top level all-digital ultrasound system benefits

The present analogue demodulation and filtering circuitry in the two analogue/digital signal processing board (echo and Doppler) of actual diagnostic ultrasound system will be replaced by two digital board having each chains of some ASIC FIR filter in cascade for a total of 7 ASICs on each board.

The competitive advantage for Esaote to be present with an all-digital diagnostic ultrasound equipment suitable for covering the top-model request from the market is given in Figures 12 and 13 where are respectively represented the expected turnover and market share of Esaote in the next years.

Without introduction of top level all-digital diagnostic ultrasound models, made possible also by the digital filtering solution offered by the developed ASIC, for Esaote it would be hard to be still competitive in the future. Figures 12 and 13 show clearly the decreasing in turnover and market share that could be expected without the product innovation.

The ultrasound product complexity, where filtering is only a part, makes very difficult an estimate of payback and ROI for the specific investment of developed ASIC. Any quantitative calculation is anyway a limiting view, because of:

- the quantitative importance that this investment could have for the general economy of the company (recognise by the decision of the company to accept the risk to proceed with the ASIC maker investment)
- the major quantitative return of the all-digital echograph development, where the ROI of the ASIC FIR filter is within the general ROI of the total equipment development.

A specific consideration for ROI could arise by the economical comparison between the analogue solution and the digital solution (excluding the qualitative technological advantage not quantifiable).

For each manufactured echographic unit, the cost for the analogue filtering acquisition section is of about 950 ECU for the proper filter part with an additional 450 ECU for other electronics component of the boards. To this amount it has to add a 100 ECU amount for the work of analogue filter synchronisation. From this calculation the necessary occasional after sales service for filtering re-synchronisation after some period of utilisation is

not considered. For any manufactured unit, the acquisition unit with its analogue filtering section has a cost of about 1500 ECU.

The cost of the corresponding digital section (made of couple of identical pc-boards) is given by the cost of 14 ASICs (7 for each board) with an unitary cost of about 60 ECU and of about 400 ECU of additional electronics for a total cost of about 1240 ECU.

An estimation of ROI is given in the following table based on the hypothesis of new equipment to be sold in next years (starting August/September 1998). ROI estimation is calculated by cost comparison of digital solution used respect to analogue solution replaced by this one in such equipment.

Year	1998	1999	2000	2001	2002	
Sales of new product (units)	150	550	550	450	300	
Global cost for new digital acquisition section (KECU)	186	682	682	558	372	
Global cost with old analogue acquisition section (KECU)	225	825	825	675	450	<i>Total</i>
Increase of profitability (KECU)	39	143	143	117	98	540

Considering a total cost of the ASIC prototype of 88 KECU and a total increase of profitability of 540 KECU, the ROI is calculated:

$$ROI = (540/88) * 100 = 614\%$$

The payback period results in 12 months

17. Target audience for dissemination

The advanced multifunctional FIR filter.

Originated for the specific purpose to execute the sophisticated and complex filtering procedures of a diagnostic ultrasound system acquired signals, the resulting ASIC FIR filter don't preserve any confidential content of the procedure used by Esaote for ultrasound signal filtering. Its confidentiality arises only from the specific programmability used and the surrounding electronic configuration of the pc-boards where it is installed.

Although Esaote has been forced in developing such FIR filter because it could be find on the market only components with some of the above indicated features but not all together, the developed component general features (cascadability; decimation of coefficient, an overall dynamic of 32 bits; programmability and change of filter coefficient at every clock pulse; interface configuration with a master DSP; choice for the report; low consumption) make it suitable for utilisation in the most sophisticated digital filtering applications.

The interest to this project is far more general than the specific Esaote case as demonstrated by the fact that ATMEL-ES2, the prototype manufacturer, has requested to have a license for producing and commercialising abroad the result of this application experiment. In fact, such a FIR filter can be successfully applied to others sectors beyond that of ultrasound imaging system, like communication, and can help in all the sectors where video and signal processing operations are to be performed. Then, the stimulation to the use of this new microelectronics device, other than the dissemination of its existence made by the FUSE dissemination actions, will be further enhanced also by its commercial availability through ATMEL-ES2.

The following table shows the possible fields interested in the digital FIR application:

Sectors	PRODCOM	Description
<u>Electronic Components</u>		
<i>Telephone Apparatus and Equipment</i>	3220	The signal processing should be take advantage by the FIR filtering features, improving the communication performance and quality
<i>Radar</i>	3230	The signal filtering process extracting radar information should be realised by the FIR improving performance and reliability with space, power and cost saving
<u>Precision Instruments</u>		
<i>Medical Apparatus</i>	3310	Since the FIR was developed to be used in image processing in echotomograph devices, it should be useful used in all the medical apparatus where the diagnostic medical activity is supported by the image analysis, as magnetic resonant apparatus
<i>Instruments & Appliances for measuring, testing, checking ...</i>	3320	The high performance filtering capabilities should be useful in fields as sounding-line and sonar, producing high performance small size devices

In order to better focalise the company to reach in dissemination activity, the following table states the Company characteristics:

- Management:** It works at a really good level; it had not experience to choose technology and methodology to internal ASIC realisation.
- Starting technology:** PCB; SMT; μ P; DSP; FPGA/CPLD, digital and analogue discrete components techniques
- Applications:** Precision Instruments, Medical Equipment
- Development** EDA tools
- Methodology:**
 - Barriers:** Although Esaote recognises needs to innovate its ultrasound products with introduction of new technological approach in digital electronics, the economy reasons was the main Company barrier
- Company Size:** 579
- Company turnover:** About 124 MECU

The experience in ASIC design

The results of this AE under the profile of the lesson learned and the expertise acquired in ASIC design could give useful indication in any industry that needs to introduce a large extent of ASIC technology in its electronic products developing with its proprietary technology without being an ASIC development centre or a foundry.