

FUSE Application Experiment 1708

Dissemination / Demonstrator document

**SMT and FPGA achieve Biomedical Freezer
Controller cost reduction**

Abstract

UK-based Planer Products designs, manufactures and markets biomedical freezing equipment. The company has expertise in product design aspects relating to mechanical, electrical, thermodynamic, refrigeration and electronic engineering. It employs 30 people overall with 4 people in full-time technical roles, and in 1997 had a turnover of about 5 MEuros. The company's medical products are used in four main markets: human in-vitro fertilisation (IVF), human bone marrow freezing, animal embryo freezing and biological cell-line freezing.

The Application Experiment centred on the control electronics for the freezer range, which uses microprocessor, analogue and digital circuitry to process temperature and pressure signals from the freezer. The Experiment reduced the number of components in the controller through the use of a Field Programmable Gate Array (FPGA). This also led to an increased flexibility in customising the operation of the controller, meaning it can now be used across Planer's whole freezer range. In addition, adopting Surface Mount Technology (SMT) for the first time further reduced the size and number of boards in the controller.

Increase in sales is estimated to be to approximately ECU 780k over a five-year period. Payback time is approximately 15 months. The Return On Investment (ROI) is determined to be 350% over the estimated five year of the lifetime of the product. The total cost of the AE was 59k Euros with 54k Euros funded under FUSE. An additional 30k Euros was needed to bring the product to production. The duration for the AE was 12 months.

This project should be of interest to any enterprise with predominantly analogue or discrete component design experience, particularly in the fields of medical electronics, instrumentation or process control.

Keywords and Signature

- Freezer Controller
- Microcontroller
- Machine Automation
- Biomedical Application

Signature: - 0141 555 0142

1. Company name and address

PLANER PRODUCTS LTD
110 Windmill Rd
Sunbury
Middlesex
TW16 7HD
United Kingdom

2. Company size

Planer has 32 employees of which 4 are engaged in design and technical roles. In 1997 the turnover of the Company was approximately 5 Million Euros.

3. Company business description

Established as a small group almost fifty years ago, Planer Companies have been active in research projects for many organisations for many years. The company was involved in the very early stages of research and development of controlled rate freezers and has been designing, manufacturing and marketing such products for over twenty years.

All design elements are managed and controlled from within the Company but some design tasks are assigned to groups of specialists outside the Company. On the electronics side, the company had a

basic in-house through-hole PCB design capability and performed simple designs in-house. Detailed analogue and digital design was subcontracted, but all software for both embedded microcontrollers and PC host systems was developed and maintained in-house.

Planer Products Ltd operates in two distinct market areas that are served through its two divisions, Planer Biomed and Planer Industrial.

The Biomed Division, which is the subject of this project, accounts for approximately 60% of sales and is responsible for the design, manufacture and marketing of biomedical freezing equipment. The company outsources most of its subassembly manufacture, including all electronic subassemblies. Final assembly and test is all performed in-house however. Controlled Rate Freezers are used for the preservation of organic materials of many types and are very specialised products serving the needs of niche markets, in different fields, on a global scale. World-wide marketing, distribution and support is difficult for a company with so few employees so a network of Distributors has been established, through whom the Company operates.

The Industrial Division specialises in tools for the electronics industry. The products comprise items such as surface profile measurement for the hybrid and thick film semiconductor industries and hot gas soldering and rework systems for users of surface mount devices. The range is backed up by value added items including production pre-forming equipment, video based inspection systems, linescan cameras and a range of laser operated measurement systems and motion analysis systems for both industrial and medical applications.

4. Company markets

Controlled Rate Freezers are used in four main markets, which can be grouped as follows:

- human in-vitro fertilisation (IVF),
- human bone-marrow freezing,
- animal embryo freezing and
- biological cell-line freezing

IVF markets tend to develop at a rate proportional to the GNP of the geographical territory concerned, whereas bone-marrow freezing, being related to the treatment of cancer-related conditions, is subject to the development of medical as well as financial resources. In IVF, the company is market leader with approximately 75% of the world market, in bone marrow an estimated 35% of the world market and in biological and animal markets an estimated 15%.

The size of the global market is estimated to be approximately 600 freezers per year across the above application areas, at a value of approximately 10M Euros. Planer ships approximately 250 Freezers per year to the above market areas.

Planer established a lead of several years in most markets utilising controlled rate freezers and through constant development and product improvement has maintained a dominance of the human applications areas in most territories. Competition is strongest outside of the IVF field, notably from Cryomed from the United States, and a number of small Japanese companies, Taiyo Sanso, Nihon Freezer and Hoxan, serving the needs of the Pacific Rim. Within the IVF market most competition comes from a small Australian company marketing a product developed for the animal market and adapted for human use. Its main virtue is its low cost, which is important in some territories.

The adoption of new technology has allowed planer to continue it's strong presents in the IVF market in the face of the competition. Planer market share is substantial and needs to be maintained in the face of stiff competition. If this market share is maintained, coupled with the expected growth in the IVF market, as stated earlier at a rate that is proportional to the regional GNP, then an increased overall sales level will result.

5. Description of the product to be improved and its industrial sectors

The component is being used in an Electronic Controller within a liquid nitrogen fuelled Controlled Rate Freezer. Controlled Rate Freezers made by Planer are essentially insulated chambers into which is injected a stream of liquefied nitrogen (LN₂) which vaporises at a temperature of -196 degrees Celsius. The rate at which the chamber temperature falls is controlled by the rate at which LN₂ is injected and by the application of electrically controlled heater elements. Precise temperature measurements within the chamber provide the electronic controller with the means to control the LN₂ injection and the heating in accordance with a pre-programmed temperature demand curve, retained within the memory of the controller.

The most popular range of products, the Kryo 10 Series, utilises two separate enclosures for the chamber and for the controller. The controller used in the Kryo 10 product is called the MR3 System and is based on a Hitachi HD64180Z microprocessor. The heart of the controller is housed on 3 through-hole mounting PCB's containing the microprocessor, standard microprocessor peripheral ICs, discrete logic and analogue components.

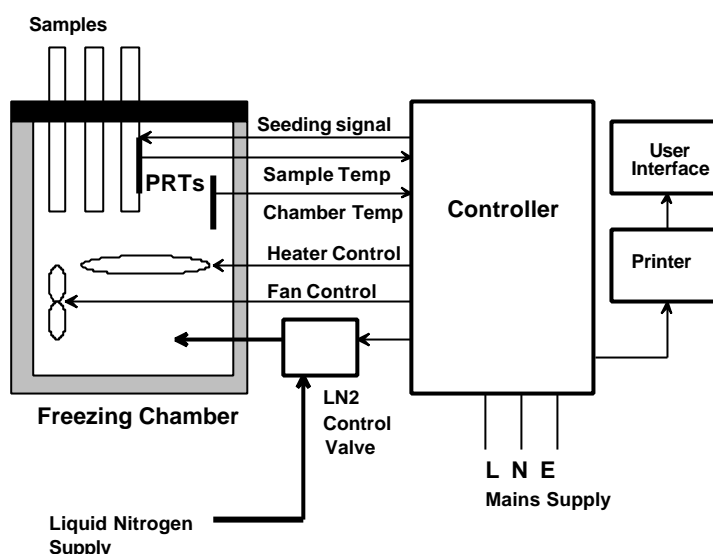
The need for product innovation has arisen as the result of any identification of a number of critical factors to the continuing success of Planer in the field of control rate biomedical freezers: -

- International nature of the IVF market, which is the primary market for Planer's products and competition from Japanese and US companies.
- Product unit cost is a critical selection criterion for some customers, so manufacturing cost reduction per unit is very important.
- High product quality and reliability, high reliability is demanded by customers as Patients undergoing IVF treatment must be reassured that the freezing of their embryos for long term storage does not adversely affect maximum viability of the embryo once thawed and implanted.
- Planer has reputation for its innovative products within the biomedical freezing. This needs to be continually cultivated. This continues this with the possibilities of customisation of the product and in field upgrading, all innovative features.



Kryo 10 Series Product, showing (from L to R) Freezer Chamber, Controller and Host PC

Below is a diagram of the existing system



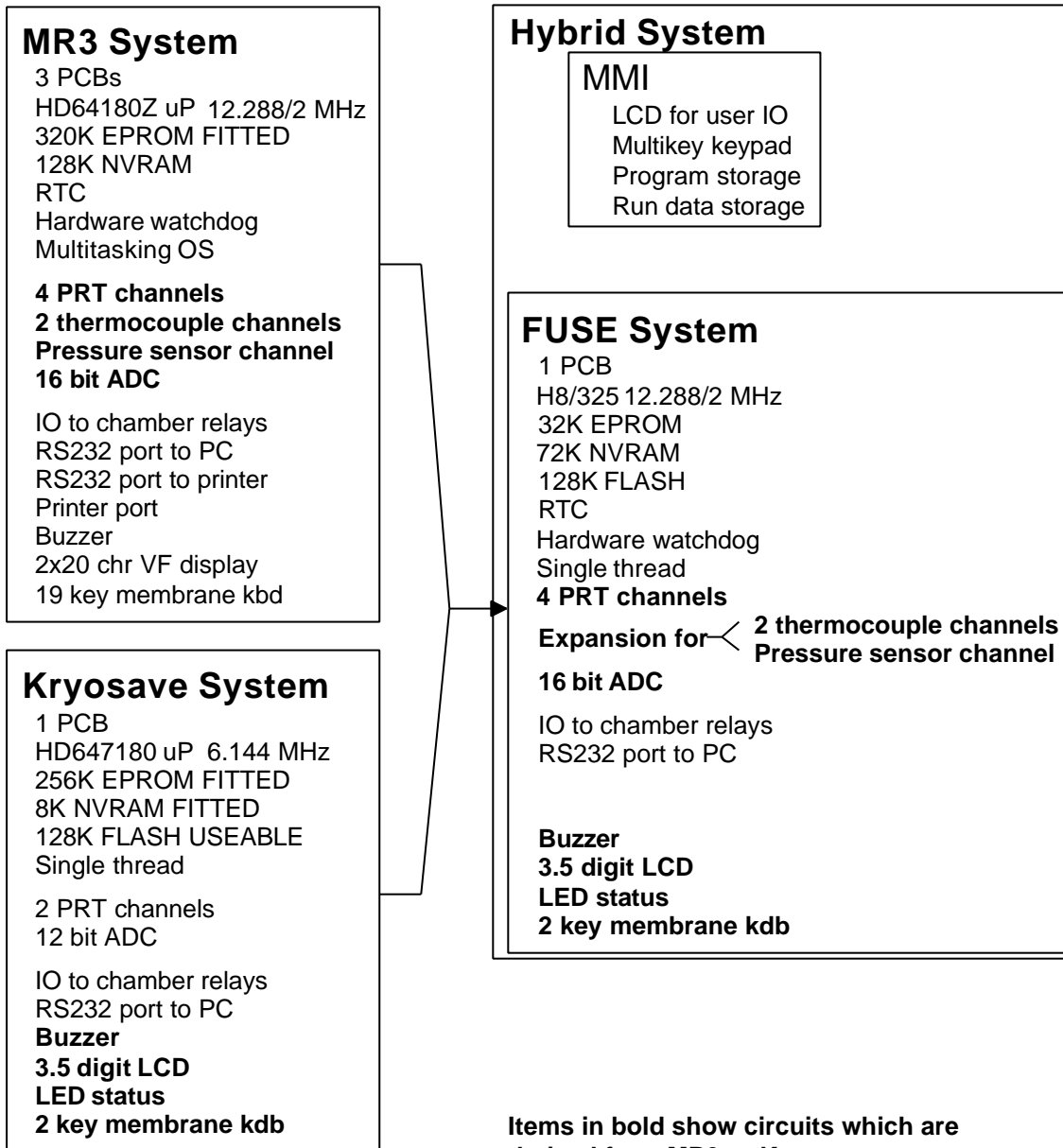
6. Description of the technical product improvements

The 'footprint' of the Kryo 10 product (the amount of space taken up within the laboratory) would be beneficially reduced if the controller enclosure could be eliminated and the MR3 electronics built into the chamber enclosure. Clearly the elimination of an entire enclosure brings about significant cost savings too. From bottom to top, the controller enclosure housed the power supplies, controller module and printer.

The object of the experiment was primarily to achieve a cost reduction in the manufacture of the electronic control module, with no major change in the general functionality of the complete system. This saving was achieved by the reduction of the number of circuit boards, the number of interconnections, the number and size of components, together with a reduction in assembly and test times. Additional other advantages were: -

- A reduction in the product size – as logic is now on a single chip.
- Low cost customisation capability – achieved by the use of flexible design tools.
- Ability to develop and adapt the technology.
- Ability to perform field upgrades – achieved through programmable device use.

The aim of the Experiment was to reduce the number of components in the controller module through the use of a Field Programmable Gate Array (FPGA). In addition, the size and number of boards in the controller was also reduced by the adoption of Surface Mount Technology (SMT). Apart from combining the features of the two predecessor systems, the overall function of the controller was not significantly changed apart from the addition of an improved LCD display I/O capability. This supports the use of a graphics display, rather than just a two-line character display. In most configurations the LCD can be used for plotting temperature curves and replaces the use of a hardcopy printer previously placed at the top of the controller enclosure - again contributing to a space saving.

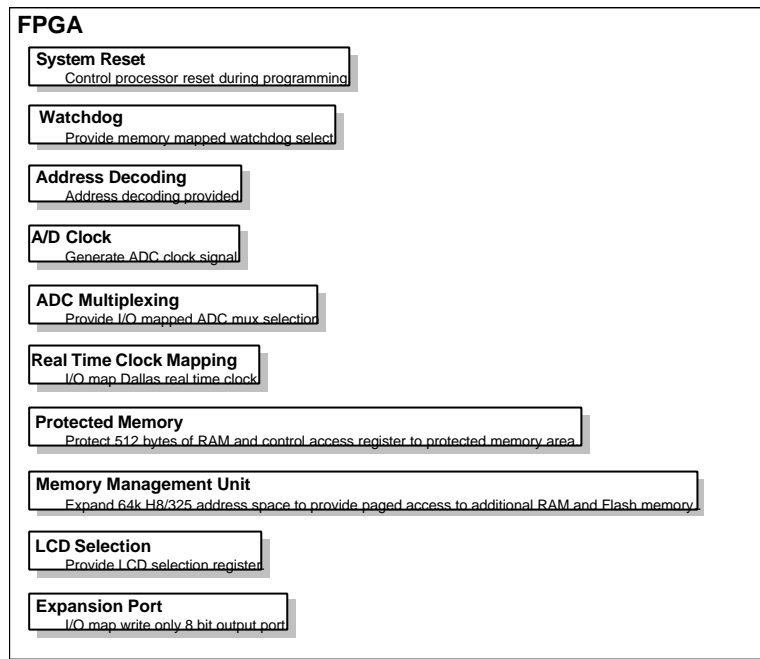


Items in bold show circuits which are derived from MR3 or Kryosave systems.

MERGING OF MR3 AND KRYOSAVE INTO THE FUSE SYSTEM

The diagram below shows the functions included in the FPGA component.

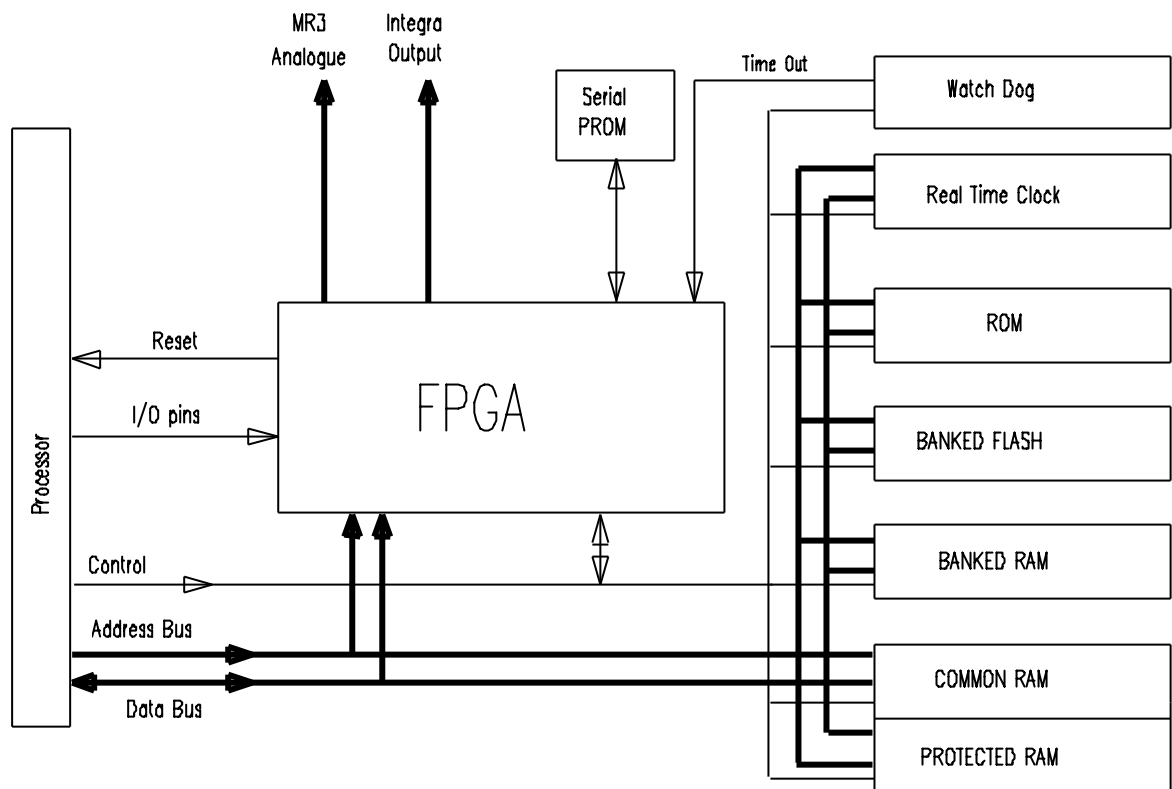
FPGA Block Diagram



Compared with the previous MR3 controller, the FPGA replaces 38 components including 15 ICs. It has 87 functional pins necessitating a 160 pin TQFP (SMT) package. Gate capacity required is approximately 2.5K-3K gate equivalents. Using the FPGA gave a slight increase in bought-in component cost (8 ECU) over the equivalent discrete devices, but reduced board area by 110 sq. cm. alone.

Including the Real Time Clock function in the FPGA was considered as it would be possible without adding many pins. However, design effort required would have been high, given that industry enquiries failed to find a compatible off-the-shelf macro. Also, standby power consumption would be higher than the present dedicated RTC part, leading to shorter battery life.

Block Diagram of MRX with respect to FPGA



7. Choices and rationale for selected technologies, tools and methodologies

7.1 FPGA Device Selection

FPGA technology was chosen since the cost of integrating either the digital-only or the mixed A/D functions into a masked ASIC whilst preserving the high levels of analogue accuracy was not justified by product volume. Use of SRAM-based FPGAs with a single PROM for both hardware and software programming enhanced the capability to supply field upgrades and bug fixes at low cost to Planer's worldwide customer base. Low standby power was also a feature of this solution. Anti-fuse-based FPGAs were considered but these lack in-system re-programmability and actually have higher standby power consumption since they incorporate charge pumps.

The device finally chosen was the Xilinx 5202. This has fewer features and therefore lower cost than the Xilinx 4000 series, but offered all that was necessary for the Planer controller.

7.2 New Microprocessor Selection

It was judged that the use of microprocessors in the existing products was appropriate. The microprocessor was essential to support the computational complexity of the temperature control algorithms and the real-time, multi-tasking nature of the overall control problem. However, soon after the project started the existing microprocessor vendor announced that it was planning to cease making the device then in use. Consequently, it was not recommended for inclusion in new designs.

A variety of microprocessors were reviewed to determine the best fit for the new design. These included the Hitachi H8 series, Motorola MC68HCxxx series and the Siemens SAB80C166. The H8/325 processor was finally chosen. The advantages and disadvantages given below were in comparison to a range of 8 bit and 16 bit processors.

H8/325 8 bit Microprocessor

Advantages

- Low immediate risk development as developer was already familiar with porting from Z80 to H8 series
- Low unit cost
- Development tools already available
- Makes best use of FPGA capabilities.

Disadvantages

- Unable to create curves in real-time
- More extensive memory management in FPGA
- Less spare capacity for future proofing.

7.3 Tools and Methodologies

Schematic based circuit design was chosen for the PCB as this mapped well onto the company's existing capability and working methods. Additionally, VHDL was adopted as the method for the entry of the FPGA design as the company was comfortable with managing and understanding a descriptive language without the need for a schematic representation. It complemented their existing software expertise. Software design proceeded according to the company's established procedures.

Functional testing was performed in-system using a mixture of the present, through-hole PCBs and the new SMT PCB. This allowed the concurrent use of FPGA and microprocessor in-system debug tools. No special Design For Test, (DFT) features needed be incorporated, as SRAM-based FPGAs are 100% tested at manufacture.

Final evaluation of the full controller was completed using existing rigorous test schedules as used for the existing product ranges. Each freezer performs a range of freezing programmes, the results of which are predicted by a wealth of statistical data collected over a number of years. All new freezing products, or variations to existing products must conform to the same QA standards as previous products.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

The Company has expertise in product design aspects relating to mechanical, electrical, thermodynamic, refrigeration and electronic engineering.

The support for such highly technical range of products demands a high level of expertise be retained within the Company, hence one mechanical engineer, three electronic engineers are involved full time in development and other engineers of Chartered status are employed within other departments of the Company.

On the electronics side, the company had a basic in-house through-hole PCB design capability and performed simple designs in-house. Detailed analogue and digital design was subcontracted, but all software for both embedded microcontrollers and PC host systems was developed and maintained in-house. The resources mentioned above were assigned to the project part time.

9. Workplan and rationale

9.1 Rationale

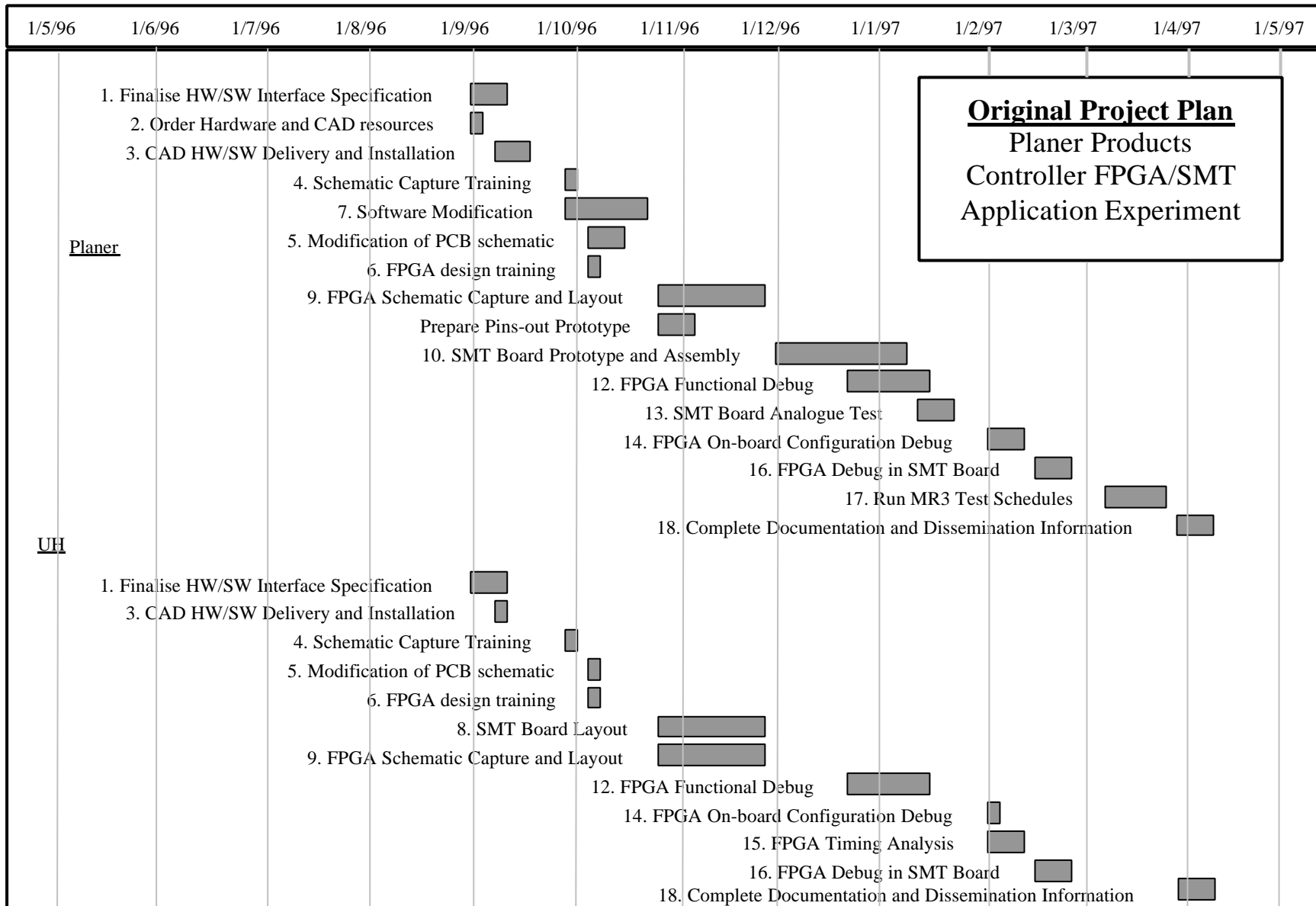
At the outset of the project Planer had in production two main types of electronic controller known as MR3 and Kryosave. The original project was intended to produce a replacement for the MR3 controller using a Field Programmable Gate Array (FPGA) and Surface Mount Technology (SMT) in order to gain the following benefits:

- Create a system, which does not require the elaborate enclosure currently used on the MR3.
- Reduce the number of components in the MR3 through the use of the FPGA.
- Reduce the size and number of PCBs through the use of SMT.

The original design process was envisaged as follows:

- Specify the design
- Modify the schematics
- Modify the software
- Layout the FPGA
- Prepare a pin-out prototype based on current MR3 PCBs
- Test on pin-out prototype
- Layout SMT PCB
- Test on SMT PCB

The original workplan schedule is shown on the next page, along with the allocation of tasks between Planer and UH, the subcontractor.



However, during the specification stage it became clear that using the MR3 as the basis for the design was neither the most practical nor the most desirable route. Instead, it became apparent that the Kryosave product could be combined with the MR3 to create a hybrid system, which would then be redesigned using SMT and an FPGA. This was coupled with the discovery that the 64180 microprocessor, used by both products, was not recommended for new designs by Hitachi. Although no obsolescence date had been formally released it was felt that moving with a microprocessor at the tail end of its life was not appropriate for a major redesign of the PCBs.

Given the requirement for a fundamental review of the design to accommodate the microprocessor change, the key functions of the MR3 were reviewed. The product was split into two main functional elements, a chamber controller and a man machine interface (MMI). It was quickly realised that the FPGA and SMT technology would allow the design of a small Chamber Controller, or Engine, which would be common to all Planer freezer products and could be differentiated across the range by the addition of the MMI.

Therefore the MR3 and Kryosave systems were compared and a hybrid system devised, with the MMI removed. The key benefits for this approach are summarised below:

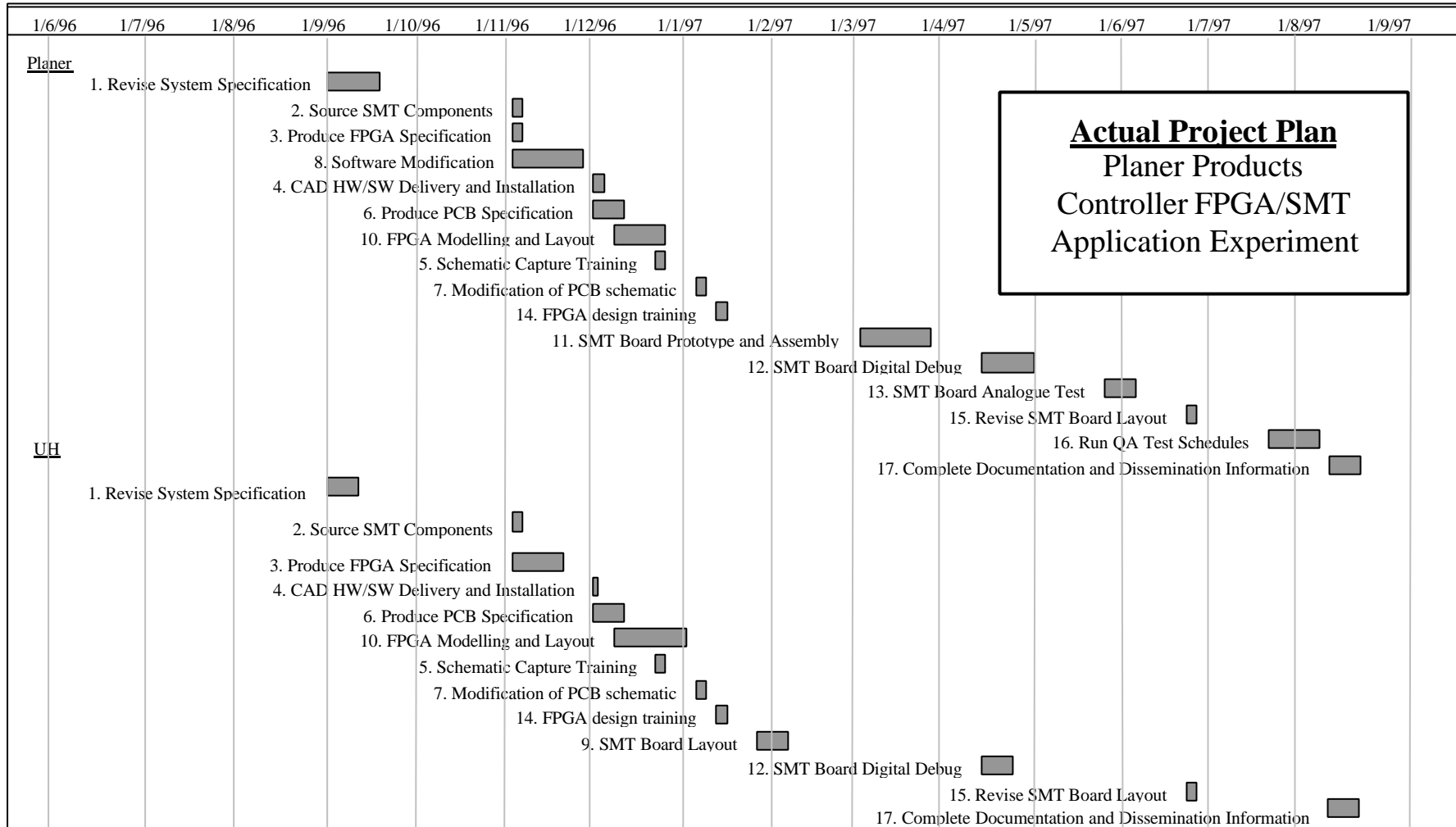
- Engine becomes a proven and validated controller for the entire product range.
- Separation of the MMI decouples the core, performance critical, function (freezer control) from the User Interface which is less critical but more volatile in terms of customer requirements and more likely to require future modification for product differentiation.
- Use of an FPGA and SMT to produce a small Engine allows the control to be physically embedded in the freezer chamber.

9.2 Workplan

Given the change to the strategy, the design process was duly amended to allow for the fact that as the CPU PCB had now changed, the pinout prototype could not be used. The revised strategy was now inherently higher risk as more elements were changing simultaneously. The amended strategy was as follows:

- Specify the design
- Modify the schematics
- Modify the software
- Layout FPGA
- Layout SMT PCB
- Test on SMT PCB
- Rework SMT PCB
- Retest

The overall duration of the plan was increased to 12 months to allow for the 1 to 2 month delay due to the project redefinition, plus some contingency for any further unplanned delays. Once these amendments were made to the design strategy the overall work kept close to the revised plan. The final actual workplan schedule is shown below. The one additional task was the need to revise the board layout after the analogue debug stage.



A full task breakdown is shown below:

Task	Start Date	Duration (Weeks)	Planner Effort (Person days)	Subcon. Cost (kEuros)
0. Start project	1/9/96	0	0	0
1. Revise System Specification <ul style="list-style-type: none"> • Select new microprocessor • Define new display interface • Define new HW/SW interface • Define physical configuration 	2/9/96	9	15	2
<p>Notes: With the announcement by the Microprocessor supplier that they were stopping production of the older style processor, a newer processor had to be chosen. Modification of the HW/SW interface to reduce amount of logic to accommodate FPGA configuration from software PROM.</p>				
2. Source SMT Components	4/11/96	4	5	1
3. Produce FPGA Specification <ul style="list-style-type: none"> • Define I/O, package etc. • Define memory map • Define logical hierarchy • Define register architecture 	4/11/96	5	5	3
<p>Notes: The subcontractor in conjunction with the FU wrote the specifications for the FPGA. Reuse of as much HW/SW from the original product as possible was included. The changed microprocessor was also detailed where this affected the FPGA.</p>				
4. CAD HW/SW Delivery and Installation	2/12/96	3	5	0.5
5. Schematic Capture Training <ul style="list-style-type: none"> • Component library maintenance • Schematic editor • Netlist import & export 	23/12/96	1	5	1
<p>Notes: Training was undertaken on FPGA/ASIC project management, which included, specification, design and debugging with the emphases on 'Top-Down' and 'Right-First Time' techniques</p>				
6. Produce PCB Specification <ul style="list-style-type: none"> • Define physical configuration • Define design rules • Define envelopes, clearances, dissipation etc. • Source SMT component types 	2/12/96	5	10	2
<p>Notes: The subcontractor in conjunction with the FU undertook the specification of the PCB. The PCB supplier in regard to board processing rules provided additional assistance.</p>				
7. Modification of PCB schematic	6/1/97	3	5	1
8. Software Modification <ul style="list-style-type: none"> • Port kernel and code to new CPU • Implement changes to HW interface, memory management etc. • Implement new display drivers • Write/update test code 	4/11/96	6	20	0
<p>Notes: SW modification was the province of the FU, the modifications allowed operations with the FPGA, and to implement the change in the microprocessor used.</p>				
9. SMT Board Layout	27/1/97	5	0	2
10. FPGA Modelling and Layout <ul style="list-style-type: none"> • Code test bench & RTL • Simulate & debug RTL • Synthesise & place & route • Perform timing analysis and post-layout simulation 	9/12/96	5	15	3.5
<p>Notes: Modelling and simulation of FPGA, in parallel to design of PCB layout. Undertaken jointly between FU and subcontractor.</p>				

11. SMT Board Prototype and Assembly	3/3/97	6	20	0
12. SMT Board Digital Debug <ul style="list-style-type: none"> Configure ICE for microprocessor & download for FPGA Debug HW/SW interface 	14/4/97	6	15	2
	Notes: Debugging and verification of FPGA and Microprocessor functionality with PCB design and prototyping.			
13. SMT Board Analogue Test <ul style="list-style-type: none"> Switch to fully populated PCB Static test of analogue I/O On-line test of analogue I/O in full freezer 	26/5/97	4	10	0
	Notes: Prototype of fully populated SMT board was tested to verify the analogue subsystem functionality. The tests were undertaken using an existing test rig which allowed debugging of the pin-outs system.			
14. FPGA design training <ul style="list-style-type: none"> Introduction to VHDL & simulation Synthesis & Fitting Analysis & debug techniques 	13/1/97	2	5	1
	Notes: Use of VHDL and the process to a programmed PROM for the Xilinx XC5200 family was explained.			
15. Revise SMT Board Layout <ul style="list-style-type: none"> Update schematics to incorporate all mods Update layout to match 	23/6/97	4	5	1
	Notes: From results of task 13, modifications and changes were completed on SMT board layout, and all relevant documentation.			
16. Run QA Test Schedules <ul style="list-style-type: none"> According to existing company standards & procedures 	21/7/97	3	15	0
	Notes: A standard MR3 test schedule was run with the new SMT/FPGA – based unit.			
17. Complete Documentation	11/8/97	3	10	2
18. Complete Project	29/8/97	0	0	0
TOTAL EFFORT and COST			165	22

In terms of the cost and resources required, the following variations to the final plan were noted.

	Planned KECU	Actual KECU
Labour	26	31
Durables	2	0.5
3rd party sub-contract	18	22
Services	3	2
Travel	2	0
Consumables	3	3.5
TOTAL	54 k Euros	59 k Euros

10. Subcontractor Information

10.1 Subcontractor 1

Name: University of Hertfordshire

Size: 1700 employees

Business

University, Microelectronics in Business Centre and FUSE TTN

The Subcontractor was able to supply the expertise and experience, as described in the following section, which fitted closely with what Planer was looking for. They were able to provide a direct design support as well as training and support at the very outset of the project addressing such as the following: -

- Technology selection, addressing such issues as cost of ASICs/FPGAs adoption.
- How much of a reduction in PCB real estate should we anticipate? With a goal like PCB size reduction which was critical in terms of a projected manufacturing costs savings per unit.
- The adoption of design methodologies.
- The feasibility of the introduction of both SMT and FPGA/ASIC technology simultaneously.
- What are the technical risks and are they manageable and acceptable?
- Advice on the financial risks manageable.
- What is the likely cost of obtaining suitable knowledge?

Relevant Expertise & Experience

The subcontractor has design tools on both UNIX workstations and PCs covering the full range of technologies from PCB through PLDs and Field-Programmable Gate Arrays (FPGAs) to Masked Gate Arrays, Cell-Based and Full Custom devices as well as Microcontroller-based design. PCB tools cover both through-hole and surface mount design with auto routing. Most of these facilities are completely separate from University teaching facilities and so provide a secure environment where industrial users can gain experience with a wide range of tools and produce their first designs. On the FPGA side Actel, Altera and Xilinx are fully supported with capture in either schematic or VHDL.

The subcontractor was appointed the DTI Regional Electronics Centre for southeast England in 1989 and the DTI Microelectronics in Business (MiB) Eastern Support Centre in 1994. It is an active member of the EURO-PRACTICE scheme and many of its divisions are DTI-registered consultants. The subcontractor has been the UK national Xilinx FPGA training centre for over 5 years, with courses being delivered to over 200 trainees. It has completed over 50 subcontract electronics design projects for companies as well as a further 75 feasibility studies in advanced component technologies.

Services provided

The subcontractor assisted with system- and board-level specification, FPGA specification and design using VHDL, and also SMT component sourcing and PCB layout. It also trained the company in the use of the new schematic tools and FPGA design and debugging.

During the specification phase, there was a lot of interaction between the subcontractor and Planer with all the assumptions underlying the project proposal being questioned once again. This led to the idea of replacing both the existing controllers with the new board. After these consultations and discussions, the subcontractor finalised the specification for Planer's approval.

Once the specification phase was complete, the subcontractor's staff wrote the initial VHDL code for the FPGA device. Subsequent hands-on training of the First User's staff was given on a one-to-one basis, and this centred on the debugging of the FPGA simulation. The subcontractor is also a VHDL training consultant and so had the appropriate training materials to hand. The time spent in the specification phase paid off in that this implementation phase was very rapid (less than 4 weeks).

The subcontractor's SMT expert first worked with the company to identify sources for SMT equivalents of the discrete components that were to remain. This process took about 4 weeks. (The only components that were not available in SMT form were some very high precision resistors used for system self-

calibration). Once component sources were identified and physical package data captured, the subcontractor helped perform schematic editing and component library definition for the new SMT PCB, using a system compatible with that purchased by Planer. This enables Planer to maintain the design in the future. Layout was done on tools owned by the subcontractor, and prototype board fabrication was performed at Planer's established PCB suppliers.

Personnel

The FPGA design consultant trained with Philips Radio Communication Systems and subsequently worked on technology transfer projects for Polyfield Electronics Ltd. and the DTI Regional Electronics Centre. He has designed many PLD; FPGA and Microcontroller based instrumentation systems, a number of which have been exploited commercially.

The SMT PCB consultant has many years experience in advising companies on moving to SMT-based PCB technology and is an expert in SMT PCB design and design for manufacturability. He is currently chairman of the technical committee UK Surface Mount and Related Technology (SMART) industry interest group.

Rationale for choosing / evaluation of the subcontractor

Although not known to the First User before the start of the project, both consultants were introduced via the contact with the TTN, and hence an assessment of capability was made during the early discussions with the personnel from the TTN. Having judged the consultants to be capable of not only performing the design tasks themselves but also of passing on essential expertise to personnel within the First User company. A decision was made to continue work with the chosen subcontractors as they had a very good understanding of the project as a result of earlier discussions.

Contract

As the subcontractor was also the supporting TTN it was agreed that Planer's standard terms and conditions of purchase would apply. However, key to the overall success of the AE was the detailed specification as to what the subcontractor would actually deliver. This agreed specification allowed both parties to understand what the subcontractor would provide.

The following IPR model was used:

- Planer retained all intellectual property rights with respect to any Background (i.e. prior art) and Foreground (i.e. intellectual property arising) aspects of the work that were proprietary to Planer.
- The subcontractor granted a royalty-free non-exclusive license with right of assignment to Planer, with respect to all Background intellectual property of the subcontractor incorporated in the work.
- Ownership of the Foreground aspects of the work which were generic and related to published standards remained with the subcontractor, which granted a royalty-free non-exclusive license with right of assignment to Planer with respect to the same.

11. Barriers perceived by the company in the first use of the AE technology

There were several barriers preventing Planer from immediately using the proposed technology to improve its products and compete more effectively. Although Planer Industrial Division has been involved with companies working with surface mount components, through the supply of hot gas rework equipment, it had never utilised SMT principles in any of its own products. As a result of contact with so many companies involved with SMT, there is certainly an awareness within the company of some of the problems that might be encountered when such new technology is brought into the production environment. Perhaps more significantly, the gaps in understanding of ASIC and FPGA technology were even more profound especially with regard to the essential feasibility of introducing such technology. The combination of the above areas of ignorance represented significant barriers i.e.

- How many ASICs/FPGAs do we need to purchase in one year? With the choice of ASIC or FPGA technologies a critical issues for the selection is the expected sales volumes and associated manufacturing cost, higher cost for FPGA than ASIC per unit verse a higher Non Recurring Engineering (NRE) cost of ASIC, but a lower per unit cost than the FPGA.
- How much of a reduction in PCB real estate should we anticipate? With the adoption of new technology to achieve a goal like PCB size reduction there is a question of how to determine a like reduction in PCB size, so that an economic justification can be made in terms of a projected manufacturing costs per unit.
- What will the impact be on stock volumes and production tooling? Any stock of components represents a tie-up of cash resources, if these components are high value part then this can represents a large investment. This can be critical issue, for example, in the case of ASIC components in which a contract between vendor and customer may require a minimum volume, which can lead to a build-up of stock.
- Is it feasible to introduce both new technologies simultaneously? This is the question of parallel adoption of two complementary technologies, verses the adoption one technology followed by adoption of the other technology at a later date.
- Are the technical risks manageable and acceptable? What are the risks, pitfalls and problem from a technology stand point that can arise from the adoption of either of the two technologies. If there are any issues what is the means to minimise or negate those risks.
- Are the financial risks manageable and acceptable? Similarly are there commercial risks that can arise from the adoption of these technologies, and again what is the answer to the minimisation of the risk.
- Where do we go to get such knowledge?
- What is the likely cost of obtaining suitable knowledge?

12. Strategy / steps taken to overcome barriers and arrive at an improved product

Initial contact with the TTN enabled some of the barriers to be quickly dismantled. We immediately knew that we were talking to engineers and designers who not only knew more than we did but who also understood the requirements of our current designs thus imparting to Planer staff confidence that we could work with the TTN to achieve a successful outcome. The question of having sufficient confidence to take the initial step is a most important barrier to overcome as embarking on a major development such as this needs Board approval within Planer. Technical and financial risks on such a project as described herein would have been unlikely to proceed without a) confidence in the TTN and b) support from FUSE. As many of the perceived barriers were related to correct initial technology selection, and the associated implication to the overall management of the technology adoption, the TTN was able to provide training under FUSE to allow us to make a valid technical selection. Assistance and advice was also forthcoming from the TTN throughout both the initial pre-AE phase and the whole of the experiment.

13. Knowledge and experience acquired

The experiment has gained the first user knowledge in project management, surface mount technology and FPGA design. The First User has gained experience of FPGA design methodologies including schematic capture and layout, FPGA design and in-circuit verification, SMT layout, assembly and test activities.

Knowledge was gained through hands-on training covering schematic capture and component library definition on the new system. The method was also used to cover FPGA design entry and simulation through VHDL, use of the vendor's place and route and timing analysis tools, and techniques for debugging, including post-layout simulation and in-circuit testing and debugging using a download cable.

Knowledge was also gained through close co-operation with the subcontractor, particularly at the specification, component sourcing and debugging stages. Working on the specifications together both gave Planer an understanding of best practice in the relevant areas and ensured they were in overall control of the project.

Planer are now able to specify and design FPGA components and/or SMT boards for use in some of their other products such as hot-gas rework systems and surface profiling systems for the electronics industry. This is what was anticipated at the beginning of the experiment.

14. Lessons learned

One lesson learned from the project is that of the need to be flexible and prepared to make changes in plan during the course of a long running project. In his case it was decided to make changes to the specification so that further benefits could be derived, i.e. by incorporating the designs of MR3 and Kryosave controllers, not just the MR3.

Secondly it was necessary to accommodate changes invoked by Hitachi the manufacturer of the microprocessor component used in the controller. By accommodating such a change the anticipated product life cycle has been considerably extended.

The conclusion is that it is important that when undertaking the expense of a technology change, factors in both the “essential” and “desirable” categories should be incorporated, to maximise the expected life of the revised design. In addition, one must take a creative approach and look at the application of the new technology in the widest terms across a product range, again to maximise the potential benefits.

Otherwise, the company is very pleased with the way the project progressed, and the managing director has said: “The design has far exceeded our expectation... We’ve enhanced performance and quality as well as reducing production costs”.

15. Resulting product, its industrialisation and internal replication

The use of an FPGA has allowed the incorporation of more sophisticated memory management, including a protected memory area. The use of Surface Mount Technology coupled with the implementation of the FPGA has provided a significant reduction in both board size and potential cost of the controller.

However, it can be concluded that the FUSE engine has provided Planer Products with significant advantages, which would have been difficult to achieve through the use of the technologies previously utilised. These are:

- A lower cost core system thus improving competitive advantage,
- A more reliable and robust memory management system,
- A more easily packaged and flexible system giving opportunities for more varied products in the future,
- A smaller overall design footprint giving customer benefit of increased laboratory space.

The final result of the Fuse experiment was the successful creation of a small footprint control PCB, known internally as the FUSE Engine, which is being used within Planer Products' entire controlled temperature product range. This control PCB provides a core three term control (PID), multi-ramp controller, which can be incorporated, with only minor alterations, into a range of freezing and also heating products. As well as a control function the engine provides links to both a man-machine interface and computer/printer.

The required steps for industrialisation are:

- The design and implementation of a distribution PCB, to allow the engine to be incorporated into specific products. The PCB provides for connections to the outside world and enables appropriate mounting points. At this point EMC testing will be assessed internally or implemented externally, as appropriate, to enable compliance with CE Mark regulations.
- Modification of the firmware to include commercially required features that have evolved since the original specification was established and to correct minor bugs found during prototype testing.
- A range of production engineering/procurement functions including the updating of bills of materials, correction of minor PCB errors and liaison with the SMT PCB manufacturers for production quantities.

The work carried out under this Application Experiment was sufficient to get the new surface mount PCB through prototype testing. Additional work was needed, as outlined below, to get the product into production and into the market place.

Task Description	In-house / External	FU Effort (Pers-Days)	Cost (K Euros)
Prototype testing	IN	8	1.15
Field testing	IN	8	1.15
Mechanical Design	IN	3	0.43
Industrial Design	External		1.15
Manufacture Prototype	IN	3	0.43
PCB's Design	IN	4	0.57
PCBs Manufacture Prototypes	External		2.30
Manufacture Miscellaneous parts	External		2.30
Manufacture Base	External		2.01
Electrical Design	IN	6	0.86
Freezer wiring	IN	3	0.43
Procure components	IN	18	2.58
Firmware design & Implementation	IN	10	1.44
New UART Modules	IN	4	0.57
Print modules	IN	5	0.72
Low level debug	IN	4	0.57
PC software implementation	IN	12	1.72
Formal validation	IN	2	0.29
Assembly drawings and BOMs	IN	8	1.15
System Integration	IN	3	0.43
Initial test and debug	IN	5	0.72
Formal validation	IN	6	0.86
Approval	IN	2	0.29
User Guide	IN	8	1.15
Draft manual excluding images	External		1.15
Incorporation of final images	External		0.57
Proof Read and rework	IN	2	0.29
CE Marking	IN	4	0.57
EMC Tests	External		1.15
LVD Tests	External		0.86
Release	IN	1	0.14
Total		159	30

The complete industrialisation phase from the completion of the AE in August 1997 to the launch of the new product in July 1999 will have taken approximately 22 months. This is longer than normal for a product of this complexity, but delays were caused by pressures from other projects within the Company. Small Engineering departments within SMEs face a constant battle of balancing the needs of existing products in the field, which need improving and updating to comply with current legislation etc., and the needs of new products coming on-stream.

The total cost of industrialisation is estimated to be of the order of 30 K Euros. The product will be managed in the same way as others within the Biomed Division that it replaces. I.e. PCBs will be manufactured external to the Company and will be assembled and tested before delivery to Planer. System assembly will take place within the Company, which utilises unit-cell assembly techniques to facilitate short delivery times to the customer. Maintenance is carried out by changing modules and returning to the factory, or approved service centres. This service is undertaken by trained personnel resident within the distributors in over 40 countries world-wide.

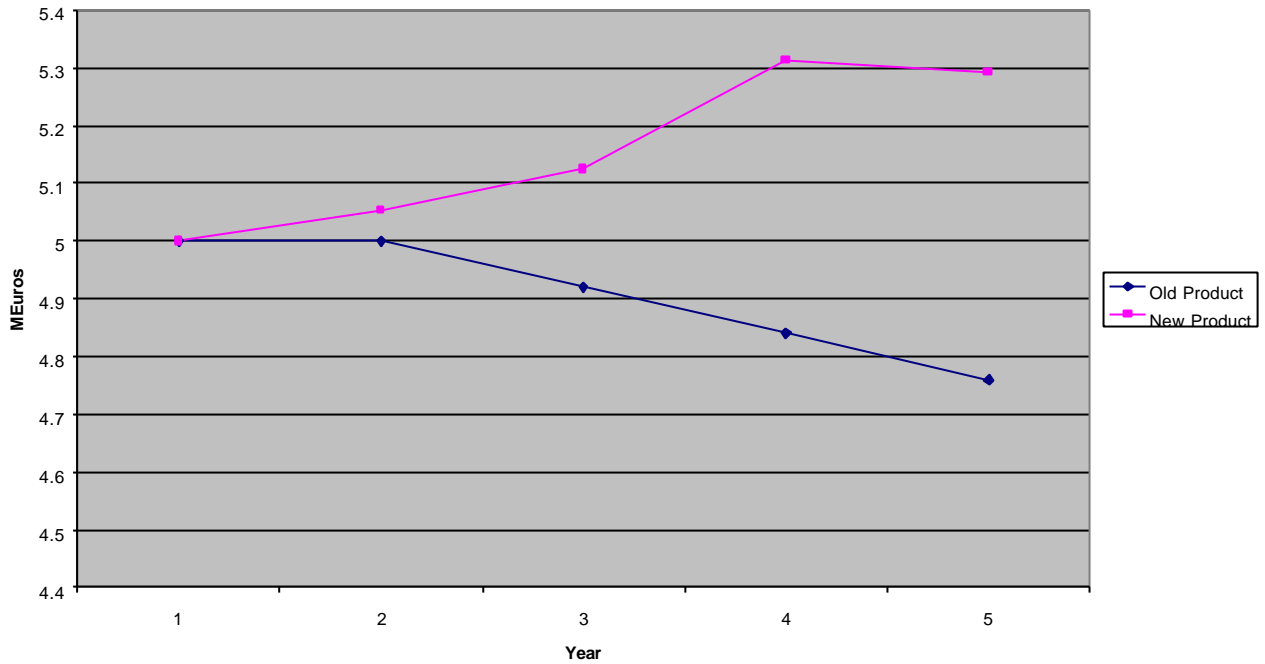
Plans are already in place to enable the new FPGA based product to seamlessly replace existing products as stocks diminish. Other products require the development of an appropriate man-machine interface, which has been specified and is in hand. Plans for future products that will incorporate the new PCB are already being established at the strategic level and will be detailed within the next four to six months.

The schematic capture tools have already been used to good effect on a product involving the control of solenoid valves, and are currently being used for the design of the distribution PCB that is necessary for the commercial exploitation of the FUSE Engine. The FPGA design experience has not yet been used on other products but will allow Planer Products to review each new design with sufficient experience to assess the virtues of replacing multiple discrete devices with an FPGA or other type of programmable logic device.

16. Economic impact and improvement in competitive position

By reducing size and hence manufacturing costs it is anticipated that significant inroads into the bone-marrow, animal and biological markets will be made primarily at the expense of current competition from the US and Japan. At the time of writing this report such savings had not been fully established as the new freezer product was not fully into production, but signs are that savings in production costs will enable products to achieve the stated ambitions. The creation of a hybrid system makes a comparison between the current product, the MR3 controller, and the result of the FUSE project difficult, as there is no longer a one to one relationship between the designs.

Sales for Old and New Products for the First Five Years in Million Euros



However, the following table gives a guide to how well the use of SMT and the FPGA has met the requirements. The MR3 IO board has been ignored in comparisons as this is mainly involved in printing and display activities and removing it from comparisons reflects the removal of the Man Machine Interface (MMI); the resulting comparisons are therefore conservative in nature.

Table of Projected Improvements

Description	MR3 System	FUSE Engine	Improvement
Size of system	CPU PCB + Analogue PCB = 327 cm ²	180 cm ²	45% reduction in size
Number of PCBs	2	1	50% reduction in quantity
Suitable for physically embedding in chamber	No	Yes	100% improvement
Complex enclosure required	Yes @ 100 Euros	No @ 50 Euros	49% reduction in cost
Major chip count	27	24 (with just RAM and EPROM as MR3)	11% reduction in chip count
Material Cost	260 Euros	230 Euros	12% reduction in material cost
Future Enclosure Material Savings*	227 Euros	0 Euros	227 Euros reduction in material cost
Future Enclosure Labour Savings*	245 Euros	0 Euros	0 Euros reduction in labour cost

* Future savings estimated – requires manufacturing changes beyond scope of this project.

Anticipated changes in market share over a five-year period, as a result of incorporating FUSE Engine into complete range of new products are illustrated in the graphs below for each of the four markets discussed. Increase in sales equates to approximately 780k Euros over a five-year period. Payback time of the FUSE investment is 18 months. Estimated product lifetime is approximately six years, however the Return on Investment (ROI) is determined to be 350% over the initial five years of the life of the product. The competitive position will be significantly improved if the FUSE Engine is fully incorporated into all Planer freezer products, since this will offer a complete range of products to the customer at a variety of price and performance levels.

17. Summary of best practice and target audience for dissemination throughout Europe

This experiment has demonstrated:

- A comprehensive review of a product range to assess the widest applicability of new technology
- A rational approach to technology choice, including life cycle and future-proofing considerations
- A thorough specification process, including partitioning of tasks between the microprocessor software, the FPGA and the remainder of the circuitry
- Appropriate choice of design methods: with schematic capture at board level and VHDL as the method of entry for the FPGA.
- Choice and use of subcontract effort in a mode which empowers the company for future development
- A thorough planning process, involving the subcontractor in a collaborative fashion

The target audience for this AE could be any SME with predominantly analogue or discrete component design experience, particularly in the fields of medical electronics, instrumentation or process control.

Target audience industries: Precision Instruments (Prodcom 33)

Subdivision: Precision Instruments medical (Prodcom 3310) and non-medical (Prodcom 3320)