

**FUSE demonstrator document
FUSE Application Experiment No. 2021**

Monitoring TTN: IAM F&E GmbH, Braunschweig, Germany

Introduction of latest technologies for automatic board testing, IEEE 1149.1

Abstract

DVS Digital Video Systems designs, manufactures and markets digital video interface and storage systems ranging from standard TV up to HDTV (high definition television). A new board is designed and developed which contains all modifications for JTAG boundary scan test. This test procedure is standardized by the IEEE by the Joint Test Access Group (JTAG) and is also named boundary scan test. The test procedure is implemented with a simple serial bus (JTAG bus) which is distributed between all JTAG testable components. The core logic for testing is realized internally in the chips and allows the access to all IO pins via dedicated shift registers. The board is part of the ProntoVideo digital video disk recorder developed and manufactured by DVS. The reason for JTAG test is that for complex and high density electronic boards an analysis of errors (soldering errors for example) by hand costs a lot of time and is very expensive. Testing the board via JTAG allows a quick location of errors and reduce the manufacturing time drastically.

The project had a duration of 12 months and cost 72 KECU. The payback period is about 2 years, the product lifetime is 4 years, the ROI is 300 %.

As target audience all companies are relevant which develop products in the areas "electronic engineering", "multimedia systems" or "audiovisual electronics".

1. Company name and address

DVS GmbH, Digital Video Systems
Krepenstrasse 8
D-30165 Hannover
Germany

2. Company size

Number of employees is 20 with 7 involved in research and development.

3. Company business description

DVS Digital Video Systems designs, manufactures and markets digital video interface and storage systems ranging from standard TV with sampling rates of 13.5 MHz up to HDTV (high definition television) with sampling rates up to 74.25 MHz. The systems can be separated into two groups: **RAM based storage systems** and **disk based storage systems**. In RAM based storage systems the digital video data is stored in large arrays of DRAM (up to 4 Gbyte) while in disk based systems the data is stored in large arrays of harddisks (24 harddisks for example).

DVS designs the hardware and the software internally. The products are manufactured internally.

All systems are mounted in standard 19-inch chassis or in PC-compatible chassis. The systems are delivered as complete subsystems including power-supplies, harddisk arrays, cooling and

so on. Typically the systems are connected to a host computer by the customer via SCSI or Ethernet. These links are also used to control DVS systems.

All systems consist of hardware and software. The software contains a powerful graphical user interface which runs on the host computer and allows the user a very easy control of DVS systems.

Some examples of DVS systems are:

- SCSI/Video: Realtime Video IO interface via SCSI bus using M-JPEG compression
- ISP500: Image sequence storage and processing system
- ProntoVideo: Digital Video disk recorder

4. Company markets and competitive position at the start of the AE

DVS systems are used for two application areas:

- Research and development
- TV studios and video production companies

For research and development RAM based systems are used. These systems have video interfaces with complete programmable video time base generators, high data rates and a number of video channels running in parallel. Application areas are for example the simulation of video processing hardware and software and the emulation of video processing ASICs via dedicated digital data links which can be connected to some user hardware.

For TV studio applications the disk based systems are used. In this application area a long playing time ranging up to 1 hour and more is important. Also additional IO interfaces are necessary for record and playback of digital audio signals and time code information. Application areas for this kind of systems are video post production, storage of computer generated digital video sequences, computer animation, TV studio broadcasting, medical imaging and so on.

The company DVS exists for 12 years. RAM based systems are manufactured since that time while disk based systems are built for 3 years.

All DVS systems are sold worldwide in the USA, in Japan, Taiwan, Korea and in Europe. For disk based systems DVS holds a market share of about 10 % while for RAM based systems the market share is about 50 % worldwide.

Competitors for RAM-based systems are the US company Viewgraphics Inc. For disk based systems there are a number of competitors like Accom, Abekas, Sierra Design, Hewlett Packard, Tektronix and so on. Costs of components and complete systems are in a range of several thousand ECU to a few hundred thousand ECU.

All companies use the same basic technology. Features, performance, reliability and costs of the product are important aspects, considered by customers. Especially a small company, competing with larger, well-known companies, has to supply leading edge technology with high reliability, but costs must not be higher than competing products.

5. Product to be improved and its industrial sector

5.1 Product Description

The product to be improved is the ProntoVideo digital video disk recorder.

This product is a system to record and display digital video sequences in realtime. The system can be connected to a host computer via SCSI (Small Computer System Interface) or Ethernet IO links. The Digital Video Data is stored on large arrays of harddisks. A powerful graphical user interface (GUI) allows an easy to use user control of the system. The system provides all necessary IO signal connections to be easily integrated into a digital TV studio environment. Figure 1 shows a photograph of the Pronto Video disk recorder.

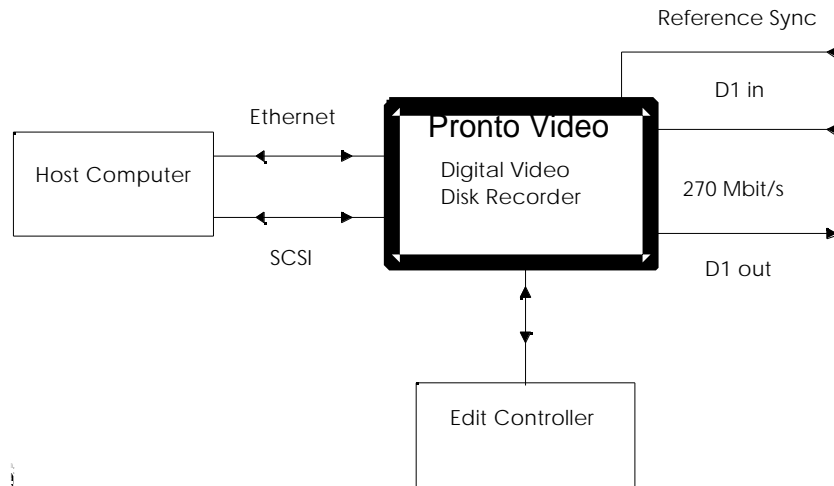


Figure 1:
ProntoVideo digital
Disk recorder

5.2 Application Area

The ProntoVideo digital video disk recorder can be classified into the following industrial sectors:

EE: Electrical engineering and related technical consultancy

IA: Audiovisual consumer electronics

IC: Electronic components

IE: Electronic engineering and related technical consultancy

Figure 2 shows how the ProntoVideo disk recorder is embedded in a typical application environment at the customer.

Figure 2: ProntoVideo digital video disk recorder in a typical application environment

For video IO signal connection a video input and a video output connector are provided. These interfaces are serial digital IO links according to the standard SMPTE259M with a data rate of 270 Mbit/s transmitted via a 75 Ohm Coax cable. The host computer is connected via a Fast or Ultra SCSI link or via Ethernet. Via these links the disk recorder can be controlled (for example starting at display at frame number X). For a simple and easy to use user interface a powerful GUI (graphical user interface) is provided. Unix based workstations (Sun, Hewlett Packard or Silicon Graphics) and PC based host computers (WindowsNT) are supported. The SCSI and/or Ethernet connection is also used to download computer generated video sequences to the disk array of the Pronto and to display these sequences in realtime after that.

Another possibility for controlling the system is the so-called **stand-alone mode**. In this case a separate control channel realized as a RS422 channel is used. The disk recorder emulates a VTR (video tape recorder) in this case. An Edit controller can be connected to the RS422 link and the user can control the operation of the disk recorder via the Edit controller including special effects like Jog/Shuttle mode or fast motion and so on.

The Sync input named Reference sync allows the synchronization of the video output to an analog studio sync. This is important for TV studio applications.

5.3 Testing of the ProntoVideo Hardware

The ProntoVideo contains the following hardware components: a number of harddisk drives, a DRAM, a local 68040 processor, a number of SCSI processors, hardware building blocks for video interfacing and so on. All electronic components with the exception of harddisks and power supplies and so on are mounted on a single multi layer board with 8 layers and with a

high packing density. A number of chips which have a fine pitch package are mounted on this board. The minimum distance between two pins is 0.5 mm. The board has been designed, layouted and tested at DVS. The production of the board and the assembly and soldering of components are done outside. The boards are delivered by the outside companies and tested by DVS. Testing means:

1. Visual inspection of the board
2. Connection of power supply and check if the processor boots
3. starting special test programs like memory test
4. connection of two Prontos with Video-IN going to Video-Out, start a display at Pronto A, a record at Pronto B and compare the data of Pronto B.

The test No. 4 can only be performed if tests 1.. 3 did not show any errors of course. A severe problem arises if test 2 is not OK and the processor does not boot due to a fatal hardware error (short circuit or missing interconnection for the DRAM for example). In this case the following steps are done:

- Additional visual inspection of the board and trying to find out soldering errors
- Connect a logic analyzer and trying to find out whats going wrong

During the last 3 years we have commissioned several subcontractors who assemble and solder the electronic boards. We have got the following experiences:

- The level of quality of the produced boards was independent of the subcontractor
- A lot of boards which are delivered contain errors:
 - Wrong placements of digital components
 - Visible and invisible bridges between pins (soldering error)
 - Visible and invisible bridges between lines (PCB error)
 - Broken lines (PCB error)
 - Unconnected pins (soldering error)
 - Placement of defective digital components
 - Missing placement of passive components

The most errors are mainly located at IC packages with fine pitch pins

- It costs about 3 hours up to 5 days for a technician and/or engineer to find out fatal hardware bugs in the digital part of the PCB depending on the severity of the error. Errors in the analog part can be found reasonably fast.

- Even if a system seems to work perfectly it could be that there are hidden errors. Imagine for example a short circuit between a dynamic signal and a static signal. In this case it could be that you get the correct level in 99,999 % of all cases. In the rest the signal is a little bit disturbed (not a clear High or clear Low) and could produce one error every 24 hours.

These are the reasons why additional tests must be done with the boards to find out errors more quickly, to increase the level of quality and to reduce the costs.

6. Description of technical product improvements

The improved product is named ClipStation PRO.

For the new product the following improvements have been implemented:

- A. Use a Pentium-based PC motherboard instead of the 68040 local processor
- B. Use the PCI bus as the interconnecting bus between the new board and the processor

C. Implement an **advanced test method** for automatic board testing

The first and second aspects are only changes to the architecture of the board. DVS has a lot of experience in the design of PCI bus interfaces. So this is not a problem. The third aspect is the main topic of this project. As will be shown in the next chapter the JTAG (Joint Test Action Group) boundary scan test architecture is the suitable technology for our application. This test procedure is implemented with a very simple serial bus with 4 (sometimes 5) signals (the JTAG bus) and is standardized by the IEEE as IEEE1149.1. For more detailed information see the Technical report to this project or the JTAG standard.

To implement and to execute the JTAGTEST procedure the following steps are necessary:

- Connect all JTAG testable components together in a serial mode
- Implement a small flat cable connector (10-pin for example) which carries the JTAG bus signals. Connect this 10-pin-connector to a PC (usually with an adapter for the printer port of the PC). On the PC a suitable JTAG test software is installed.
- Via the JTAG bus (nearly) all IO signals of all chips which support the JTAG can be accessed. With the software running on the test PC a number of test patterns (stimuli) can be generated automatically. These test patterns are shifted down to the JTAG bus and generate High or Low levels on all IO pins which are JTAG testable. Short circuits or missing interconnections can be found out by generating a High or Low at IC A, Pin x and monitoring the signal at IC B, Pin y.
- With this test not only board errors but also defect components with stuck-at-one or stuck-at-zero errors can be found because the serial shift registers cells internally in the chips are connected directly to the IO drivers of the chip. Also bonding errors can be detected with the JTAG test.

Of course not all chips support JTAG (FIFO chips for example do not). These components are called "clusters" in the JTAG terminology and can be tested via JTAG by looking at signal levels at the input and output of the cluster. This JTAG test architecture has been implemented for the new board.

In the following some more technical information about the new board is given. This can only be done on a block diagram basis. Detailed technical information is confidential and can be found in the technical report. A photography of the new board is shown in figure 3.

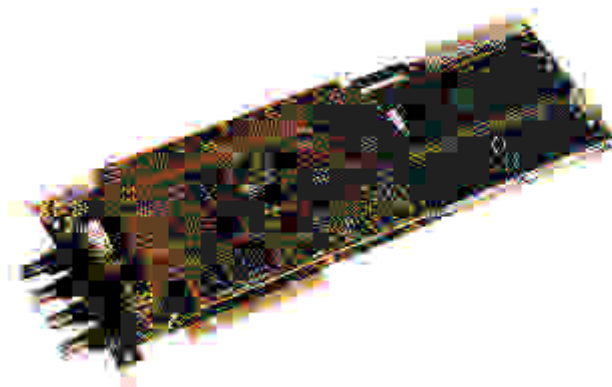


Figure 3: photography of the new board

The new board contains a lot of electronic components which can be divided into 3 groups:

- Programmable devices
- Dedicated VLSI devices
- Analog components

The following EPLDs/FPGAs are used as programmable components:

- AMD MACH EPLDs: MACH211SP, MACH446, MACH466
- XILINX FPGA: XC4010E-2

The following hardware components support JTAG testability:

- MACH EPLDs
- The DEC PCI-to-PCI-bridge 21150
- the Xilinx FPGA
- the PMC module (if present) (PMC = PCI Mezzanine Card, expansion)
- the RAID module (expansion)

Figure 4 shows the hardware implementation of the JTAG boundary scan chain. All JTAG testable devices are arranged in a chain. The JTAG interface has two primary sources:

- a 10-pin flat cable connector which carries the JTAG serial bus signals and which is connected to a JTAG test station with boundary scan software
- the JTAG bus embedded in the PCI primary bus which is driven by logic on the PC motherboard. With this option complete system test using JTAG is possible.

The JTAG controller consists of a small EPLD which routes the signals to its appropriate destinations. The following hardware components are JTAG testable:

- the primary PCI bus
- the secondary PCI bus
- the AMCC local bus (partially)
- the video interface (partially)

For the preparation of the boundary scan test of the board using a PC connected to the 10-pin flat cable connector the following working steps must be done:

A) Generate the **EDIF netlist** (Electronic Design Interface Format) of the board which is a netlist of all components including passive components like test points, pull up resistors, power connectors and so on.

B) Manipulate the EDIF in a suitable form so that the JTAG test software which runs on the Test PC can interpret this file.

C) Collect all **BSDL files** (Boundary Scan Description language) for all JTAG testable components. The BSDL files describe the behavior of all JTAG testable components if they are accessed via JTAG. These files are supplied by the semiconductor Manufacture and can usually be downloaded from the web.

D) Edit 4-5 intermediate files to "tell" the software which components are passive for example and cannot be accessed via JTAG (for details see also the Technical report).

E) After all files have been edited properly run the JTAG test software and interpret the results.

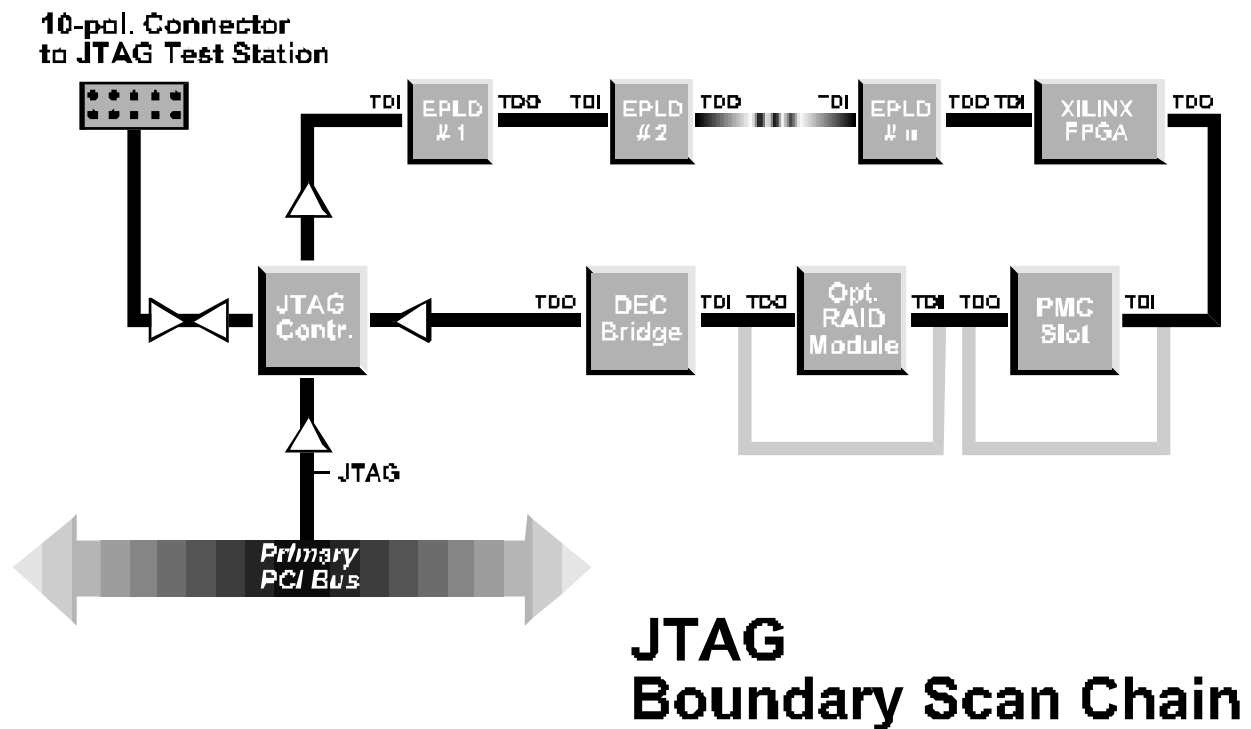


Figure 4: Implementation of the JTAG chain for the new board

7. Choices and rationale for the selected technologies, tools and methodologies

As was explained in the previous chapter the JTAG boundary scan test architecture was implemented for the new board. Of course there are other test methods available like:

- Use of a bed of nail adapter and test every board on a dedicated test station (TeraDyne or GenRad)
- Use of a flying probe test adapter

These test methods are not applicable for our boards because they are too expensive and/or require a lot of additional board space for test points which is not available. They only make sense for high volumes (10000 boards per year for example). Also the programming of the test adapters is a very difficult task and requires a lot of time including mechanical work for the testing nails and so on.

Compared to these test methods the JTAG test architecture requires only an easy to implement serial bus and a PC as a test station. Because more and more semiconductor manufacturer support JTAG with their chips the JTAG test standard will become more and more important in the future. Note for example that for new chip packages like BGA (ball grid array) packages an optical inspection of soldering is impossible. In these cases the JTAG testability is a must to get good boards.

8. Expertise and Experience of the company

DVS has about 12 years of experience in the design and development of complex electronic systems. The experience ranges from the design of high speed digital systems with clock frequencies up to 66 MHz to the design of sophisticated analog electronic (filter, PLL etc.) for video interfacing. For the design of programmable logic powerful design tools like ABEL 6.3 are used. DVS has experience in EPLD design (AMD Mach devices in this case) and FPGA design (XILINX).

DVS has also experience in the development of multilayer PCB. The layout is done by ourselves.

Then the multilayer PCB is produced outside. The assembly and soldering of the PCB was done by DVS itself 5 years ago. Due to the miniaturization of components like surface mounted devices (SMD) the assembly and soldering cannot be done by DVS today. For this work soldering machines must be used and this is done by subcontractors.

For software development a lot of experience has been gained for SCSI or Ethernet links to UNIX workstations or PC based platforms running under WindowsNT.

At the moment 3 engineers and 2 technicians are allocated for the production of the ProntoVideo disk recorders. The JTAG boundary scan architecture is completely new at DVS and has not been used before.

9. Workplan and rationale

The workplan for the project including all necessary steps is shown below. The project started in November 1996 and ended in October 1997. A delay of three months before the beginning of the layout must be taken into account because some semiconductor components (M-JPEG compression processor CL560 by C-Cube MicroSystems and ALTERA FX780 EPLD) were discontinued. This required some reorganization of the hardware of the new board and has nothing to do with the main scope (improved testability) of this project.

All working steps which are related to the JTAG boundary scan test have been taken with support of the **subcontractor Synatron GmbH**. Synatron also provides the software named JTAGTEST which runs on the test PC and which contains also the hardware adapter from the printer port of the test PC to the 10-pin connector on the board.

The key phases for the project can be defined as follows:

- Training course: Introduction to boundary scan test procedures and overview on all related topics (Subcontractor + DVS).
- Design, development and evaluation of a test board in cooperation with the subcontractor to learn JTAG boundary scan test methodologies and to get some design rules for the JTAG serial bus interconnection for the final board.
- Hardware design: specification of the block diagram, generation of the circuit diagrams and the netlist, layout of the board and production of 3 prototypes
- Software design: Generation of all software modules or modification of existing ones and adaptation to the new board (DVS)
- Production of three fully equipped prototypes (DVS)
- Testing of prototypes: JTAG boundary scan test and functional tests (DV, subcontractor)

A maximum of four persons were engaged with the project: 3 engineers and 1 technician (for the layout). Due to the discontinuance of some components an additional delay occurred before the layout began. This required additional development time for the hardware design (reorganization of the architecture of the board). That is the reason why more time for the hardware development was needed compared to the amount which was scheduled at the beginning of the project.

For the outhouse production of the 3 prototypes two companies were involved:

- the company Würth for printed circuit board production
- the company Printronic for assembly and soldering

The board is a standard PCI board with large form factor. It is a multilayer board with 8 layers and a lot of chips with PQFP packages (plastic quad flat packages) with 0.5 mm distance between two pins. There are about 2800 interconnections on the board. The placement of components and layout of the printed circuit board are done by hand by a DVS expert. Detailed technical information concerning the board can be found in the technical report.

The time which was needed for project management, writing of reports and so on was about 20 labor days.

The costs for the project can be separated into three groups:

- Labor cost for First User: 33.5 kECU
- Cost for subcontractor Synatron for training course and technical support: 11.0 kECU
- Other costs for production of three prototype boards: 16.5 kECU

An overview of the amount of effort for each task is shown in the following table.

WP ⁴	Task	Done by		Amount of effort	
		FU ¹	SC ²	Planned	Actual
1	Task 1: project management	x		9	19
	Task 2: Dissemination	x			2
	Task 3: Reporting	x			28
2	Task 1: Functional specification of system	x		17	25
3	Task 4: design training	x	x	17	10
	Task 5: evaluation training	x	x		9
4	Task 1: system level design	x		68	35
	Task 2: subsystem level design	x			39
5	Task 1: prototype production	x		34	20
	Task 2: test set-up	x			8
	Task 3: functional testing	x			10
	Task 4: prototype testing	x			9

¹FU: First User

²SC: subcontractor

³in person-days

⁴WP: Workpackage

⁵Deviations: redesign because of unavailability of some parts
voluminous writing of articles

10. Subcontractor information

The company Synatron GmbH was chosen as a subcontractor for this project. The test equipment of this company is based on Personal Computer and the support is available in Germany. (Test equipment from other companies e. g. Hewlett Packard is also available. This test equipment is based on Workstations and isn't useable for a small company like DVS.)

Name and address of the company are:

Synatron GmbH
Lilienthalstrasse 21
85399 Hallbergmoos
Germany

This company has a 5-year experience with JTAG boundary scan test hardware and software. It is the European distributor for the JTAGTEST software package developed by the company JTAG Technologies (Netherlands). Synatron offers training courses concerning this new technology and technical support during and after the design phase of the new board. All

technical questions and problems concerning JTAG which arised during the project life time are discussed and solved in cooperation with Synatron.

Because the JTAGTEST software is very complex and there are a lot of possible errors and misunderstandings in using the JTAGTEST software tools this support is essentially necessary.

The main responsibilities of the subcontractor were:

- introduction to the theory of operation of JTAG boundary scan
- evaluation of the JTAGTEST software using the test board (error diagnostics and so on)
- design rules for implementing the JTAG serial bus on the new board
- technical support during the generation of test patterns (proper manipulation of all files like EDIF)

11. Barriers perceived by the company in the first use of the proposed technology

There were three barriers that have prevented the company from using the new technology for their products:

A) Financial barriers

The JTAG boundary scan exists since 5 years. The hardware costs to implement this new technology are very low as has been explained before. This is not a problem. The problem was the cost for the complex JTAGTEST software. The costs for this software were in the order of 80.000 DM for a complete package with all testing options a few years ago. This investment is much too high for a small company like DVS. Only during the last 3 years the costs for the JTAGTEST software are reduced drastically so that investments in this new technology became reasonable.

B) Technical barriers

About 5 years ago we do not have such kind of problems like soldering errors on the board because for low density packages like DIL packages (Dual Inline) the probability of soldering errors could be held very low. If there are errors they could easily be detected by visual inspection. So it was not necessary to think over advanced board testing procedures like JTAG. As high-package density chips with high pin counts and small pin distances became the standard for electronic design more and more problems with soldering and/or printed circuit board errors arised in the past.

C) Psychological barriers

DVS has always implemented new technologies for their product by the method "learning-by-doing" (for example EPLD or FPGA design). In these cases this was a good method because a lot of experience could be gained by learning from own errors. The JTAGTEST implementation is too complex and it would have required too much time and money to adopt this new technology by the "learning-by-doing" method.

12. Steps taken to overcome barriers and to arrive at an improved product

The following steps have been taken to overcome the above mentioned barriers:

A)

Discussion of the main scope of this project (testability) with the TTN during the planning phase of the project. The TTN (IAM in Braunschweig, Germany) also has a lot of experience in testing electronic components..

B) Training course held by Syntatron

During a one-day training course an introduction to the theory of operation for JTAG boundary scan has been given. Practical demonstrations also showed the usage of the JTAGTEST software. A complete working flow for JTAG test by starting at the netlist and ending at the terminal message "No Errors found" has been exercised by using the test board explained below. The proper manipulation and preparation of all files which are input to JTAGTEST have been learned.

C)

Design and development of a small test board which contains some JTAG testable components. With the test board errors (short circuits or missing interconnections) could be simulated with jumpers. The JTAG test software has been started and it has been verified that all these "hand produced" errors can be located correctly. With this test board a lot of experience has been gained in using this new technology. Also some design rules in designing the JTAG serial bus on the final board were dedicated from the design and the evaluation of the test board

13. Knowledge and experience acquired

- Implementation of the JTAG serial bus on the board including the 10-pin connector
- Handling and manipulation of all necessary design files which are input for JTAG test software which runs on the test PC.

The first step must be considered during the hardware design phase of the board. This step requires the selection of components which support JTAG and the internal organization of the JTAG bus. This is done with a simple EPLD called "JTAG controller" which distributes the JTAG signals to all necessary components and which is also used for download of incircuit-programmable EPLDs and/or FPGAs (also down via the JTAG serial bus). Technical Details are not given here but shown in the technical report.

The second step is the main problem for preparing a JTAG test. The main working steps are already described:

- Generation of EDIF netlist
- Collection of BSDL files
- Manipulation of additional files which describe the board and its components
- A deep insight into the theory of operation of the JTAG boundary scan test architecture. This is necessary to interpret test results correctly.
- Design methodology for JTAG boundary scan testable boards
- Handling and proper preparation of all necessary files which describe the board and all components on it in detail (EDIF files, NIF files (net information file)) and so on
- Usage of the complex JTAG test software supplied by Synatron.
- Correct interpretation of test results.
- Preparation of a PC test station for board test. This is necessary because it is planned to run the JTAG test "in place" at the company which is assembling and soldering the boards. This leads to a higher level of quality measure and enables DVS to refuse the acceptance of boards on which the JTAG test fails.

14. Lessons learned

Main problems which have been encountered were:

- Manipulation of the EDIF netlist is a little bit cumbersome because the files are very large, contain a lot of "dummy" information and have a complex syntax.
- The BSDL files supplied by the semiconductor manufacturers contain a lot of errors (missing pins for example). We don't know why this is the case but that's the experience we made during the project. The semiconductor manufacturers have been contacted and we asked for new corrected versions of BSDLS. In some cases we were able to correct these errors by ourselves by careful analyzing the BSDLS.

A lot of time (about 3 months) was spent before the JTAG test software produces the message "No Errors found" on the terminal.

The following advises for the newcomer can be given:

- If it is possible do not use EDIF netlist files because they are difficult to handle.
- If the user collects BSDL files from semiconductor manufacturers, he/she should ask if these files are correct and have been tested. If this is not the case he/she should ask for error free BSDL files. Otherwise a lot of time is spent for BSDL file debugging.

15. Resulting product, its industrialization and internal replication

The JTAG test is implemented **in-house** at the company who assembles and solders the boards (JTAG boundary scan test station). The hardware costs for this test station are very low. Only a simple PC is necessary with a printer port. The rest is software and all the board description files provided by DVS. This enables some kind of **quality measure** for the board and the soldering. If the JTAG test fails the board is refused to be accepted and it is the responsibility of the assembly and soldering company to solve the problem.

At the moment the assembly and soldering company deliver boards to their customers **without** any electronic test after soldering (only the unmounted boards are tested electronically by the printed circuit board supplier).

75 boards have been produced and tested with JTAG outside DVS.

The boards have been tested by DVS again. A board error statistic is given:

- 52 Boards were error free
- 12 Boards had soldering errors of SMD RLC components located in the "analog" part of the board and not not detectable by JTAG boundary scan
- 10 Boards had soldering errors in some components located in the memory part (DRAM) of the board.

These errors are currently not detectable by JTAG Boundary Scan but will be detectable in the future.

These error were found with an additional DRAM test program

- 1 Board contained a defective component.

It is also planned to create a cluster test for the DRAM. This can be done when some devices near to the DRAM are replaced against new devices with JTAG feature. These devices are not available at present.

The JTAG test is implemented for other **new boards** to be developed at DVS. All the experiences which have been gained during this project could also be used for new projects. We also hope that the required time to implement the JTAG test for a new project could be drastically reduced due to the knowledge gained during the FUSE project.

16. Economic impact and improvement in competitive position

The competitive improvements for the new product can be classified into two areas:

A) Increased sales

The JTAG test reduces the "debugging" time used for locating errors drastically. In the past we have had the situation that a number of customer orders for systems are available. But these systems could not be delivered to the customers because the boards contain errors. With the JTAG test it is expected that the time required for testing and debugging can be reduced drastically (shorter time-to-market for manufacturing the product).

Another important aspect concerning sales is the possibility of the board for **future expansions**. Here a lot of things have been taken into consideration. Only a few of them are mentioned here. As can be seen in the technical report the board has a lot of expansion capabilities like RGB disk recorder, HDTV disk recorder, RAID extension and so on. All these capabilities dramatically influence the market chances of the new product. Because the product is located in a multimedia electronic business market which is rapidly changing from year to year or even from month to month a look into the future and an estimate about the future market share is extremely difficult or nearly impossible.

All the above mentioned aspects are only technical nature from an application point of view and have nothing to do with the scope of the FUSE project. Nevertheless they influence the market chances of the product dramatically.

B) Cost reduction

This aspect is mainly covered by the FUSE project and its main topic (improved testability). The cost reduction and the return-of-investment can be computed as follows:

At the moment (August 1997) DVS produces about 150 boards and/or systems per year. The average time to locate and repair faults is about 15 hours per board. Only 50 % of the boards which are delivered by the outside companies are error-free. The average labor cost (engineer and technician) is 53 DM.

This means the following costs for boards without JTAG:

- Number of boards per year : 150
- Number of boards which contain errors: 50 %
- Average time to locate errors: 15 hours
- Hourly personnel rate: 53 DM
- Total costs per year for testing **without** JTAG: 59.625 DM

To compute the reduced test costs for the new board another important aspect must be taken into consideration. It is planned to prepare a test PC for the outside companies who assemble and solder the boards. They should run the JTAG test **in-house**. Every board which shows errors during the JTAG test is refused to be accepted by DVS. It is the responsibility of the company (and **not** DVS) to find out and repair the errors. Of course not **every** board error could be found with the JTAG test (see the above mentioned considerations about JTAG "coverage").

So a realistic number of 20 % of all boards is assumed which contain errors but which are **not locatable** by JTAG test. These 20 % of the boards are delivered to DVS and must be debugged by using the "old" test procedures (logic analyzer or oscilloscope). If it is assumed that most of these errors are much simpler to locate and debug (for example errors in the analog circuits of the board) it is also realistic to assume a (reduced) time of 5 hours per board for debugging.

This leads to the following computation:

- Number of boards per year: 150
- Number of boards which contain errors: 20 %
- Average time to locate errors: 5 hours
- Hourly personnel rate: 53 DM
- Total costs per year for testing **with** JTAG: 7950 DM

This means reduced costs of about 50.000 DM per year and a payback-period for the project after **two year** because the complete costs for the project are 61.000 ECU which is (nearly) equivalent to 100.000 DM. The product lifetime is 4 years. The ROI is about 300 %.

Two additional important aspects concerning cost reduction should be mentioned here:

A) If the JTAGTEST software detects some errors it also makes proposals what "could be wrong on the board" (for example: possible short circuit between signal X and signal Y on IC 1, Pin 2). Detection and repair of the error can be done by an **non-expert operator** and not an expert operator who can handle complex things like a logic analyzer and has a deep understanding of the functionality of the board.

B) In the past we sometimes had the problem that it is possible to **destroy** components due to board errors. Imagine for example an EPLD who generates control signals for bus drivers. To test the board in the "old-fashioned" way the EPLD must be programmed to get results. If there is an error on the board which disturbs the control signals for the bus driver it could be that the bus driver is destroyed due to bus contention with other chips. With the JTAGTEST the board can be tested without programming all EPLDs and/or FPGAs. This minimizes the risk of destroying additional components like bus drivers during the test phase.

17. Target audience for dissemination

The industrial sectors in which the project and the new product are located can be classified as follows:

A) from a product-point-of-view (application area of the board):

Digital video (and audio) disk recorders can be mainly located in the areas "reproduction of video recording", "electronic components and tele, audio and video equipment", "optical instruments and photography" and "industrial process control equipment" (PRODCOM Codes 2232, 32xx, 3330 and 3340).

B) from a project-point-of-view:

From this point of view the project can be classified in "technical testing and analysis". Most companies, which manufacture electronic products (PRODCOM Codes 30xx to 34xx), must test this products.