

# ***FUSE***

## **Demonstrator document**

**Experiment Submission Number: 25891**

# **Speaking machine for multi-access telecommunication equipment**

**Integration with FPGA reduces testing costs, while  
greatly enhancing performance**

<b>AE:</b>	25891
<b>New technology:</b>	FPGA
<b>Industrial sector</b>	Other telephone switching apparatus (3220)
<b>Contact TTN</b>	COREP

June, 1999

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## 1. AE abstract

**Keywords:** Telecommunication, Phonic group, Added value services, FPGA, VHDL versus schematics, Resource allocation.

**Signature:** 3 0410 555 0410 1 3220 2 32

Appel Elettronica (Italy), a company with 140 employees and 28 engineers, has been active in the communication business since 1967, designing and producing equipment and systems for a large number of applications.

As far as public and private communication networks are concerned Appel Elettronica has reached a high level of expertise in the design of automatic telephone exchange support systems to carry out special and peculiar services such as automatic addressing systems for phone calls of public utility or emergency, automatic systems capable of performing services of added value (exact time, telephone waking, urgent calls, change number announcements, calls re-routing...).

Appel delivers to the domestic market with 20% market share.

Appel Elettronica, whose current microelectronic experience is PCB and microprocessors, has decided to develop a multifunctional system that contains a new phonic group for message recording and reproducing.. They decided to exploit the FPGA technology for the first time. The new system is based on a modular, flexible hardware platform open to implement the telephone exchange support systems having the capability of handling all the services presently performed by different equipment. Additionally its architecture is capable of expansions in order to be able to implement new services.

Thanks to the increased integration it is possible:

- To multiply by 4 the number of processed PCM (Pulse Code Modulation) channels
- To double the maximum storage capacity for the recorded messages (68 min. instead of 34)
- reduced problems in PCB design and manufacturing
- cost reduction in PCB master realisation
- cost reduction due to reduced test and assembly time

The total cost of the Application Experiment is of 45.5 kEUR and its duration has been of 6 months (December 1997 to May 1998).

Considering that the new product will give a positive trend to the mayor part of next years Appel production, and payback period is supposed to be less than one year from May 1998 (end of AE), and we estimate that more than 5 times the global investment will be regained in three years taking into account the global industrialisation costs.

With this AE Appel Elettronica has developed a Phonic Group for a new telecommunication system with performance never reached in previous products (16 PCM streams, that means about 500 telephonic channel served at the same time, up to 68 minutes of phonic messages stored in a static memory bank, including on-board digital mixer). This has been made possible thanks to FPGA technology.

In this AE we developed the FPGA using a schematic diagram approach, because this approach was more familiar to us and requested a shorter learning period; however at the end of the AE we decided to ask our subcontractor to give us a training on the VHDL description and synthesis and learnt how productive, flexible and portable is the tool. In fact at the end of the course we were able to redesign the complete logic architecture in less than 1 week.

Therefore we believe that we will follow this high level design approach for future FPGA developments

## 2. Company name and address

Company name: APPEL ELETTRONICA S.R.L.  
Address: Via Fausto Coppi, 5 - Orbassano (TO) – ITALY  
Phone: ++39 011 9030.411  
Fax: ++39 011 9034.064  
Contact Person: Mr. Paolo Geninatti  
e-mail: [rs1@appel.it](mailto:rs1@appel.it)  
Web Site: <http://www.appel.it>



## 3. Company size

The company employs 140 persons, of which 28 are electronic engineers. Current turnover of the company (1997) is 10,5 MEUR/year

Appel Elettronica is a full manufacturing company: it has a research and development department, an industrialisation and production department, a marketing and sales department, and an installation and service department.

## 4. Company business description

Appel started in 1967 in the radio-engineering field developing amplification systems, mixers, and high fidelity audio recording systems. Subsequently the company undertook the development of equipment and systems in the telecommunication field, which at the moment represent the key products of Appel Elettronica. In particular the company is specialised in the design, construction and installation of equipment for public telephony (equipment and systems installed inside telephone exchanges) and for private telephony (equipment and systems installed at the end-users).

Nowadays, Appel Elettronica has two main branches of products (public telecom and private telecom market), with a common feature for almost all equipment: the voice treatment. Main Appel products are:

- Announcements delivery systems
- Call re-routing systems
- Telephone call loggers and recorders
- Courtesy services
- Voice-mail system

## 5. Company markets and competitive position at the start of the AE

The company delivers to the European and extra-European public and private Telecom companies.

The categories of products where Appel Elettronica has leading roles are the following:

- ❑ Systems for the generation of generic messages and messages dedicated to specific applications (for example Change Number) (DEVIOMAT, DEVIOMAT7, ARIANNA, SIDAN, SCANN4000, ...)
- ❑ Systems for telephone traffic routing with or without the intervention of the user (SNAR7, STAN7/AU)
- ❑ Systems for automatic telephone services (Telephone wake-up call, Speaking-clock, Urgent call) (STAN7)
- ❑ Systems for phone call recording (for police, emergency services and so on) (APPELMASTER, RECORDER PLUS)
- ❑ Interactive voice response systems for large users (OPERA, BRIDGE)

However, all Appel Elettronica products were, before the start of the AE, limited to the function they were developed for, that means that each of them had been conceived to perform a pre-defined set and category of services (for example precise clock, phone wake-up, urgent calls, change number announcements, calls re-routing, call recording, weather forecasting announcement system, chemist's shop time-table information system...).

By examining the economic assessment of these products, from 1995 to 1997, we have a potential domestic global market of about 50 MEUR/year: (this is Telecom Italia investment) for such products and such period. In which, Appel Elettronica had a market share of about 20%.

But Telecom Italia suspended investments for this product category since last May, and new service providers are not ready for this kind of value-added services yet. As a consequence, the actual year forecast reflects a "poor" market.

However, we foresee for 1999 a new positive trend, with a return to previous years mean values.

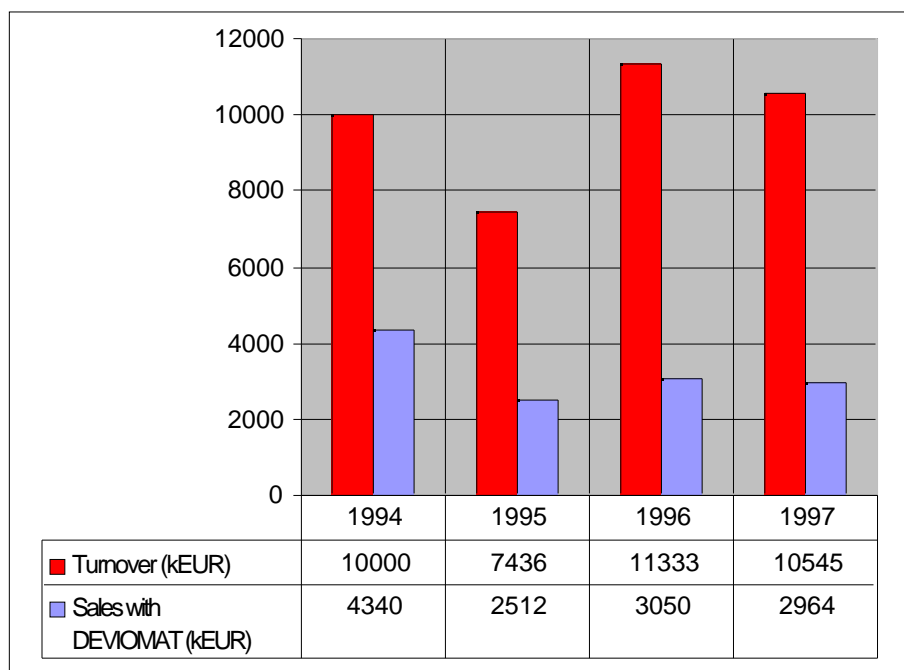
1997 turnover analysis is showed in the following table.

Category	Equipment	Turnover (kEUR)
Courtesy services and Voice-Mail	3830, 4030, OPERA	1154
Interactive Voice Response Systems	BRIDGE	949
Recording Systems	RECORDER PLUS, APPELMASTER	92
Change Number Announcement Systems	DEVIOMAT	2964
Automated Service Systems	STAN7	97
Conversion Systems	RAB, DIBRA	1981
Alarms Management Systems	SGA/TLI	3067
Others		241
<b>TOTAL</b>		<b>10545</b>

The purpose of new product development, of which the AE is an main part, is to obtain a complete and versatile multi-application platform, on which, with the aid of a *Service Creation Environment*, the customer is able to develop its own applications.

As a matter of fact our aim is not limited to innovate a single product. Our final goal is to upgrade a full set of products. However, we decided to select a single application, the DEVIOMAT, a change number announcement system since with this product APPEL Elettronica has obtained an important part of its turnover in the last five years.

Appel Elettronica turnover before the start of AE is show in next figure.



Unfortunately the discontinuity in the telecommunication market does not allow, especially for small-medium size enterprises, reliable long-term sales forecast.

In any case APPEL foresees, in the next few years, to confirm its presence in the domestic market and expand, thanks to the EMU, its presence (presently negligible) in the world wide market, with a global increase of its total gross operating margins (2500 kEUR of foreign market forecasted for 1999).

The main Italian competitors of Appel are companies which have, more or less, the same domestic market share, and, like Appel, are present in domestic telecommunication market since years. They include Urmet, that, with its Service Node, has a market share of about 22% and Necsy, which is just below 20%.

They are companies whose main goal is not "voice". Appel, instead, made with voice and sound recording and management, its core business since birth.

Very different is the European scenario, where this sector is covered by big companies (such as Alcatel, Matra, Ericsson, Lucent Europe, Clemessy,...), that, however, can't offer a versatile, customisable, easy to use and reliable product as the new Appel system. This because value-added special telephone services does not represent their core business.

However, all competitor products are complete and interesting, and we surely know that it won't be easy to reach our market share target.

Technically, competing products use a different technological approach based on PC or workstation, platforms instead of dedicated hardware solutions.

Often, competing products don't have a static Phonic Group, but instead a messages delivery system based on magnetic storage media (single hard-disks, or disk array configurations).

Hence, APPEL products are expected to be more reliable, cheaper, smaller and with better performance. However, our development costs are higher with a longer time to market.

In any case, APPEL is strongly convinced that its strategy will pay-off in the long term and believes that the new component developed in this AE will represent a breakthrough in this direction.

We can summarise the competitive strength of our phonic group in the following:

- Increased flexibility (with a much more modular approach than the one allowed by the magnetic hard disks)
- Better performance and lower size due to a more efficient architecture.
- Higher reliability due to very severe test and acceptance procedures.

Main weaknesses reside in:

- an higher price (due to higher development, manufacturing and test cost)

- a longer development time

This is why APPEL decided to introduce more integration into our current product to save costs and reduce the time to market.

## 6. Product to be improved and its industrial sectors

The product improved in this Application Experiment is DEVIOMAT, a Change Number Announcement delivery system with call re-routing.

It is a system for automatic Change Number Announcements and call re-routing on a 2 Mbit/s PCM stream.

DEVIOMAT receives, from the public telephone exchange, the calls addressed to the old number, answers them with a change-number announcement containing the new number, and then automatically re-routes the call to the new number.

DEVIOMAT has a digital interface (4+4 PCM 2 Mbit/s), it can handle up to 120 telephone call at the same time, and has a phonic group with RAM and EPROM stored messages

DEVIOMAT Phonic Group has the following characteristics

Technology:	Phonic Group with messages stored on static RAM. Control functions implemented using and group of low-complexity PLDs (9 chips)
Number of telephone lines served simultaneously:	120
Maximum capacity of message memory:	16 Mbyte equivalent to 34 minutes of message recording
Maximum number of messages:	256
Maximum delay of message emission:	512 ms

The block diagram of the Phonic Group is shown in Fig. 5.1, where following functional units can be identified:

- ❑ Four PCM streams: they represent the connection lines of the Phonic Group towards the Public Telephone Network. Each 2 Mbit/s PCM stream handles 30 telephone lines.
- ❑ Memory Bank: it represents the functional unit where the phonic messages, previously digitised, are stored
- ❑ Priority Encoder: it handles the requests of access to the Phonic Group coming from the 120 telephone channels (4x30) connected to the system, establishing priorities and avoiding conflicts within the time constraints of the PCM streams. Each channel shall be able to access the Phonic Group within 125  $\mu$ s.
- ❑ Message Allocation Table: it is the support ancillary memory within the main memory where the information of phonic message allocation is stored.
- ❑ Address Counter: it generates the addresses for the memory bank to allow the generation of the requested phonic message on each line.
- ❑ Timing Source: it supplies the timing control criteria and synchronisation for all the other functional units.
- ❑ CPU: it carries out the supervision of the Phonic Group controlling the request of emission of messages coming from the telephone lines.

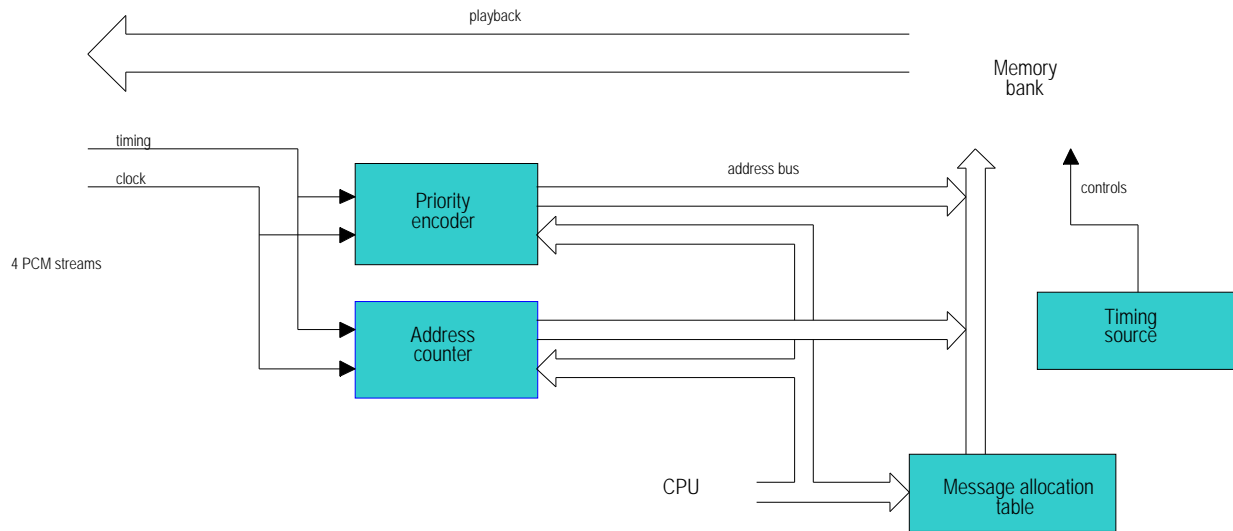


Figure 5.1: Block diagram of existing Phonic Group

Our objectives in innovating the old product were:

On the domestic market

- increase our sales to the main Italian telecom public service (at least 5%)
- address the new request of the new private service companies (taking at least 30% of the market share)

On the European (and extra European) market

- Acquire a significant market share (at least 2%; currently our presence is negligible).
- increase the number and the flexibility of the offered services
- increase our capability to handle more advanced electronic technologies

In the previous figure the coloured blocks represents the parts replaced in the new control based on FPGA technology.

In order to comply with the requests of our most important customers we have planned the following improvements for the new generation of the DEVIOMAT product:

- ❑ Increase of the number of simultaneously deliverable messages (to 16 PCM streams, that is 496 telephone channels using common channel signalling protocol)
- ❑ Add a digital mixer block, that performs a run-time digital mixing of two different stored messages (for example a music with a speech message)

A photograph of the old phonic group board is showed in fig. 5.2.



Figure 5.2: Old phonic group board

The complexity of the board can be represented with :

- ❑ Double Europe size (233\*220 mm)
- ❑ 16 Mbyte memory
- ❑ 9 chip low density PLDs (5000 equivalent gates)
- ❑ Pin limited usability of the PLD (total gates number is much larger than requested because of the pin-out needed)

## 7. Description of the technical product improvements

To comply with the motivations reported in the previous section, we have developed a new Static Phonic Group able to carry out the simultaneous generation of messages for 496 telephone channels (32 channels for each one of the sixteen 2 Mbit/s PCM streams handled by the new system); every message will always be reproduced from the beginning with a minimum delay with respect to the relevant emission request. A digital mixer having the particular feature of the contemporary generation of two phonic tracks (i.e. the actual message and background music) on each channel output is under development. The phonic messages are to be loaded onto a RAM memory bank having the possibility of remote control.

The main performances of this Phonic Group are:

Technology:	Phonic Group with messages stored on static RAM. Control functions implemented using a single FPGA of medium-complexity (2500 gates-equivalent)
Number of telephone lines served simultaneously:	496

Maximum capacity of message memory:	32 Mbyte equivalent to 68 minutes of message recording
Maximum number of messages:	1024
Maximum delay of message emission:	512 ms

The block diagram of the newly developed Phonic Group is shown in Fig.6.1, where the following functional units can be identified:

- ❑ Sixteen PCM streams: they represent the connection lines of the Phonic Group towards the Public Telephone Network. Each 2 Mbit/s PCM stream handles 31 telephone lines.
- ❑ Memory Bank: it represents the functional unit where the phonic messages, previously digitised, are stored
- ❑ Digital Mixer: it is the unit which allows the mixing of two phonic tracks during the transmission on each telephone line
- ❑ System Phonic Bus: it is the unit that interconnects the phonic channels of all the system; it is also used for the remote loading of the messages to the RAM memory bank.
- ❑ Control Unit: it handles the timing of the units, the addressing of the RAM memory bank
- ❑ CPU: it carries out the supervision of the Phonic Group controlling the request of emission of messages coming from the telephone lines.

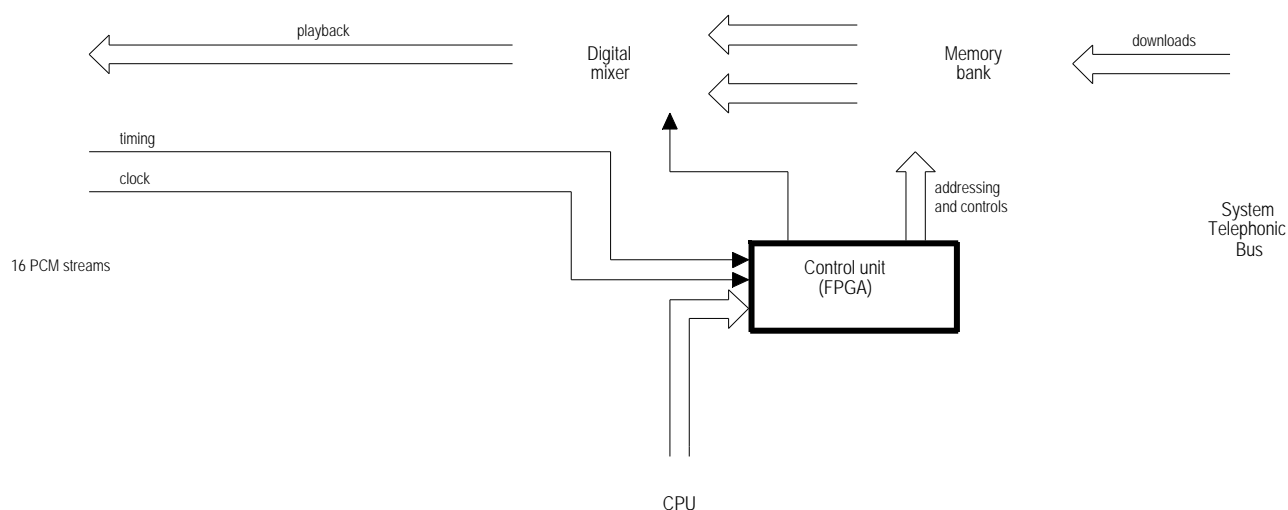


Figure 6.1: Block diagram of the new Phonic Group

Fig. 6.2 shows the block diagram of the Control Unit that will be implemented using FPGA technology.

The following functional groups can be identified: the Priority Source, which controls and puts the access requests to the Phonic Group in sequence, the Addressing Source, which drives the memory bank, the timing and control circuit of the Digital Mixer, the RAM memory where the message allocation table is stored.

As you can see, the only functional unit of SMMATE that are not been inserted into the FPGA are function that couldn't be inserted into a medium-complexity FPGA, which include:

- ❑ SRAM bank (32 Mbyte)
- ❑ Digital mixer (using a 128k x 8 bit EPROM)
- ❑ CPU (a Motorola 32 bit microcontroller MC68340)
- ❑ PCM and system bus interface circuitry
- ❑ Non volatile (battery operated) static RAM (SRAM)

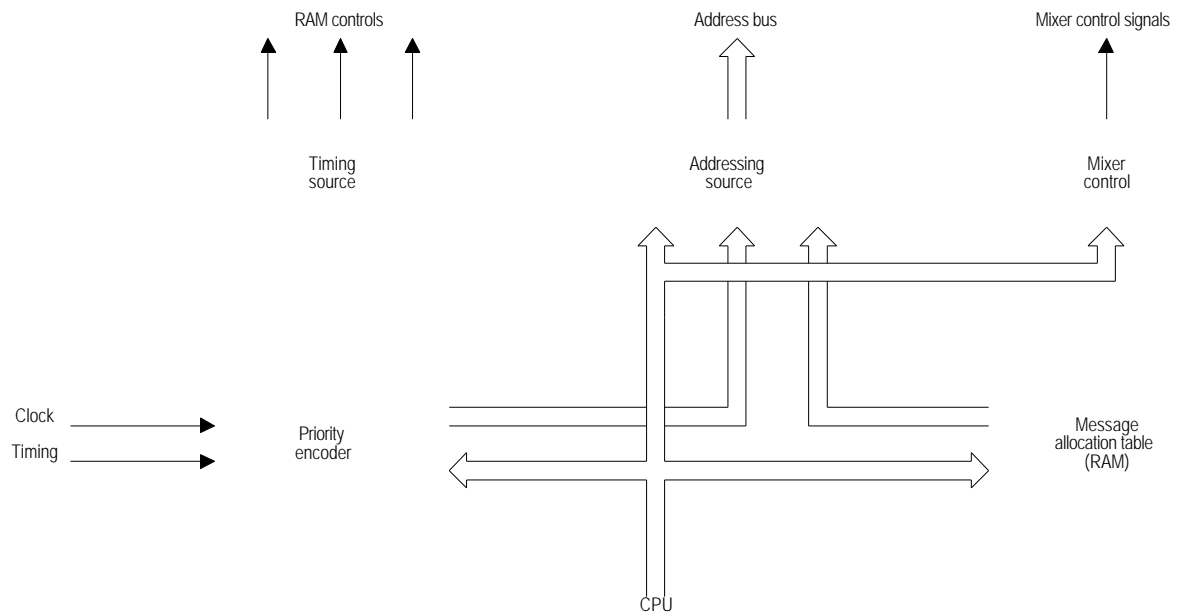


Figure 6.2: Block diagram of the Control Unit of the Phonic Group (new design)

A photograph of the new phonic group board is showed in fig. 6.3.

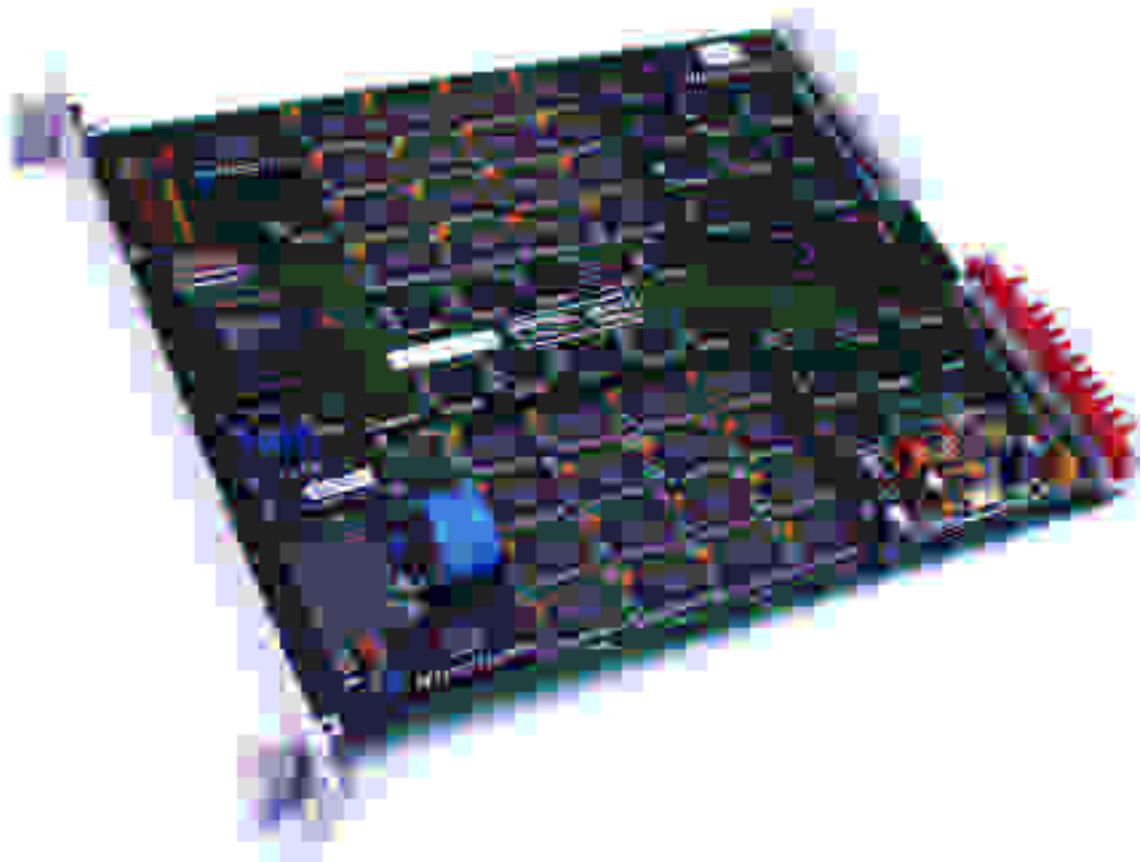


Figure 6.3: New phonic group board

The overall complexity of the FPGA can be estimated of the order of 2500 gates and it implements all the Finite State Machines used to control the whole Phonic Group (addressing, priority encoder, mixer control, timing control)

The new phonic group has almost the same production costs (components, mounting, process and test costs) of the old one, but it is included in a much more complex unit of large added value for our company. The product competitiveness is due to the following improved features:

- ❑ number of telephonic channel multiplied by 4 (from 120 to 496): this means that each new board is able to manage 4 times the number of channels than the old one
- ❑ storage capacity doubled (from 34 to 68 minutes): this means that the storage message duration is doubled
- ❑ mixer function inserted: this means the possibility to have a musical tone in the background of the message
- ❑ Modularity and versatility of the new board assure the possibility to easily include upgrades and future improvements
- ❑ Completely realised with electronic technologies (SRAM, EEPROM, FPGA) instead of magnetic disk as the other products of our major European competitors

The new features would not have been compatible with the level of integration of our current technology and requested to introduce a new technology as explained in the next section

## **8. Choices and rationale for the selected technologies, tools and methodologies**

In the new Phonic Group we wanted to keep the PCB manufacturing cost at the same level of the previous one (110÷120 EUR), while greatly enhancing the obtained performance.

With this objective we examined the different technological alternatives.

- ❑ traditional technology based upon the use of discrete components with a low level of integration as it is in the existing Appel Elettronica products
- ❑ FPGA technology
- ❑ ASIC technology

The enhanced performance (for example the increased clock frequency (40 MHz)) and the newly introduced features, discouraged us in following the conventional approach with standard PCB and discrete logic components, considering that in this case the size of the PCB (increased of more than 40%, according to our estimation) would have been a bottleneck for the new product (with an estimated increased cost of more than 20%). This is due to the requested high number of low complexity PLDs, (more than 20 for handling the highly increased number of telephone channels and recorded messages) and a clock frequency which is higher than technology limit of previously used components (30 MHz).

The ASIC solution has not been taken into consideration because the low production volumes (few thousands per year) are not sufficient to justify the cost of the masks (more than 20 kEUR) and the strong and extended requested effort (development time nearly doubled with respect to an FPGA).

The second solution (FPGA) seemed to be the most feasible one within the constraints of limited cost implications and acceptable technical risks related to the guaranteed performances of internal flexibility and speed.

The choice of FPGA family to be used in the new board has been made after a careful market survey.

Two alternatives seem to meet our requirements in the best way: FPGA product family developed by Xilinx and those developed by ACTEL.

Xilinx products have been chosen for the following reasons:

- 1) Xilinx FPGA architecture, based on a CLB array, with CLB structure very simple and versatile, could be well adapted to SMMATE project requirement: our design needed an intensive use of sequential logic (counter and shift registers mainly) working with 3 different clocks (2 MHz, 4MHz and 30 MHz).
- 2) Xilinx is a manufacturer with great experience; since it offers this kind of component since 1985.
- 3) Xilinx could offer a complete set of solutions to First Users such as:
  - Development and simulation software
  - Placement and routing software
  - Hardware for off-board programming of components
  - Technical support during development
  - Training courses

As FPGA development methodology, we could choose between two different possibilities, both supported by Xilinx tool: schematic and VHDL (really, for VHDL development, we also would have needed a third party synthesis and simulation tool).

Surely, schematic approach required a shorter training period than VHDL, because we already normally use CAE tools for schematic editing.

Moreover, our FPGA complexity (in gate-equivalent term) was not so high, and for this, a schematic approach design could appeared advantageous.

So, we decided to develop our FPGA using a schematic entry approach.

However, learning how to design with VHDL was one of our main goals, for future FPGA developments, and a VHDL training course, given by a selected consultant during the AE, provided us with a solid base.

## **9. Expertise and experience in microelectronics of the company and the staff allocated to the project**

The company has expertise in development, production and installation of telecommunication equipment and systems.

In the telephone field, the different development steps of communication networks have been passed through with products characterised by various telephone interfaces (analogue, digital, PCM, ISDN).

The company has an established experience in developing telecom circuits using PCB technologies with off the shelf logical gates, microprocessors and low complexity PAL and PLD.

The personnel involved in this Application Experiment include:

- Project manager: 10 years of experience in hardware and software engineering and 5 years of experience in project managing
- Senior HW/FW engineer: 8 years of experience in hardware and software engineering
- Junior HW/FW engineer

The following technologies have been used and are currently used by APPEL Elettronica:

- traditional analogue components (discrete components, operational amplifiers,...)
- traditional digital components (logic families such as CMOS, TTL, high speed CMOS, advanced CMOS)
- eight and sixteen bit microprocessors (Motorola 68HC05, 68HC11, 68000, Intel 80x86, NEC V25+)
- fixed point 16 bit DSP (Texas 320C25)
- commercial VLSI peripherals (2 Mbit/s PCM stream interfaces, UART, HDLC controller,...)
- programmable digital components (PAL , PLD)

- ❑ double face and multi layers PCB with through-hole and SMT components (Appel uses it but doesn't develop it itself).

Neither FPGAs nor ASICs have been utilised till now; similarly development systems based upon high level editing (such as VHDL and schematic entry) and timing and functional simulations have not been used.

## 10. Workplan and rationale

**Risk Assessment:** The risk for an FPGA development (at least at this level of less than 3000 gates complexity) is not very high for a company with an established electronic know-how infact:

- The CAD tools for the design are user friendly and self explaining
- The hardware is reconfigurable and therefore design errors can easily corrected and last minute changes accommodated with minor effort

The original work plan of SMMATE development has been divided in following phases:

- WP0: Management
- WP1: Definition of the specification
- WP2: Personnel training
- WP3: Development and simulation of the component
- WP4: Integration of the component in the host board
- WP5: Prototype development
- WP6: Prototype testing

### WP0-Management

- ❑ Objective: to develop an efficient and attentive project management throughout the whole experiment
- ❑ Time duration: 6 months
- ❑ Description of the activity: in this phase the technical management of all design development activities planned for the application experiment was carried out
- ❑ Measurement of the success: Deliverables completed and available according to the foreseen schedule
- ❑ Roles and responsibilities:  
First user: plans and controls the application experiment operation  
First user: contributes to the creation of the dissemination material
- ❑ Deliverables:  
First user: monthly report  
First user: dissemination material
- ❑ Task list:  
T01: project management  
T02: dissemination

### WP1-Definition of the specification

- ❑ Objective: to define the FPGA specification and its interfaces with the host board of the Phonic Group
- ❑ Time duration: 2 weeks
- ❑ Description of the activity: in this phase the development specifications of the FPGA and its interfaces with the host board (I/O signals, timing, ...) was defined
- ❑ Measurement of the success: release of the technical specification of the FPGA and of the host board

- ❑ Roles and responsibilities:
  - First user: to prepare the technical specification of the FPGA
  - First user: to prepare the technical specification of the host board
- ❑ Deliverables:
  - First user: technical specification of the FPGA (milestone M11)
  - First user: technical specification of the host board (milestone M12)
- ❑ Task list:
  - T11: FPGA technical specification preparation (6 person/days )
  - T12: host board technical specification preparation (4 person/days)

## **WP2-Personnel training**

- ❑ Objective: to train the engineers in the use of FPGA, its architecture and the relevant development tools
- ❑ Time duration: 4 weeks
- ❑ Description of the activity: in this phase external training courses and internal on job training was carried out
- ❑ Measurement of the success: successful completion of the training courses
- ❑ Roles and responsibilities:
  - First user: purchase of Development Tool for FPGA (SW)
  - First user: purchase of Development Tool for FPGA (HW)
  - First user: purchase of Personal Computer for FPGA Development (HW)
  - First user: internal on job training
  - Subcontractor 1 (Xilinx): training course on Development Tool for FPGA
  - Subcontractor 2 (Europractice): training course on VHDL
- ❑ Deliverables: certificate of course completion
- ❑ Task list:
  - T21: training course on VHDL (7 person/days)
  - T22: development tool course (7 person/days)
  - T23: on job training (10 person/days)

## **WP3-Development and simulation of the component**

- ❑ Objective: To develop the simulation and the programming of the FPGA
- ❑ Time duration: 6 weeks
- ❑ Description of the activity: in this phase the hardware description of the component was carried out using its specific development tool and the timing and functional simulation of the chosen component
- ❑ Measurement of the success: preparation of the hardware description file and successful completion of simulation tests
- ❑ Roles and responsibilities:
  - First user: completion of component development
  - First user: completion and verification of the functional simulation
  - First user: completion and verification of the timing simulation
  - Subcontractor 3 (University of Genoa): design assistance
- ❑ Deliverables:
  - First user and subcontractor 3: component programming file (milestone M31)
  - First user and subcontractor 3: functional simulation file (milestone M32)
  - First user and subcontractor 3: timing simulation file (milestone M33)
- ❑ Task list:
  - T31: component development (10 person/days)
  - T32: functional simulation (10 person/days)
  - T33: timing simulation (10 person/days)

## **WP4- Integration of the component in the host board**

- ❑ Objective: to define the electrical schematic of the FPGA host board
- ❑ Time duration: 2 weeks
- ❑ Description of the activity: in this phase the schematic of the board where the FPGA was installed is to be completed
- ❑ Measurement of the success: release of the schematic of the host board
- ❑ Roles and responsibilities:  
First user: to develop the schematic of the host board
- ❑ Deliverables:  
First user: electrical schematic of the host board
- ❑ Task list:  
T41: development of the schematic (10 person/days)

### **WP5-Prototype development**

- ❑ Objective: to develop the prototype of the board containing the FPGA
- ❑ Time duration: 9 weeks
- ❑ Description of the activity: in this phase the following items are to be developed: the PCB master, the PCB prototypes and the Phonic Group board prototype
- ❑ Measurement of the success: availability of the Phonic Group board prototype
- ❑ Roles and responsibilities:  
Subcontractor 4 (Paleologo Company): development of the PCB master  
Subcontractor 5 (Corona Company): PCB samples  
First user: assembly of the components on the PCB
- ❑ Deliverables:  
Subcontractor 4 (Paleologo Company): PCB master (milestone M51)  
Subcontractor 5 (Corona Company): PCB samples (milestone M52)  
First user: Phonic Group board prototype
- ❑ Task list:  
T51: PCB master development (4 weeks-external)  
T52: PCB samples development (4 weeks- external)  
T53: PCB assembly (3 person/day-)

### **WP6-Prototype testing**

- ❑ Objective: to test the FPGA board prototype
- ❑ Time duration: 3 weeks
- ❑ Description of the activity: to test the correct operation of the FPGA and of the host board
- ❑ Measurement of the success: successful completion of the test
- ❑ Roles and responsibilities:  
First user: prototype testing
- ❑ Deliverables:  
First user: Phonic Group board prototype (milestone M61)
- ❑ Task list:  
T61: prototype testing (25 person/ day)

### **Actual workplan at the end of AE**

Several modifications have been made to the initial organisation during the AE development:

#### **Different Role of subcontractors**

Subcontractor 1 (EUROPRACTICE) was eliminated (reasons are explained below)

Subcontractor 2 (XILINX) was only used for supplying the FPGA and the software tools and for giving us assistance with the use of the component.

Subcontractor 3 (University of Genoa) was mainly used for training on VHDL tool and for hot line assistance, but was not given any responsibility for the design as it was planned in the original proposal

### **Different training scheduling**

- We have suppressed T22 (development tool course) for the following reasons:
  - Xilinx wasn't able to offer us such training when we had planned it
  - Europractice (another subcontractor, specialised in ASIC/FPGA training courses) wasn't able to offer us such training when we had planned it
  - We choose a 'schematic editing' approach to FPGA development and the tool we'd brought seems to be very user-friendly and self-training for this approach
- We have postponed and lengthened T21 (VHDL training course) for following reasons:
  - We choose a 'schematic editing' approach to FPGA development and, for this, VHDL training was not urgently needed.
  - However, we would learn VHDL approach for ASIC and FPGA for future projects and we also would, as a training example, try to redesign our FPGA with VHDL language, comparing the results with those that we obtained with the schematic approach (that was working without problems).

#### a) T51 (PCB master development) delayed

- T51 task results lengthened because, as a consequence of circuit complexity and circuit timing requirements, the PCB resulted more complex to develop than we had planned, and with greater layers number.

#### b) T61 (prototype testing)

- Field tests of the new product went on after the end of AE. The main reason for this was the availability of our customer (Telecom Italia). For this, we didn't require to prolong the AE itself.

Next figure shows initial and actual AE workplan.