Application Experiment 235

FPGA based Digital Mobile Radio Processor

Realises radio systems for national coverage

AE abstract

Rohill Engineering designs, develops, produces, and sells systems and products for professional mobile telecommunication. The company is focused exclusively on the professional mobile communications market. The products are sold through agents (assistance during sales phase only), OEM / consultancy and distributors / system integrators.

The product portfolio includes trunked radio systems, hand portables, and mobiles for trunked mobile radio operation, and peripheral equipment for trunked radio systems and conventional radio systems. The application for these systems and equipment can be divided in security applications (police, fire brigade, ambulance), utilities (electricity, gas and water suppliers), transport and industry (industrial estates, chemical factories).

The AE (Application Experiment) is related to an application within the infrastructure of trunked radio systems. An FPGA has been developed, which is used to perform switching, routing and multiplexing/demultiplexing of speech and data streams. These streams of speech and data are transferred using modem and ISDN technology, and replaces the existing software solution.

The FPGA based product allows Rohill to sell and build significant larger infrastructures for trunked radio systems than was possible with the current product. Furthermore, it will enhance their competitive position when customers consider (future) expansion of existing networks.

The project was exeuted in the planned duration of 16 months excluding reporting. However, due to market changes during the project an FPGA solution was produced rather than an ASIC. The original budget of 117 kEURO was therefore reduced to 97 kEURO. It will cost a further 400KEURO to productionise the unit. It is estimated that the AE investment for this project will be paid back within a year. The ROI, assuming a 5 year product life cycle, will be 16 times the AE investment.

The AE has provided Rohill with the knowledge and experience for designing FPGA using VHDL, as well as the steps that have to be performed to realise these components. Although the end-result is a FPGA, a gate-array as well as a standard-cell ASIC has been considered as alternatives. This could become important if the quantities rise significantly. During the AE, Rohill managed to solve a wide range of problems, especially related to the correct use of the CAE software. They also learnt that it is more effective, in the long term, to get expert advise and training in VHDL and FPGA design rather than trying to follow the self taught route.

Keywords: FPGA, VHDL, Telecommunications, CAD Tools, Switching, Multiplexing of speech, radio system

1. Company name and address

The company address and related information is shown below:

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2. Company size

The company, founded in 1992, now employs 25 persons, of which 9 are involved in the development of hardware and software. Their turnover in 1999 was 6M EURO.

Rohill Engineering is part of the "Van der Boom Holding" group of companies. This group includes the company T.F.K. Benelux, a distributor for mobile phones and professional mobile communication equipment, and Nethlease, a service provider for the Traxis network of KPN Telecom. This group achieved a turnover of 14 million EUROs in 1998.

3. Company business description

Rohill Engineering designs, develops, produces and sells systems and products for professional mobile telecommunication.

The company is focused exclusively on the professional mobile communications market. The products are sold through agents (assistance during sales phase only), OEM / consultancy and distributors / system integrators.

The product portfolio includes trunked radio systems, hand portables and mobiles for trunked mobile radio operation, and peripheral equipment for trunked radio systems and conventional radio systems.

The trunked radio systems and subscriber equipment (hand portables and mobiles) are based on the MPT-1327/1343 standard. The application for these systems and equipment can be roughly divided in security applications (police, fire brigade, ambulance), utilities (electricity, gas and water suppliers), and transport and industry (industrial estates, chemical factories).

The main markets are those which require MPT trunked mobile radio systems and terminals. These include Germany, U.K., The Netherlands, Belgium, Denmark, Poland, Chech Republic and also Indonesia, Malaysia, Thailand, India and China. In these countries, products are mainly sold through distributors and system integrators. Systems are also sold through agents, in Vietnam and Saudi-Arabia. The MPT trunked radio market accounts for around 80% of the company's turnover. Some MPT products are also sold under an OEM agreement.

The company is mainly involved in the product development, marketing and sales activities whilst high-volume production is subcontracted to third parties. A small team of personnel is also engaged in the installation, commissioning and servicing of systems and products.

Consultancy projects are mainly spin-off projects, whereby an already completed software project is ported to another hardware environment. Large consultancy projects have been completed for a number of large multi-national companies.

Rohill also markets other products, both related to trunked radio systems and conventional radio systems. The turnover for these other products varies between 20% and 30% of the total turnover.

Other products include:

- Emperor-9 mobile radio for MPT-1327/1343 trunked mobile radio systems
- Emperor-7 hand portable radio for MPT-1327/1343 trunked mobile radio systems
- R-580 trunking telephone interconnect, a product that interfaces a third-party trunking radio system with a company's PABX
- R-2000 series base station transceivers
- Products for integration within conventional radio systems, such as the R-292 Base Station Controller and R-280 Telephone Interconnect

4. Company markets and competitive position at the start of the AE

The large number of trunked radio standards, the transition of analogue towards digital trunked radio systems and a fast changing market place (introduction of GSM) creates a large amount of diversity. Because of this diversity, it is rather difficult to specify detailed figures for market size, market shares and future development.

One method to quantify the market for mobile radio systems is to relate the figures such as market share and cost to the number of radio ports. This is necessary due to the fact that a single trunked radio system can either be a low-cost, small single site system supporting only 4 radio channels, or could be a large, national wide coverage system, supporting as many as 2,000 radio channels.

The estimated market share of Rohill in various markets is shown in the overview below:

Market	Market share	Countries in which the product is marketed
Worldwide	3 %	Marketed in Indonesia, Vietnam, China, India, Malaysia, etc.
Europe	2 %	Marketed in Belgium, Denmark, Poland, Chech Republic, etc. Note that Rohill is not particular strong in large markets such as Germany and the UK.
The Netherlands	3 %	Note that the market share is highly affected by the large public trunked radio system operated by PTT Telecom, which is delivered by Nokia

In the table below, an overview of the most important competitors and their market share is given. Also their market focus are shown for each of our competitors. Note that the figures are based on own market research, not on published facts.

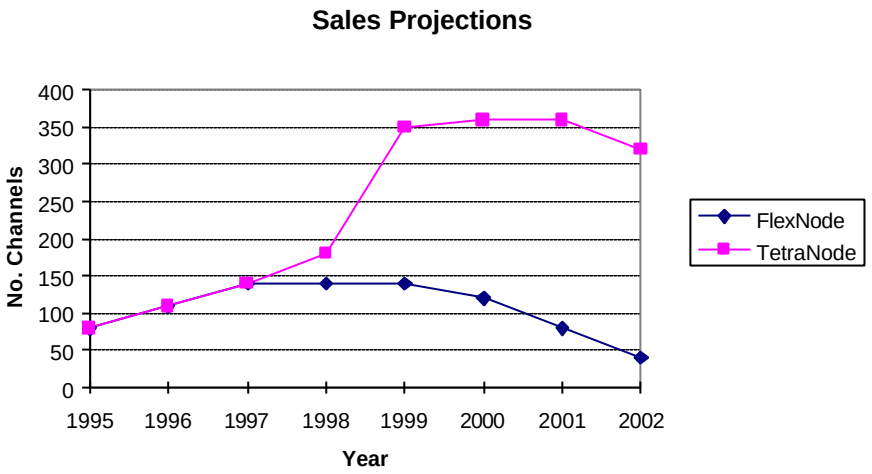
Company	Market %	Price / channel	Market focus
Rohill	3	7.000 K EURO	Small & medium sized systems
A	27	13.000 K EURO	Large, nation-wide systems
B	15	12.000 K EURO	Medium sized systems, German market
C	20	11.500 K EURO	Large systems, low density
D	6	9.500 K EURO	Medium sized systems
E	10	10.000 K EURO	Small & medium sized systems
F	4	8.000 K EURO	Small & medium sized systems
Others	15		

The total market in 1997 was around 5,000 channels and is anticipated to grow by at least a factor of 5 over the next few years.

The price per channel is an average for medium sized system (total of 50 radio channels), whereby all switching and interfacing hardware is included, not only the basic transceiver hardware.

In comparison with other suppliers in the market, the product of Rohill can already be delivered for the lowest cost. The main reason for this is the high level of integration, hence lower component and production cost, plus the fact that most of the functionality is realised in software instead of in hardware. This concerns especially the switching functionality. The product also offers a high degree of flexibility due to the emphasis on software implementation.

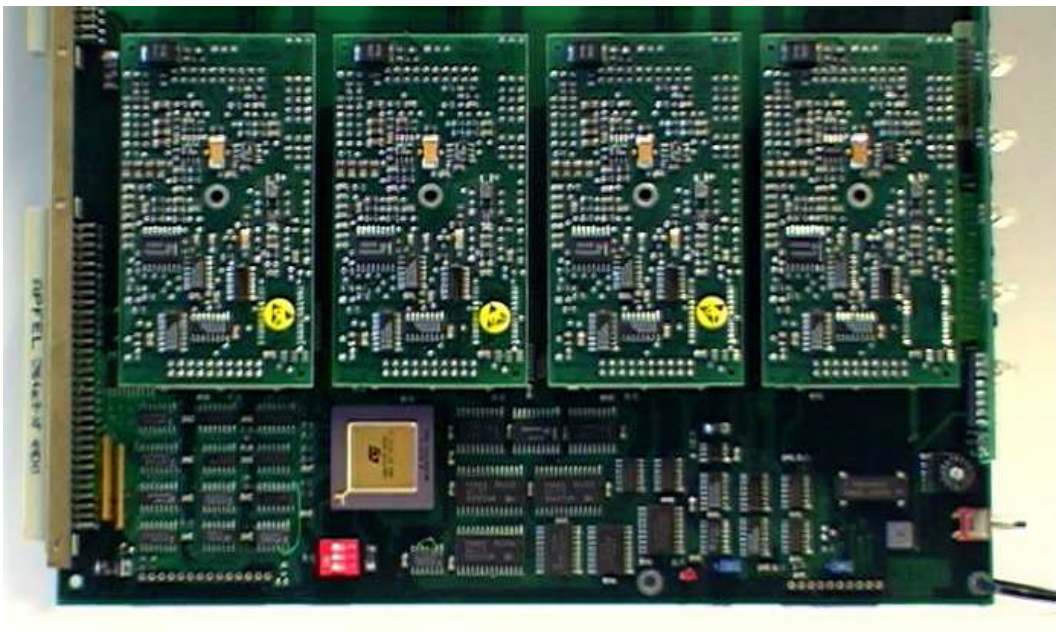
The growth of Rohill's market share, however, is limited by the fact that Rohill cannot deliver large systems. In these market segments companies such as Nokia and GEC/Marconi are much better equipped. The new product will enable Rohill to sell larger systems, and also attract buyers that are planning to expand small or medium sized systems.



Sales projections for TetraNode vs. FlexNode

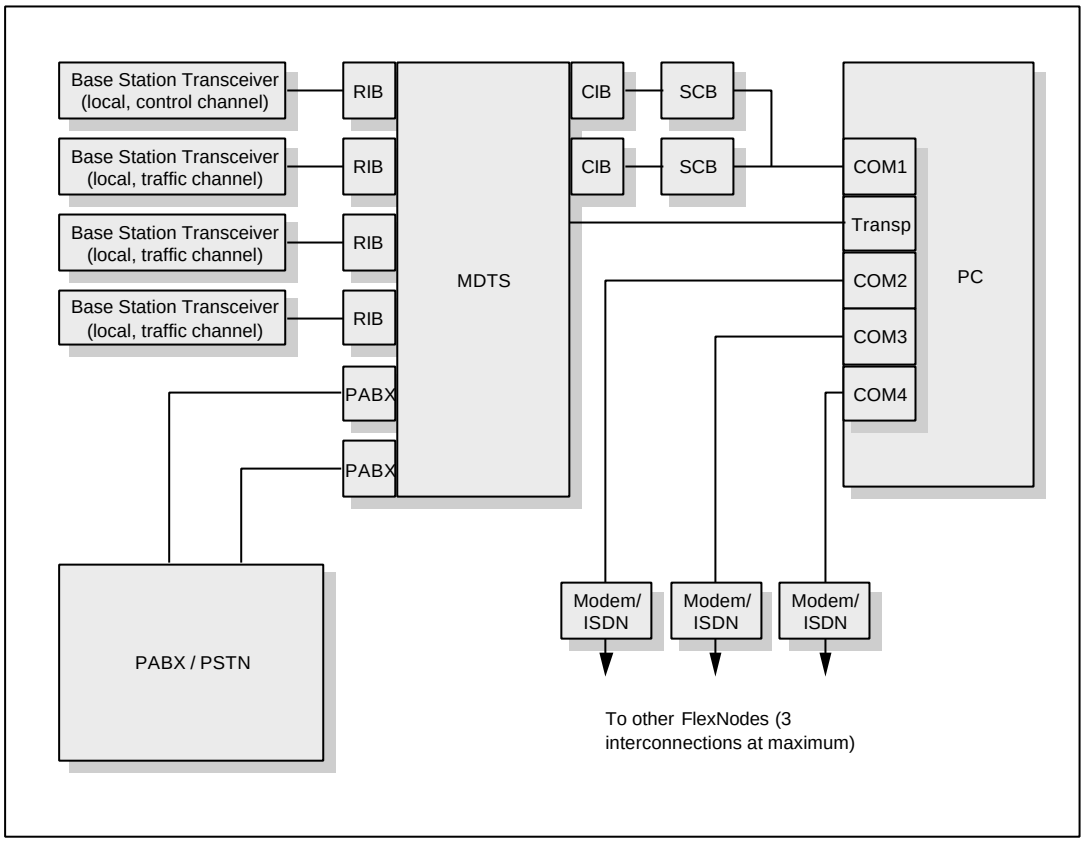
5. Product to be improved and its industrial sectors

The current FlexNode consists of a dual-ported RAM, system-bus buffers and communication-bus buffers, a transputer, and glue-logic components. The transputer takes care of the 'drop-and-insert' switch function for the speech data. In the new product, the FLEXBUS FPGA will replace 50% of the components that are shown in the picture below.



Electronics of the current single FlexNode site

The overall product consists of a number of components, which are shown in the following diagram:



Block diagram of a single FlexNode site

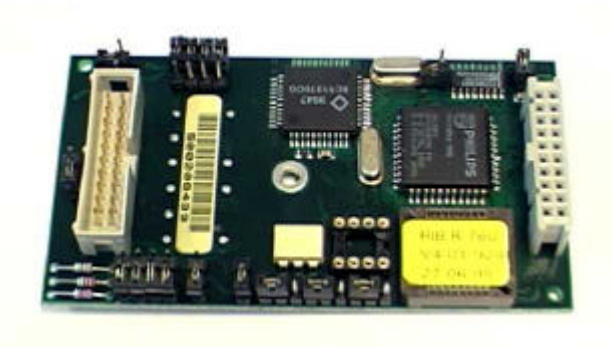
The above block diagram shows a typical configuration of a single FlexNode site. This site is equipped with four radio channels, of which one is dedicated for the control channel signalling (call set-up, registration, etc), and three for speech traffic. The MDTS controls these radio channels, and handles all local traffic within the site. Also a 2 port interconnection to a PABX or PSTN is shown, used for direct communication between mobile users and telephone users.

To realise a system with multiple sites, the MDTS's must be interconnected. In the above diagram two ports are reserved for this purpose, thus two speech connections can be established simultaneously. The interface card should be of the type CIB (Communication Interface Board).

The 64 kbps PCM speech is then routed to the SCB (Speech Compression Board). The SCB converts the 64 kbps PCM speech into 5.0 kbps ACELP compressed speech and vice-versa. The loss of speech quality is very low for this kind of compression.

The PC performs the switching and routing of the low-speed speech data to other sites via the interconnection lines. For this purpose, the speech data is converted into a 'stream' of data, which is multiplexed with data packets and send via the interconnection lines. With the overhead necessary for streaming and bit/byte synchronisation, the bit-rate is around 8.0 kbps per speech channel, thus using 33,6 kbps modem technology, up to four of these speech streams can be transferred over the modem

link. In practice, always one stream will be reserved for exchange of data packets, thus for the above example; the maximum interconnection will be 3 speech plus 1 data channel.



One of the four radio channel boards

The FlexNode PC hardware and software can be considered as the bottleneck for larger applications. The performance of a single CPU is not sufficient for applications requiring more than 3 interconnections, or a higher bandwidth than 32 kbps per interconnection. On basis of these limits, the maximum size of a complete system is limited to around 5 nodes. Even when using the most recent Intel Pentium II innovations, the capacity is only increased by a factor of two.

Tasks, which are currently handled by the Pentium processor within the PC hardware, include:

- Location management, i.e. maintaining a database where the location of each mobile or hand portable is stored (used for roaming, the capability of a trunked radio system to contact a radio on the radio site where it is registered onto)
- Exchanging event messages i.e. to establish or disconnect a speech call, to transfer data messages through the network, or to update the location databases
- Switching of data packets and speech streams
- Multiplexing and de-multiplexing of data packets and speech streams
- Controlling the serial input/output devices (UARTs)

Especially the last three functions require a high amount of processing power. Due to the complexity of the switching and multiplexing tasks, each operation triggers the exEUROtion of a large number of instructions. This is the main reason that the interconnection capability is limited to 3 links.

The cost of a system is a secondary matter.

The market for 'trunked mobile radios' (trunking radiotelephone) has become fiercely competitive, where big players like Nokia and Motorola are now playing a significant role. The Emperor-9 still remains in Rohill's delivery schedule, although the market opportunities are reduced to client specific applications. Therefore the expected production/sales projections have been revised to about 350 channels per annum instead of the anticipated 1,000's.

6. Description of the technical product improvements

The key component for infrastructure applications is the Rohill Modular Digital Trunking System, or MDTS. This MDTS offers a capacity of 32 ports for interconnection to radio channels, PABX/PSTN lines, and interconnection to other systems. Although the capacity is adequate for small, single-site systems, many applications require more than 32 ports, or require distributed systems at different

locations (lower leased-line cost). The first approach was to interconnect multiple MDTSs to each other using a smart software solution running on a PC, which was marketed under the FlexNode brand name.

The capacity of the FlexNode topology, however, was limited to interconnection of at maximum five MDTSs. To increase the number of interconnections, a hardware solution (FPGA) is necessary due to the high amount of switching performance needed.

The objective of the AE is to move a part of the functionality within the FlexNode PC software to an FPGA, whereby the PC will only control the FPGA for the purpose of switching the data streams to establish and the disconnect a (speech) call. The functionality integrated in the FPGA will be targeted at the last three functions of the list within section 5, namely:

- Switching of data packets and speech streams
- Multiplexing and de-multiplexing of data packets and speech streams
- Controlling the serial input/output devices (UARTs)

These functions require most of the CPU performance, whereas the level of complexity of the operations is relatively low. By removing these tasks from the CPU, the PC software is able to dedicate more time to the other tasks.

In addition to the switching, routing and multiplexing/demultiplexing functionality, the FPGA solution will also offer a convenient interface for DSP and/or microcontroller devices. This also allows the integration of the FPGA on an extension board with a specific function, such as the SCB (Speech Compression Board). The switching capability of the FPGA even allows Rohill to replace all of the switching functionality of the MDTS, offering even higher savings for building complete systems.

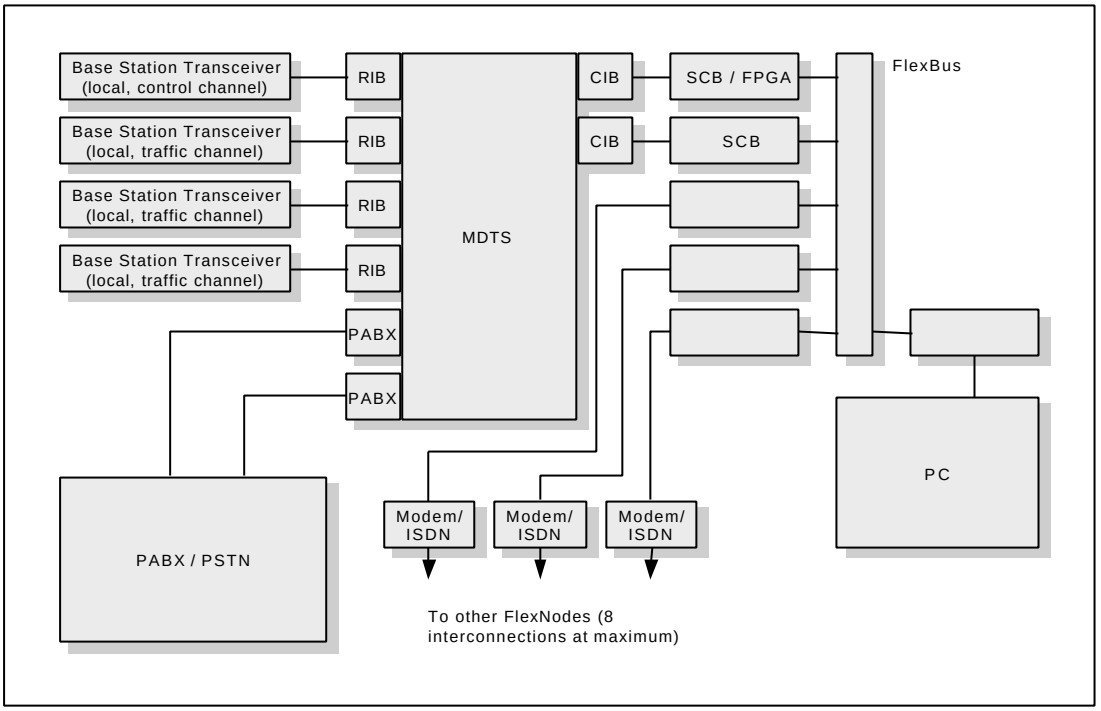
Using the FPGA solution, with 13,000 gates capacity will increase to an interconnection capacity of one MDTS and at maximum eight interconnection lines to other nodes. The bandwidth per interconnection line is specified at 128 kbps (12 speech and 4 data channels). This FPGA based solution will be marketed under the TetraNode brand name. A comparison of both solutions is shown below:

Solution	**FlexNode (PC based)**	**TetraNode (FPGA based)**
Number of interconnections to other nodes	3	8
Maximum bandwidth per interconnection	32 kbps	128 kbps
Equivalent speech / data capacity per interconnection	3 speech + 1 data	12 speech + 4 data
Maximum number of nodes	5	1.020

In the current generation of FlexNode the total number of sites, i.e. places to place an antenna to cover an area, is limited to 24 sites. In the new generation, named FlexNode TetraNode, the maximum number of sites is 8160, which is almost unlimited. Also the capacity of the speech channels per line is considerably higher with the TetraNode. This makes the realisation of networks with a large regional or national coverage possible, something that is impossible with the current FlexNode system.

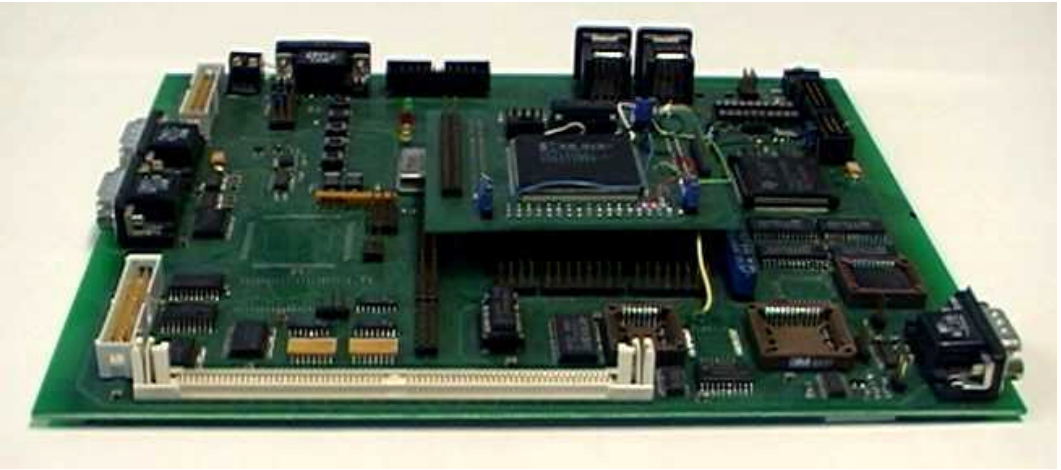
Note that also within a TetraNode system a PC is still necessary for general tasks such as database queries and updates, implementation of communication protocol layers, and controlling the FPGAs. The benefit of using the FPGA is based on the higher number of interconnections, higher bandwidth per

connection, and the reduction of CPU power needed, which then becomes available for general tasks. A block diagram of a single TetraNode site is shown below:



The above block diagram shows a small configuration of a single TetraNode site. Also this site is equipped with four radio channels, of which one is dedicated for the control channel signalling (call set-up, registration, etc), and three for speech traffic.

The cost advantage is not visible in this configuration. However, when using more than 3 interconnections to other nodes, the old FlexNode concept cannot be used due to the performance constraints of the CPU within the PC.



Prototype of the new FlexNode

The prototype board contains beside the Xilinx 4036EX FPGA, a C50 DSP from Texas Instruments, an Intel/Philips 8051 controller, and an Intel 386EX controller, which will be optional in the definitive product.

Compared to competitive products, the improved product based on the TetraNode switching and routing concept will have the following benefits:

- Flat hierarchy of the TetraNode network: no need for central switching equipment as in any of the competing systems, therefore increasing system reliability and decreasing system cost.
- Reduction of leased-line cost: the operational cost will be cut by the multiplexing capability of several speech and data streams via a single analogue modem or digital ISDN link.
- Inherent redundancy and capacity when using a meshed topology network: alternative routes for data and speech streams are available if a leased-line is down or overloaded.

The TetraNode concept allows Rohill to offer a comprehensive solution for medium to large-scale projects. In these projects, the price per radio channel is of less importance compared to small-scale projects; therefore the margin will be improved as well.

The significant reduction of leased-line costs will be an important consideration for operators to allow reduction of the operational costs. This benefit is not available in any competing system.

Finally, the compatibility with the emerging TETRA standard will benefit those operators who do not want to invest in costly TETRA technology today, while still having the option to upgrade to full TETRA functionality in the near future.

7. Choices and rationale for the selected technologies, tools and methodologies

The general requirements can be listed as follows:

- Must include all the logic for performing the tasks for switching, routing, multiplexing, de-multiplexing, bus management etc, as discussed in the previous section.
- Low system cost.
- Low power consumption.

A number of different hardware solutions were considered. A design using only standard logic components would meet the specification but the size of the circuit boards, the system reliability, and production cost will not be acceptable for series production.

Thus FPGA or ASIC techniques were considered as the only feasible solutions.

Initially it was proposed that for a prototype the FPGA technology would be used and an ASIC designed for the final device.

Xilinx had been chosen as the manufacturer of the FPGAs. Xilinx was preferred because of the fact that they offered the FPGA devices needed for the project, a sufficient growth path was offered, and the good reputation of the company in this market. The final selection of the specific SRAM FPGA device was made during the development process. This offered ease of prototyping but poor security. Thus, in order to protect their intellectual property Rohill are considering moving an antifuse FPGA for production. This will stop copying of their design and will be relatively easy since the software is not vendor specific and the design is in behavioural VHDL.

Within the time constraints of the AE project, the path (design flow) to realise an ASIC was also investigated. For the design of an ASIC several target technologies and manufacturers are available. For the transformation of the design from the finalised VHDL behavioural model to the layout of the ASIC, as required by an ASIC foundry, a design house should participate in this part of the process.

Two different types of ASIC's, the gate array and the standard cell array, were reviewed. The choice for a technology / manufacturer was left to the design-house. Only after a number of meetings with

representatives of design-houses and distributors was there sufficient understanding of the economical and technological aspects of the different technologies available.

A standard cell ASIC is not economically realisable because of the high initial costs and the large quantities (> 10.000 pieces) per year. This kind of yearly amount of devices will not be reached within a reasonable period.

A gate array was the best choice for an ASIC device for this design. For this gate-array our distributor of the FPGA's has made a quotation for the transformation of an FPGA design to a gate-array ASIC.

The initial RNE costs (Non REUROrring Expenses) were US$ 35.000 and a price per FPGA device of US$ 19,50 to 22,00 (at a batch of 10.000 pieces). Considering the costs per device of US$ 123,00 to 193,00 (at a batch of 10.000 pieces) the break-even point would be approximately 200 to 340 devices. The distributor of the Xilinx FPGA's (Rodelco) did expect that the price per device (Xilinx 4000XL series) would drop to approximately 20% of the current price-level within 2 years. The break-even point then becomes out of reach.

Therefore, the break-even point with the gate array ASIC had to be reached within one year in order to be economical more attractive than an FPGA solution.

In the current production planning a production capacity of 300 radio channels and 50 interfaces to PABX and PSTN is foreseen, which result in a total capacity of 350 devices. Thus, due to the expected required quantities per year an FPGA device is now, at the end of the development course, considered to be the right choice for the required design. A gate array ASIC is the best choice when the required quantity will increase or the price level of the FPGA's will not drop as expected.

VHDL was chosen for the development methodology of the required functionality of the target device. Other development methodologies, schematic entry or Verilog, as an alternative hardware description language, were reviewed but not considered as the best solution. VHDL as an international standard, not bound towards one or more manufacturers, was considered to be the best choice for designing complex digital designs.

Once having decided to produce designs for FPGAs and possibly an ASIC, a number of CAE tools are required for development of the design. CAE tools are required for data entry, simulation, synthesis and FPGA fitting.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

The expertise of the company is focused on systems engineering within the market of professional mobile communications. Several projects have been completed for domestic and export customers. These projects include conventional radio systems, trunked mobile radios and hand portables with customer-specified software, and standard as well as custom-defined trunked mobile radio systems. Projects have been delivered to public bus companies, utilities including water and electricity companies, airport authorities, police and fire brigade, and other applications.

The expertise of the R&D department is focused on software development (around 70% of the engineers are specialised in software development). The programming languages used include C and C++, Pascal, PL/M (for embedded 8051 applications), 8051 assembly and Occam (computer language for parallel programming, especially suited for the transputer). No expertise is available in the field of DSPs.

For hardware development, two engineers are responsible for designing, realising and testing PCB's for mostly combined digital and analogue circuitry. These PCBs contain normally a microprocessor, memory devices and peripheral circuitry, as well as analogue components (opamps, specific ICs) and

mixed analogue/digital devices such as modem ICs. The expertise is targeted here at the development and integration of controller modules with available RF modules.

The expertise in the RF field is low. No expertise was available for technologies such as FPGA's, gate arrays and custom-cell ASIC's.

Three people were involved in the project:

- Telecommunication Engineer, technical college,: project management
- Hardware Design Engineer, technical college,: specs, design and simulation
- Software Design Engineer, technical college,: test of FPGA design and prototype PCB

9. Workplan and rationale

The original workplan was based on the development of an FPGA that would be converted into an ASIC (gate-array), because this would be the best economic solution with respect to the expected number of devices needed. Due to changes in the market situation and the company objectives, this original plan had to be adjusted during the course of the product development and the final solution was FPGA based.

There was no subcontractor involved except for the support that was given by the supplier of the CAD tools and the ASIC foundry service. The acquisition of knowledge was based on training in VHDL and on CAD tool and by self-study and practical experience.

The original planning reflects the amount of work and time to realise the design and several tasks were scheduled in parallel. It did not allow any time for solving problems, and there was no contingency plan.

WP1 Project Management

The project was planned by Rohill to be run in a similar way to their internal development projects. Two days per month was allocated for project management and for reporting and dissemination. In practice slightly less than 2 days per month were required.

WP 2 Specification

The specification was planned to run for 3 months and require 26 days of effort. In practice it took 10 months and required 45 days effort. The major reasons for this change was that 4 months into the programme the market potential changed significantly. A 2 month hold was put into the programme whilst the company redefined their overall strategy and decided which product developments to pursue. The outcome was that this AE should be pursued but with an FPGA solution, which meant redefining the specification.

WP3 Training

Rohill had decided not to obtain any formal training, but train their staff using tutorials and other training material that was readily available on VHDL and FPGA design. Training, which included learning how to use the VHDL synthesis and simulation tools, was planned to be completed in month 2, excluding the evaluation of CAD vendors, and take 17 man days of effort. However, Rohill found that the task was significantly harder than anticipated, took 60 man days of effort, and was not completed until month 11. Part of the problem was due to bugs in the software which were harder to find with no previous knowledge of the tools. They also meant that training had to be redone using the corrected software tools.

WP4 Design

The design work, which included the VHDL entry model, simulation and final design, was due to run from month 4 to 15 and take 169 days of effort. In practice the task started much later than planned in month 10 but was completed in 5 months. However it took 210 days of effort. The additional effort was justified on the grounds of the errors with the software tools and their inexperience in being able to work around the problems.

During the synthesis and simulation phase, a number of problems and drawbacks were experienced.

- A problem with the tri-state outputs of the device was solved with a specific script gained from the distributor of the synthesis tool. The latest version of the tool has this script build in.
- With the previous version of the tool, a simulation of the final synthesis results was not possible. The result could only be tested after back-annotation by the Xilinx place & route tool. The tool lacked the possibility to simulate the synthesised results when ported to the selected FPGA family.

This process took a long time and all hierarchy was lost. Faultfinding became almost impossible. More than two months passed before the latest version of the synthesis tool arrived, in which these problems were solved and that was capable of simulating the final synthesis results. Finally a sound VHDL model could be constructed. With this release VHDL constructs that were not supported by the Xilinx technology could be spotted.

A performance analysis could only be performed after a successful back-annotation of the FPGA design was completed. Afterwards it was obvious that a fit of the design into the FPGA and performing the performance analysis, before testing the back-annotated results as planned, could never be successful.

For the 'place and route' phase the Xilinx step 6 was bought. Once installed, the tool didn't support the chosen device. None of the devices supported by the step 6 version were capable of fitting the design. Only after installing a temporary beta update version of the new tool could the work be started. Several problems were experienced, that could only be solved after installing several bug-fixes. The final version that worked properly arrived after several months.

In summary, although the design work was finished on time, this was largely due to a concerted effort from Rohill personnel together with the deletion of the task to produce an ASIC.

WP5 Evaluation

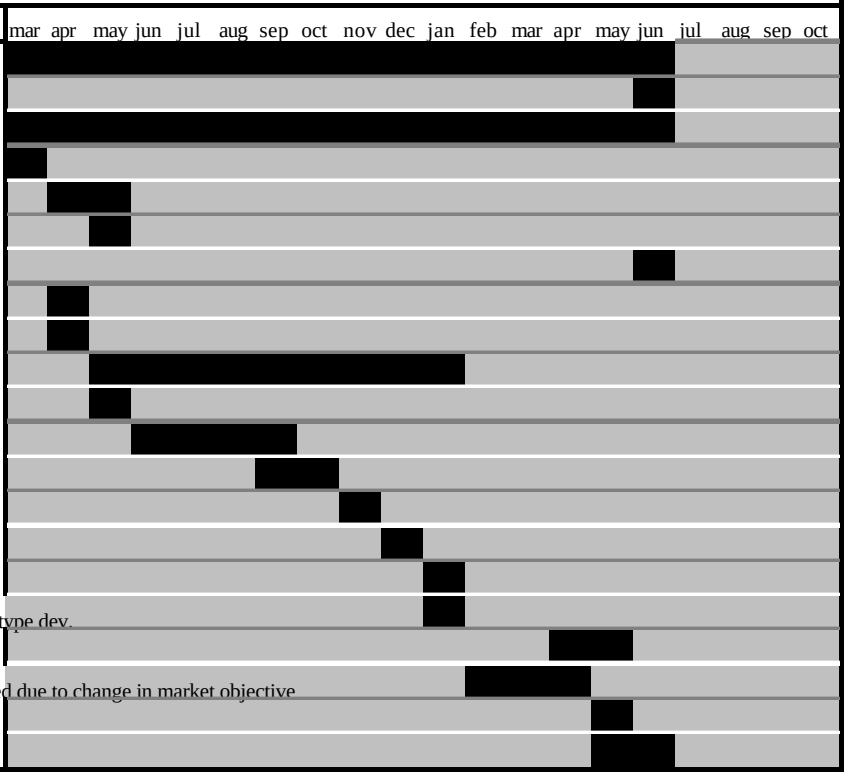
The PCB with the FPGA, rather than the originally planned ASIC, was produced and tested. This took 2 months as planned and was completed on time at the end of month 16. The final prototype functioned as planned.

Summary

The project, excluding reporting and dissemination activities, was completed in the 16 months as planned. The effort spent was however considerably higher than planned due primarily to changes in strategy, an underestimation of the time to learn VHDL and design an FPGA, and errors in the software tools. Hence, the cost of the internal resources were less than planned, and the ASIC was not produced. Hence the overall cost was less than originally planned at 97 K EURO rather than 117K EURO.

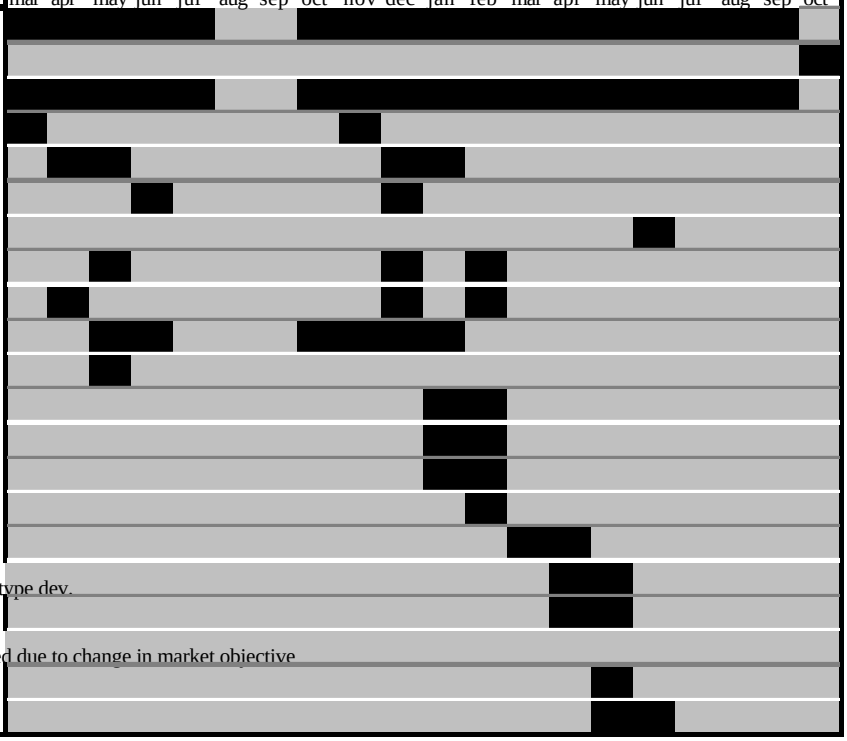
ORIGINAL PLANNING

WP	Task
1	Project management
1	Dissemination
1	Reporting
2	Functional specification
2	Detailed specification
2	Finalize and approve
2	Update specification
3	VHDL training
3	CAD SW training
3	Evaluations CAD vendors
4	Purchase/intallation CAD SW
4	Entry VHDL model
4	Simulation model
4	Simulation of design
4	Prepare prototype dev.
4	Testing prototype dev.
4	Finalise ASIC design -> finalise protype dev.
4	Create PCB design
5	Manufacture ASICs -> task cancelled due to change in market objective
5	Prepare PCB's
5	Testing of product



REALISED WORKPLAN

WP	Task
1	Project management
1	Dissemination
1	Reporting
2	Functional specification
2	Detailed specification
2	Finalize and approve
2	Update specification
3	VHDL training
3	CAD SW training
3	Meeting/evaluations
4	Purchase/intallation CAD SW
4	Entry VHDL model
4	Simulation VHDL model
4	Simulation of design
4	Prepare prototype dev.
4	Testing prototype dev.
4	Finalise ASIC design -> finalise protype dev.
4	Create PCB design
5	Manufacture ASICs -> task cancelled due to change in market objective
5	Prepare PCB's
5	Testing of product



Planned		WP1 Management	WP2 Specification	WP3 Training	WP4 Design	WP5 Evaluation		Totals
Labour	(person days)	36	26	17	169	18		266
Personnel costs	(EURO)	10,944	7,904	5,168	51,376	5,472		80,864
Travel & subsistence	(EURO)	80		850	150	120		1,200
Subcontractors	(person days)							0
Subcontractors costs	(EURO)							0
Equipment	(EURO)			480	20,311			20,791
Consumables	(EURO)					1,200		1,200
Services	(EURO)			1,500	1,600	9,700		12,800
Totals	(EURO)	11,024	7,904	7,998	73,437	16,492		116,855

Actual								
Labour	(person days)	30	45	60	210	26		370
Personnel costs	(EURO)	9,494	7,239	9,615	33,693	3,068		63,108
Travel & subsistence	(EURO)	119	0	138	0	0		257
Subcontractors	(person days)	0	0	1	0	0		1
Subcontractors costs	(EURO)	0	0	115	0	0		115
Equipment	(EURO)	0	0	0	0	0		0
Consumables	(EURO)	0	0	127	26,998	2,241		29,367
Services	(EURO)	0	0	0	0	3,819		3,819
Totals	(EURO)	9,613	7,239	9,995	60,691	9,128		96,666

10. Subcontractor information

No third-party consultancy was considered due to the fact that in the past Rohill always managed to get experienced with new programming languages using self-study and using a development suite (compiler, debugger) only. To compensate for the lack of VHDL knowledge, Rohill planned to perform self-study of VHDL and to perform hands-on training using a low-cost VHDL development tool, to be purchased at the start of the project.

However, on the advice of the TTN, Rohill did include a training course for getting familiar with the basics of VHDL more quickly.

There were however, effectively two sub contractors plus the TTN, who guided the Rohill through the AE. Neither were paid specifically as a sub contractor but received their funding in either a leased plus maintenance contract or selling the hardware. As a result there were no contracts with either of them.

Sub Contractor 1 CAE vendor helpdesk and consultancy

The "helpdesks" of the vendors of the CAE tools were used for guidance and problem hunting during the design process.

The vendor of the tools for design entry, simulation and synthesis offered this support when subscribed to a 'maintenance contract'. The yearly costs for this maintenance contract are considerable for which the subscriber automatically receives major updates of the products. Assistance is offered at solving problems with the products and a work-around, if available, will be offered. This service also has been (mis)used for gaining help at guidance through the design flow. For services beyond the scope of this

'maintenance contract' the vendor offers services on consultancy basis. This service has also been used during the construction (design entry) phase of the project for reviewing the VHDL code and to get advice on how to improve the VHDL design.

Sub Contractor 2 Xilinx - FPGA vendor

Xilinx, the manufacturer of the tool for fitting the design into the FPGA offers such a service free and on a world-wide scale. This is because the major interest of this manufacturer lies at selling devices rather than selling CAE tools. Xilinx helpdesks in the UK and Belgium/France have been contacted. These helpdesks act as knowledge centres and are more capable of solving complex problems with the CAE tool than the vendor of the products in the Netherlands is.

It turned out that most of the assistance from both the CAE vendor and the FPGA supplier was related to problems in the software. Rohill found several inconsistencies in the operation of the software, which could be corrected only by an update of the software.

11. Barriers perceived by the company in the first use of the AE technology

Prior to the AE, Rohill had not adopted the digital hardware technologies used in this AE for the following reasons:

VHDL Knowledge

No knowledge of VHDL was available in the company. It was clear that the use of VHDL is essential for successful creating FPGA and/or ASIC designs. Learning VHDL would require a substantial investment, without any practical results (read: product) at the end of the learning course.

Choice of CAE tools

The investment in CAE development tools was considered to be too expensive, and could not be justified on basis of a reduction of the time-to-market of the products to be developed. Also, Rohill was barely able to evaluate the available CAE tools due to the lack of expertise.

Lack of expertise in digital electronics

The expertise in Rohill was more directed at software development and the use of standard hardware solutions (e.g. using the PC hardware platform). The method of improving hardware designs by using highly integrated hardware devices such as FPGA's and ASIC's were perceived as 'inflexible'.

Perceived lack of flexibility in hardware design

Also related to the above, the 'specification phase' of the development of a product is frequently considered by the engineers and sales/marketing personnel as an obstacle for flexibility during the project exEUROtion. The fast changing market conditions demand lots of last-minute changes to products under development, which can be implemented easily in software. However, when designing FPGA/ASIC devices, these last minute changes were considered as 'very difficult' to implement.

12. Steps taken to overcome the barriers and arrive at an improved product

Due to the perception that it would be possible to perform all the work themselves, Rohill did not study the subcontracting option in detail. This meant that they were limited in the methods that they could use to overcome the barriers.

Lack of VHDL knowledge

At the start of the AE, no knowledge of VHDL was available. To get familiar with the VHDL language, a number of tutorial books and a CD ROM training were purchased and used during the first phase of the project.

The next step was training on the job. A small, low-cost, toolkit (the Xilinx foundation entry toolkit) was bought and installed on the computer. Using this low-cost development tool, Rohill could delay the substantial investment in the full suite of development tools. After getting familiar with the tooling, a number of small designs were build. While using this toolkit, Rohill realised that only the use of a subset of VHDL was allowed. This limited the use of certain constructs. Due to the lack of training, often VHDL constructs were used which were not sufficiently supported by the tool which sometimes resulted in an erroneous result without any warning.

Selection of CAE tools

Before purchasing CAE tools, these tools had to be investigated and the right tools had to be selected. It appeared to be an unforeseen barrier to use the tools without instruction from the supplier. Support in using the tools was only available in a form of a help desk.

Expertise in digital design

At the start of the project the knowledge of FPGAs and ASICs was not sufficient. Getting familiar with FPGAs was accomplished by studying tutorial books and data sheets. For guidance through the design flow only the manuals and reference book of the CAE tools were available for reference, and these did not include a step-by-step guide. Therefore Rohill relied heavily on the support from the vendor of these tools. When constructing the behavioural VHDL model and the test-bench, a methodology had to be found out for the building of these blocks.

The path (design flow) to realise an ASIC was also investigated. In the process of selection a technology for the ASIC design a number of design-houses were approached. Two of them were invited to make a quotation of the final design of the ASIC, but due to the fact that the FPGA design was not complete, and the projected numbers were low, both of them were not prepared to quote. Hence the ASIC work was limited to acquiring knowledge as to what different ASIC technologies would be suitable for this digital application.

Flexibility in hardware design

After investigating the number of available FPGA technologies from data books, it was decided that the choice of the final FPGA would be taken during the development process. Rohill did not investigate the possibility of modifying the functionality of the system by reprogramming the FPGA once the FPGA was operational.

13. Knowledge and experience acquired

After completing the project a lot of technical knowledge and experience has been acquired. The most significant issues are mentioned in the overview below:

FPGA Design

During the construction of the design, using the chosen toolkit and with the support offered by the supplier, Rohill has learnt how to produce a complete digital design. This includes hierarchical entry, design simulation, cost effective VHDL entry (using as few resources as possible) and using VHDL coding styles and methodologies. In this process it became apparent what good VHDL programming practice is and what is not.

FPGA Selection

The selected FPGA is capable of incorporating RAM in the design. In this design Rohill wished to use a small part of the device for this purpose. However, in order to achieve this the required library part had to be available. After intensive contacts with the support centre of XILINX in England, Rohill were able to install the required library part into the design.

Consideration of using gate-array or custom-cell ASICs

The path (design flow) to realise an ASIC was also investigated. In the process of selection a technology for the ASIC design a number of design-houses were approached. Two of them were invited to make a quotation of the final design of the ASIC, but due to the fact that the FPGA design was not complete, and the projected numbers were low, both of them were not prepared to quote. Hence the ASIC work was limited to acquiring knowledge as to what different ASIC designs could be produced.

Rohill also learnt that both technical and economical risks are present. The technical risks were discussed with ASIC suppliers before a fully functional FPGA prototype was available and Rohill personnel gained an understanding of what these were. Knowledge regarding the economic risks was also obtained. It became clear during the project that the major barrier in moving from a FPGA to an ASIC was related to costs. During the AE Rohill learnt how to work out the ROI for an FPGA and ASIC solution and from this determined that with the modified projected sales forecast the most cost effective solution was to remain with an FPGA.

14. Lessons learned

The lessons learned during the project are mainly related to technical matters. A list of the issues are shown in the following list:

- When introducing a new technology, sufficient man-hours should be allocated for correcting design errors. This was not the case in this AE.
- It is now clear that during the design of a printed circuit board, the choice of signals to the pinning of the FPGA has a great impact on the results of the final FPGA. It became obvious that a bad choice could result in a design that will use a device with double price, or is not realisable at all.
- Time and budget should be available for joining courses and for consultancy for learning the involved techniques. It is more time-effective to join focused courses than using a trial and error method. Rohill underestimated this aspect, and tried to learn about VHDL, FPGA and ASICs primarily from published data.
- Introducing a new technique the process should be guided by experts in this field. The realisation of the first design should have been guided from start to finish. It is wise to gain knowledge and skills for this process; it is not wise to try to do this without help. Training and/or consultancy should be present for learning VHDL language, design entry with VHDL, synthesis and simulation, place and route with a hands-on training.
- Although VHDL is presented as a universal design tool, we have experienced than each manufacturer has it's own preferences. Even the choice of target device (FPGA) has impact on the style of writing VHDL. This means that portability from one target device to another or from one CAE tool to another can cause problems and may require adjustments towards the design.
- The CAE tools required are very sophisticated. Only after months of use, drawbacks, omissions, and errors become apparent. Investing money in these tools is only sensible with a guarantee or help from the manufacturer to obtain proper results.

- In order to adhere to the project schedule, the printed circuit board was designed and a FPGA was selected in a stage where the VHDL design was not finalised. This was an error in judgement since once the VHDL design was finalised the required size for the FPGA had to be increased. This caused several difficulties at the process of fitting the design into the FPGA, and demonstrated that hardware choice and PCB layout should not be finalised until the design is fully complete.

15. Resulting product, its industrialisation and internal replication

The resulting product from this AE has provided Rohill with a digital component, which is essential for medium to large-scale trunked radio systems. This will enable Rohill to sell the highly optimised TetraNode solution into markets which were previously inaccessible to them.

The final development of functionality will be done in small steps. Especially the software development still requires a large amount of man-hours for the complete system implementation. By implementing and testing the software as application modules on a single PC based platform, Rohill can release the first operating software within 12 months. The full investment for realising TetraNode (limited functionality, but related to the expected sales volume) will be around 500 K EURO, from which 97 K EURO is financed by the FUSE programme. The other cost (403 K EURO) is related to additional software and hardware development for full integration of the AE ASIC into the TetraNode system.

The hardware will be easier to manufacture and maintain than the existing software solution and the complexity and number of different components will decrease. Rohill will use the same subcontractors for volume production as before.

The skills acquired in the AE are mainly related to the use of VHDL and the methods to perform the steps for realising a FPGA device. Rohill will use FPGA technology in other modules within the system concept as well, e.g. to reduce the number of standard logic components and/or to increase the hardware flexibility. Rohill already planned to use the VHDL skills for designing and testing PAL/GAL devices within microcontroller systems. These new projects also allow Rohill to maintain the skills for future projects, and increase their knowledge to improve other products as well.

If volumes for production increase significantly, Rohill will be able to reconsider the option of using gate-array or standard-cell technology. The initial steps were already performed, so there is an understanding of the cost and duration involved.

Concerning the IPR, Rohill has started the patent application procedure for two concepts used within the overall system. Although it is not directly related to the FPGA/ASIC design, it will protect the company from competition using the same hardware and software concepts in the mobile radio market.

16. Economic impact and improvement in competitive position

The improvements in the competitive position are most visible in the capability to offer trunked radio systems for medium to large sized projects which was not previously accessible to Rohill.

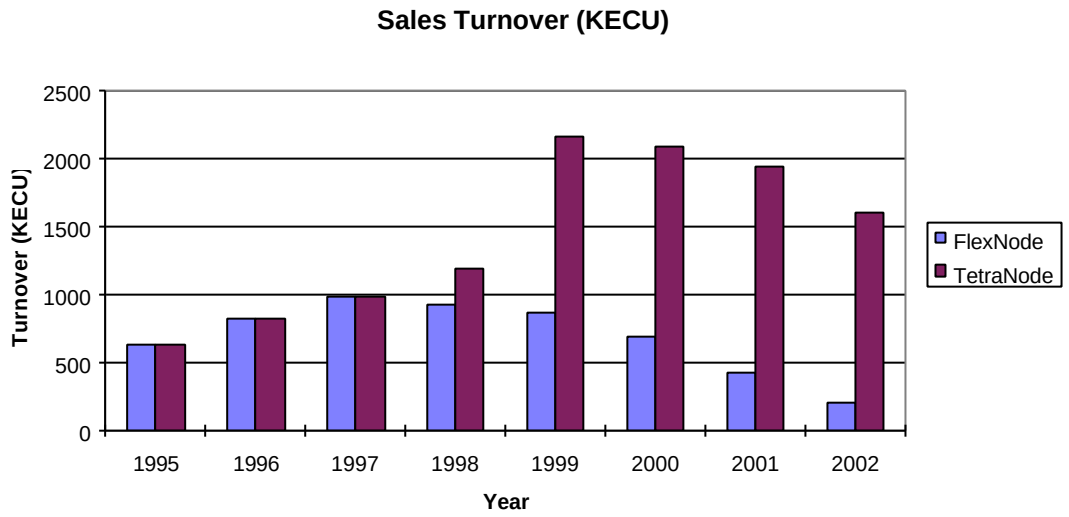
Also the advantages of the TetraNode concept, as listed before, are attractive for operators due to the lower operational costs. These advantages were available in the current FlexNode concept, and will now also become available for larger systems. For example, the need for a smaller number of leased-lines is of particular interest for countries where the fixed-line infrastructure is not well developed, such as India and China. These countries are also the high growth markets for trunked radio systems.

The economic arguments to justify the AE and the introduction of the related technology in the company are therefore most significant in the increased market size. The optimised unit cost will be of less importance, and will not appear in smaller sized systems.

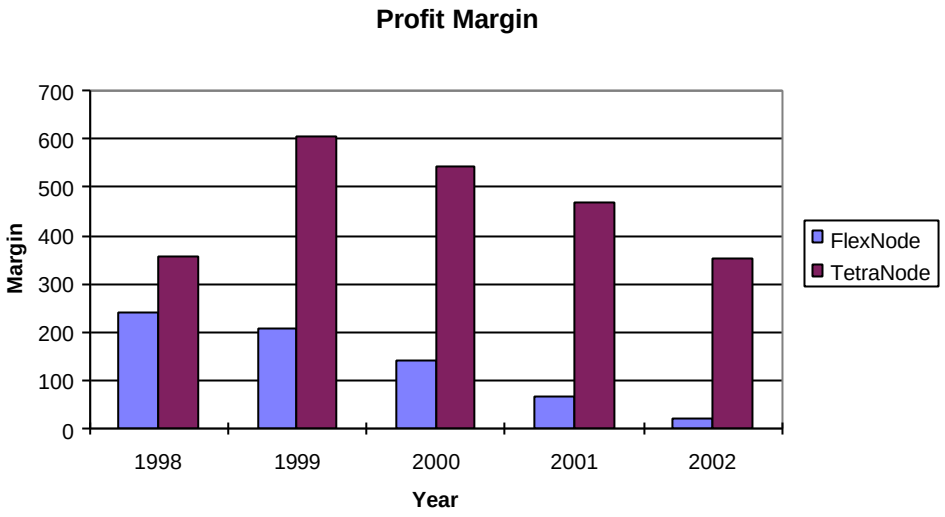
Past and projected sales figures are shown in Section 4. The introduction of the TetraNode concept using the FPGA will increase the sales volume significantly, whereby the option of using the FlexNode concept only will show a slow decline from the current year. The decline in sales from the year 2001 is mainly caused by the introduction of full digital trunked radio systems, whereby the speech is also digitally transferred via the radio path. TETRA is the main standard for these digital trunked radio systems.

The TetraNode concept is prepared for this future standard, so new generations of (mainly software based) products will compensate the declining sales of the current products. Existing operators/customers using TetraNode products will also be able to upgrade to full TETRA functionality without the need to replace all hardware.

Note that the TetraNode sales figures shown will replace the FlexNode sales from the year 1998. However, for small systems it will be still possible to utilise the FlexNode product range in the future. In terms of sales volume, the following forecast is expected:



The turnover will decrease slightly if compared to the sales volume (in number of channels). This is caused by a decrease of the price per channel from 7.000 K EURO at present to 5.000 K EURO in the year 2002.



The graph above shows the expected profit margin in the future, both when considering FlexNode alone (no AE) and when introducing TetraNode (using the AE).

It is obvious that the improved turnover and margins, provided by the AE, creates a much better competitive position compared to the situation without the investment in TetraNode.

The Return of Investment can be easily determined on basis of the graphs. Considering the FUSE investment of 110 K EURO, the investment will be paid back in one year. Assuming a 5 year product life cycle the ROI will be 16 times the initial investment.

17. Target audience for dissemination throughout Europe

This AE describes how an SME with 25 employees developed a digital product using FPGA technology for trunked radio systems, using VHDL as a development tool. This replaced an existing software solution which was limited in the application, and hence has enabled the FU to extend their market potential. The FU originally intended to develop an FPGA for the prototype and then produce an ASIC for production volumes. However, during the AE the market changed, and the number of units had to be significantly reduced. As a result it was no longer financially viable to develop an ASIC and the FU remained with the FPGA for the production unit. Best Practice was followed in that the economic aspects were reconsidered before making the final commitment to developing an ASIC.

The FU chose to follow the self taught route, which meant that the sub contractors were the suppliers of the software and hardware. Although thought to be adequate at the start of the AE, the FU realised during the project that they would have learnt more, and gained more knowledge, if they had used a sub contractor who was expert in FPGA design using VHDL to guide them through the design process.

Regarding the technology developed the replication value of the AE is particular high for companies which are interested in spin-off applications, such as the interconnection of PABX's using a similar solution as presented here. These companies operate in different markets (fixed-line telecommunications), and will not compete directly.

The knowledge gained in overcoming difficulties in the individual development phases will benefit in particular those companies that intend to use the same CAE software (Exemplar Logic's Leonardo)

and FPGA devices (Xilinx). Companies with similar levels of management and technology skills will probably make similar mistakes as Rohill did.

Rohill does not think that the scale of this project will be a problem for any company with a size similar or larger as their organisation.

ProCom	Industry
3002	Computers and other information processing equipment: Companies involved in the development of small series of special computer related equipment.
3220	Telegraph and Telephone Apparatus and Equipment and Radio and Electronic goods: Companies interested in spin-off applications, such as the interconnection of PABX's
3320	Instruments & Appliances for measuring, checking, testing etc.: Companies who develop systems and equipment for professional use.

Target audience according to ProdCom codes