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FUSE Application Experiment EPC1 2219

Monitoring TTN: IAM F&E GmbH, Braunschweig, Germany

Interface Device For PLC Signal Modules

Gate-Array-ASIC achieves a cost saving up to 30%.

Abstract

VIPA offers a wide range of supplementary components for several automation systems like the SIMATIC S5 and S7 series as well as its own modular PLC system. The supplementary products are hardware-components like memory modules, I/O modules, communication processors, central processing and interface units as well as software-tools for programming, parameterizing and controlling these hardware components. The company was founded in 1985 and has about 60 employees. VIPA's headquarter is located in Erlangen (Germany) and the company is represented in over 25 countries worldwide.

The objective of the Application Experiment was to replace several FPGAs used as interface devices on the intelligent I/O modules of VIPA's PLC system by a common Gate-Array-ASIC.

The master module of the PLC system and its slave peripheral modules are connected by a back plane bus system. The communication between the modules is based on a synchronous, serial protocol handled by hardware interface devices. The requirements for a general purpose device which could be used on all intelligent I/O modules were specified and implemented as a Gate-Array. In addition to the pure Gate-Array design flow a rapid prototyping was done with a FPGA prototyping board. The FPGA prototype offered the ability to perform an in-system verification of the entire design as well as a hardware/software co-design before the Gate-Array prototypes were available. VIPA did all the steps of the Gate-Array development, except the layout of the device, by itself. The entire design process was based on VHDL.

The integration of several functions on a common Gate-Array helped to improve the system performance, increase the flexibility of the entire product and reduce the costs of the modules significantly. The maximum permissible data transfer rate on the back plane could be raised by 33% while the costs of the modules could be cut up to 30%. In addition the open concept of the design offers high flexibility and makes it possible to use the Gate-Array not only on the already existing modules but also on future modules with new or advanced features.

The acquisition of technical know-how from the AE permitted VIPA to improve its technical knowledge and this is a crucial factor in maintaining competitiveness in the world market. Project management experience in the field of microelectronic development was another important achievement of the AE. The project which was structured on a detailed work plan, a business plan, on technical tasks and a clear assignment of responsibility as well as interfacing with an unfamiliar technology has been good on-the-job training for the engineers and managers involved in the AE. Furthermore VIPA will permit full control of industrialisation phases subsequent to development activities. Therefore the AE achievements represent a step forward in the growth of the company and towards more competitiveness of its products.

The AE started in August 1997 and ended in July 1998. The overall costs of the AE were 90K €. As there were significant improvements and savings upon the former implementation of the

modules the payback-period should be less than two years and the estimated return-on-investment is about 500%. The lifetime of the product will be approximately five to seven years.

During the AE, VIPA as the First User gained a lot of knowledge in how to handle an entire ASIC-project from the specification to the test phase. Especially the experience in VHDL-coding, ASIC- and FPGA-synthesis and FPGA-prototyping could be considerably improved.

Keywords

Gate array, field bus, PLC module, FPGA prototyping, VHDL, RTL synthesis

FUSE-Signature

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2. Company size

The total number of employees is 60, with 12 involved in the electronic development (most of them engineers,). The company realized a turnover of about 18 Million DM (~ 9 Million €) in 1998. VIPA has been dealing with the development of electronic components for industrial applications since 1985. Most often the design entry was done by schematic entry even when using programmable logic. The verification of such PLD- and FPGA-designs was accomplished rather by in-system and field tests than by simulation. As there was a lack of knowledge regarding to VHDL and simulation as well as ASIC technology, VIPA decided to take part in the FUSE project in order to improve the knowledge of its employees and its position in the market.

3. Company business description

VIPA is a privately held company with sales subsidiaries and representatives in over 25 countries worldwide. Development, design, testing and support is exclusively done at the German headquarter in Erlangen while installation and maintenance is often carried out by service engineers of the subsidiaries or a subcontractor close to the customers' facilities. Manufacturing of the products is done by different subcontractors and external suppliers.

VIPA offers a wide range of supplementary components for several automation systems, industrial PCs and its own complete automation solutions like the high-modular PLC system called 'SYSTEM 200 V'. The supplementary products are hardware-components like memory modules, I/O modules, communication processors, central processing and interface units. Some of these products are special add-on parts which are not provided by the original vendor because of low sales or the necessity to use special equipment and manufacturing facilities. Other products are compatible to existing products but can be offered at a lower

price or including additional features. The software-tools can be used for programming, parameterizing and controlling the VIPA specific components as well as the most common fieldbusses and some vendor specific automation systems.

4. Company markets and competitive position at the start of the AE

VIPA is represented with its supplementary components and PLC systems in over 25 countries worldwide. The main focus in the complementary business is on accessories, add-on and special components for SIMATIC automation systems. Siemens held about 98% of this market. VIPA had a market share of approx. 1% in the field of SIMATIC®-compatible components and supplements worldwide and a market share of approx. 5-10% in Europe.

Since 1987 VIPA has changed step by step from a pure system integrator and supplier for add-on components to a system supplier with its own complete automation solutions. In 1995 VIPA introduced the SYSTEM 200V, a high-modular PLC system for small and medium industrial applications.

Application areas for the 'SYSTEM 200V' include:

- Special-purpose machines,
- Textile machines,
- Packaging machines,
- General mechanical and engineering applications,
- Control systems,
- Machine tools,
- Installation engineering,
- Electrical manufacturing industry and associated trades.

The system can be run as a stand-alone application as well as a part of a more complex visualisation and control system connected by a network or a standardized fieldbus system. The user can configure the system individually with any mix of expansion modules to meet the precise needs of the application, while saving unnecessary investment costs. Therefore it offers maximum flexibility and optimum adaptation to a wide range of different application areas.

Although there are several competitors in the area of small to medium sized automation systems SYSTEM 200V reached a market share of about 5% in Europe because it is small, fast, reliable and can be easily integrated into existing systems by using common fieldbusses. Moreover its about 10% cheaper than comparable products from other suppliers.

Most customers are using SYSTEM 200V components for automation purposes within their own manufacturing facilities. Beside these real end users there are also manufactures providing their entire machines with SYSTEM 200V components or system integrators installing SYSTEM 200V components besides other products.

The market trend in the field of automation technologies was denoted by a continuous growth of about 10..15% per year over the last years. The company participates in this common trend but was not able to increase its market share significantly. Therefore VIPA decided to further improve major components of the systems while decreasing unit costs and manufacturing costs. By improving major parts of the system the entire systems becomes more competitive. This will offer opportunities to realize a growth of VIPA's market share that is even higher than the common growth in the field of decentralized peripheral automation systems.

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5. Product to be improved and its industrial sector

VIPA's 'SYSTEM 200V' (Figure 1) is a high-modular PLC system and can be used as a centralized automation system or as a system with distributed I/Os. The current trend toward distributed structures is driven by their added flexibility, simplicity and cost-effectiveness. 'SYSTEM 200V' offers continuity to the user as it makes no distinction between centralized and distributed I/O. One software package is sufficient to handle hardware configuration, parameter assignment, testing and documentation for all components.

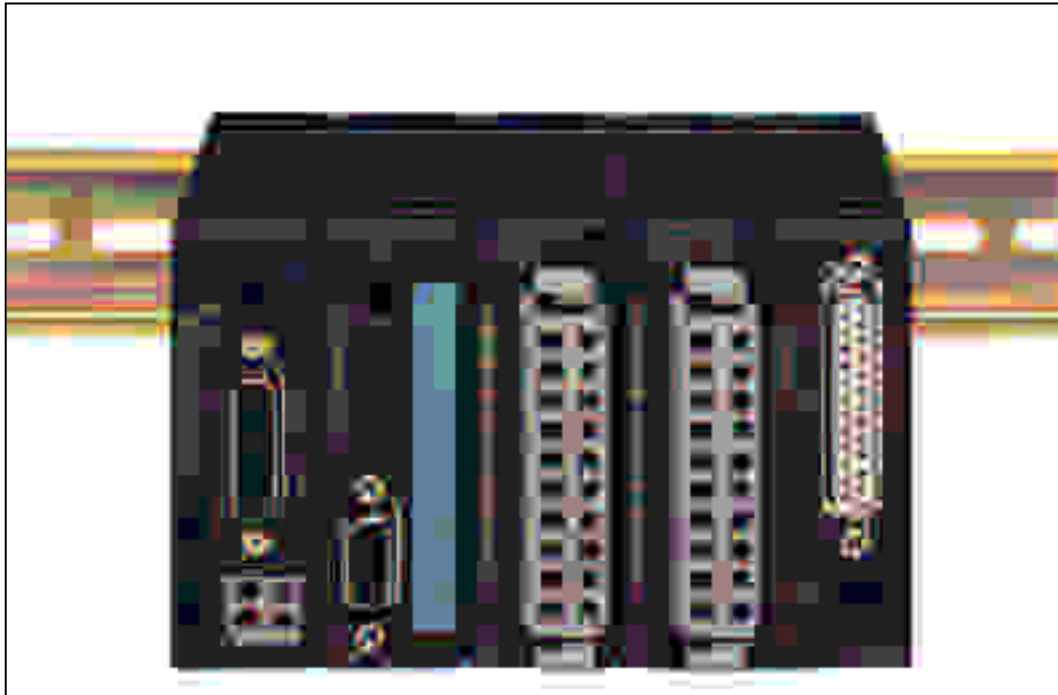


Figure 1 : Some examples of SYSTEM 200 V modules

Application areas for the 'SYSTEM 200V' include special-purpose machines, textile machines, packaging machines, general mechanical and engineering applications, control systems, machine tools, installation engineering, electrical manufacturing industry and associated trades.

The system can be run as a stand-alone application as well as a part of a more complex visualisation and control system connected by a network or a standardized fieldbus system. The user can configure the system individually with any mix of expansion modules to meet the precise needs of the application, while saving unnecessary investment costs. Therefore it offers maximum flexibility and optimum adaptation to a wide range of different application areas.

The CPU (centralized) or the fieldbus coupler (distributed I/Os) and the peripheral signal and function modules are connected by a back plane bus. The power-supply for the logic within the modules and the communication between the modules is done via this back plane bus. For this purpose VIPA created its own serial communication protocol which was handled by the interface devices on the modules. At the beginning there were individual FPGA- and PLD-



implementations for the different kinds of signal and function modules (Figure 2). Therefore it was necessary purchase and store several types of PLDs, FPGAs and PROMs and to maintain a lot of different designs and layouts although most of the intelligent I/O modules only differ slightly in function. Considering the points mentioned before and trying to reduce the space on the PCBs that is necessary for the interface devices, VIPA decided to start the development of a Gate-Array which can be used on all types of intelligent I/O modules. The open concept of the design offers high flexibility and makes it possible to use the Gate-Array not only on the already existing modules but also on future modules with new or advanced features.

Figure 2: Examples of modules using FPGAs as interface devices

With the AE it was planned to increase the maximum permissible communication rate on the back plane by 20% which will result in a higher overall system performance. The unit costs and the size of the interface device should be decreased by at least 30%.

6. Description of the technical product improvements

In order to support high-speed or time-critical applications it is necessary to achieve short cycle times between reading the process inputs, processing the incoming data and generating new output signals. Therefore it's very important to use an interface device that combines fast but also reliable operation under the worst operating conditions.

The bus interface device shall be used on all intelligent I/O modules of 'SYSTEM 200V' and on several types of function modules. Therefore it is desirable to have a low-cost interface device that supports any type of module mentioned before.

'SYSTEM 200V' is a high-modular automation system. The modules are very small and therefore it's useful to have an interface device that integrates more functions on less area.

The main objectives of the AE were:

- Increasing the overall system performance of the intelligent I/O modules while keeping a high reliability.
- Decreasing the unit costs for all types of intelligent I/O modules by using one interface device on all modules.
- Reducing the space needed on the PLCs for the interface device in order to get more intelligence on the single board.

All objectives could be reached by implementing the interface device as a Gate-Array-ASIC realized in a 1.0µm CMOS technology. The gate count of the device is 12K gates including 128 Bytes RAM. Supply voltage is 5V and the housing is a TQFP with 64 pins.

The maximum permissible data transfer rate on the back plane could be raised by 33% while the costs of the modules could be cut up to 30%. In addition, the open concept of the design (Figure 3) offers high flexibility and makes it possible to use the Gate-Array not only on the already existing modules but also on future modules with new or advanced features. As an example it's now possible to combine the functions of a 2-channel Analog Output module and a 2-channel Analog Input module on a single module.

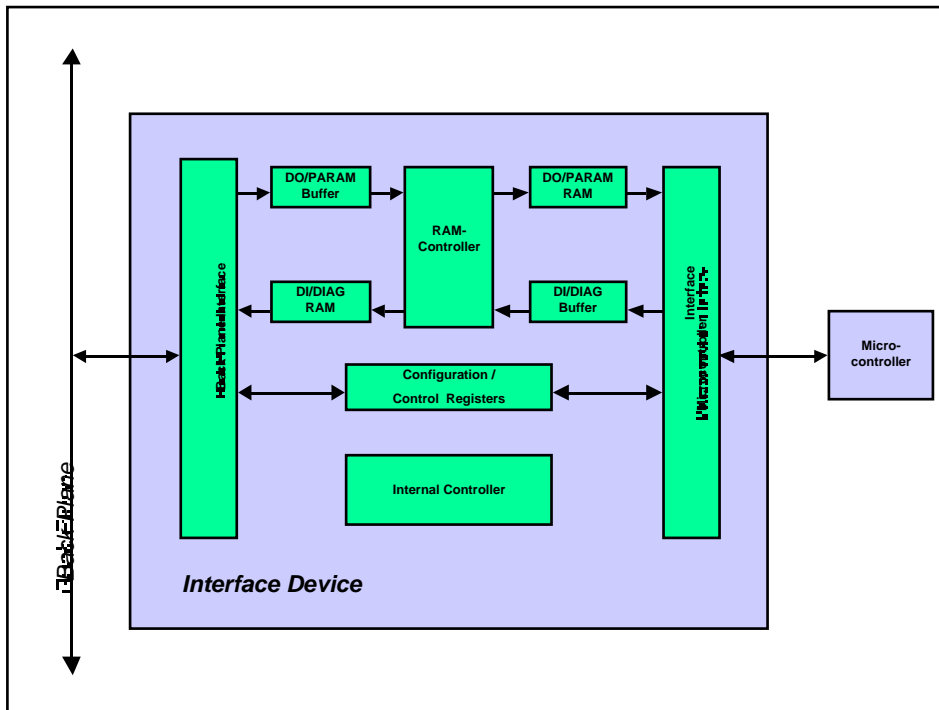
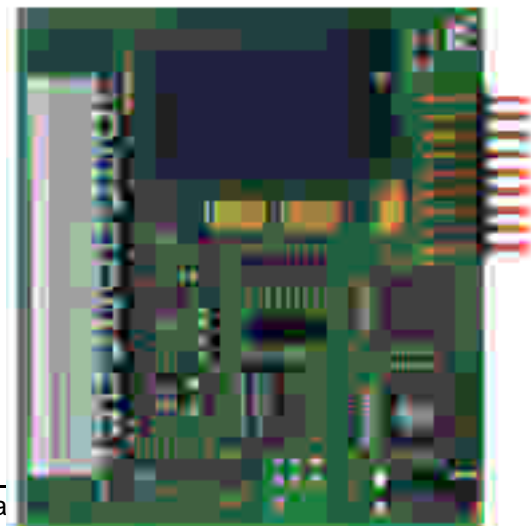


Figure 3 : Block diagram of the new interface device

Besides the pure technical improvements a common general purpose interface device also simplifies the administrative handling during development, production, test and support. A single library cell can be used for schematic entry and layout of the modules, only one device is to be purchased and stored, there's no need to create and carry out different test cases for several interface devices and it's much easier to support and maintain a single design than to have several different implementations.

The size of the interface device could also be reduced up to 65% (FPGA plus PROM vs. Gate-Array). Therefore it's now possible to integrate the same functions on less space or to have more functions on the same PCB. An example is given in Figure 4. On the left side is a 4-channel Analog Output module using a FPGA as the interface device. Four smaller additional PCBs (at a right angle to the base PCB) were necessary to implement this function into a single module. The module on the right side is using the new interface Gate-Array. Due to the smaller size of the device and some other improvements additional PCBs are no longer necessary.



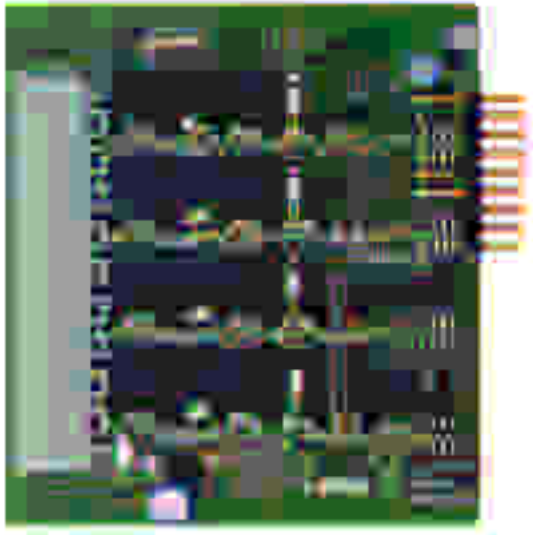


Figure 4 : Analog Output module with FPGA (left) and Gate-Array (right)

7. Choices and rational for the selected technologies, tools and methodologies

There were several things to be considered when VIPA decided to design the interface device for the 'SYSTEM 200V' signal modules:

There are several technological possibilities to implement the device. Basic technology is using PCB with standard components. This approach usually has moderate design effort and costs, but using only standard components, size constraints could not be met. Therefore, integration of several functions into a single integrated circuit was required.

The first decision with respect to integrated circuits was whether to keep using FPGAs for this kind of application or to take the risk of an ASIC or multi chip module (MCM) development. A FPGA design could have been done in less time and with less additional support from outside. There were several disadvantages of a FPGA (unit costs, performance, size) which could not compete with an ASIC solution in the end. MCM did not offer technological advantages, mainly size, over an ASIC but imposed major logistic problems for series production. MCM would require to purchase and handle a multitude of bare chips in comparably small quantities. So VIPA decided to design an ASIC to reduce the later unit costs and keep handling easy. In order to minimize the risk and shorten time to market a rapid prototyping with a FPGAs was done.

There were two possible ways for the ASIC implementation. The device might have been realized using a cell based or a gate-array-ASIC-technology. Cell based ASICs make use of a technology dependent standard cell library delivered by the ASIC vendor. The main advantages of cell based ASICs compared to gate-array ASICs are increased integration density, reduced device costs and reduced total costs for high volume projects.

Gate-arrays make use of a channel-less sea-of-gate technology. The main advantages of gate-arrays compared to cell-based ASICs are lower fixed costs, reduced total costs for low volume projects and reduced turn-around time during ASIC manufacturing and therefore an improved time-to-market behavior. The reason for these advantages is the usage of non-application specific pre-diffused silicon wafers. Only the metalization of gate-array style ASICs is application specific. This means that only a small amount of the complete mask set that is necessary to process an integrated circuit has to be produced design specific. This fact reduces the fixed costs of the design. As the ASIC vendor is able to perform the project independent processing steps before the project dependent part is fixed, the turn-around time from the design's tape-out to shipping of first samples can be significantly reduced.

As the gate-arrays offer a faster time-to-market and reduced fixed costs the interface device has been realized this way.

VIPA used state of the art tools for design entry, simulation and synthesis. The entire design entry is based on VHDL because the pure VHDL description does not depend on later ASIC or FPGA technology. That means you do not need to worry about the later realization of your design at the early stage of the design entry.

The VHDL-code was verified and validated by using the VHDL simulator ModelSim (Model Technology). This design step included the creation of a VHDL-testbench and adequate testvectors. ASIC synthesis was done with Design Compiler from Synopsys, FPGA synthesis as well as place and route was done with MaxPlus from Altera. After synthesis the same testbench and testvectors were used to simulate (and verify) the netlist generated by the synthesis tool. After the layout of the ASIC (or the place-and-route of the FPGA) had been done the final netlists could also be simulated within the same testbench. The results were compared to the results of former simulations. So each step of the design flow could be verified by simulation. The same tool environment could be used on any level of hierarchy and any stage of the design implementation.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

VIPA has been offering electronic components and supplements for industrial applications since 1985. About 12 engineers in the development department dealt with designing circuit diagrams, PCB layouts and mechanical construction of modules for automation systems and industrial PCs. The design entry was done by schematic entry only. There was little knowledge about designing microelectronic components such as ASICs and the usage of HDLs for design entry and simulation. Some FPGAs and PLDs have been designed over the years using schematic entry most often and the HDL 'ABEL' in some cases.

During the AE there were six engineers temporarily involved in the pure development process and one as the project manager who coordinated the tasks and supervised the project plan. Two engineers were mainly responsible for VHDL coding and simulation, one for testbench generation, one for ASIC synthesis, one for FPGA prototyping and one for general test setup and hardware development. The entire testing was supervised by a test and quality control engineer.

Just as there was a lack of knowledge in technical questions regarding to microelectronic projects there was little experience regarding the management of such projects. Both the technical and managerial skills had to be improved in order to carry out an ASIC project successfully. There was no experience in using ASIC synthesis tools and also the knowledge about the layout of PCBs containing special microelectronic components which are susceptible for electromagnetic and high frequency interference had to be improved.

9. Work plan and rationale

Figure 5 gives a brief overview of the work plan and the effort and costs that were necessary to carry out the AE.

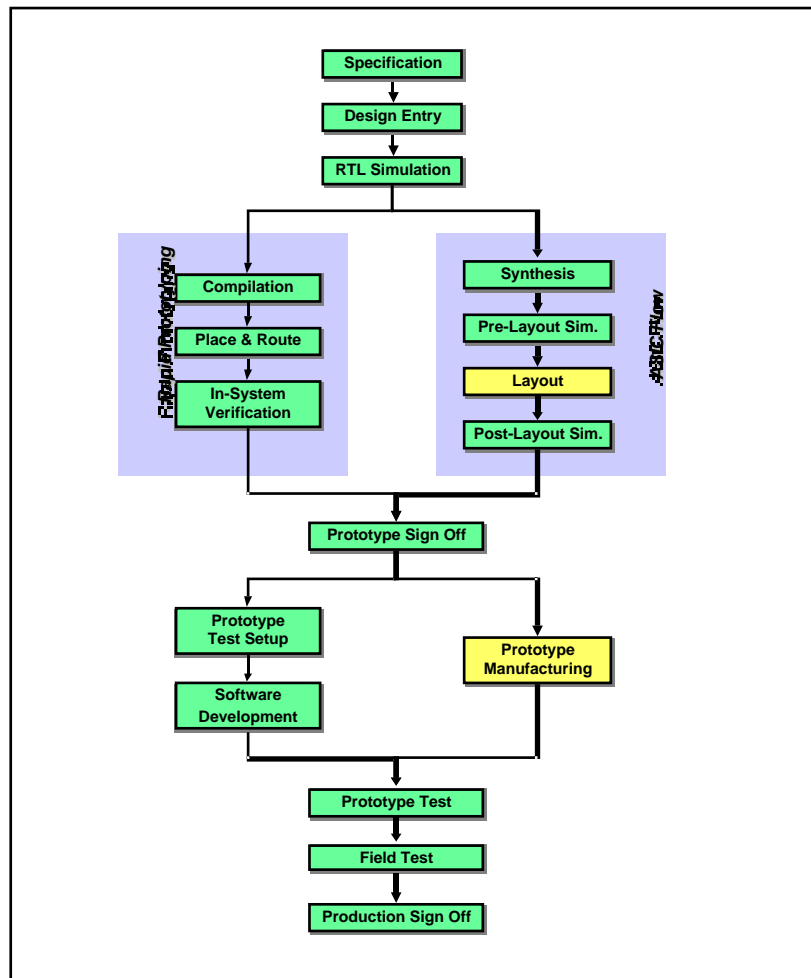
Activities	Labour (days)	Costs (€)	Month												
			1	2	3	4	5	6	7	8	9	10	11	12	
1. Management															
Project management	14	3.360													
Dissemination	8	1.920													
Reporting	13	3.120													
2. Specification															
Functional specification of system	6	1.440													
System specification of component	12	2.880													
Technical specification of component	12	2.880													
3. Training															
Management training	12	2.880													
Specification training	4	960													
CAD training	5	1.200													
Design training	5	1.200													
4. Design															
System level design	20	4.800													
Subsystem level design	31	7.440													
5. Evaluation															
Prototype production	16	3.840													
Test set-up	12	2.880													
Functional testing	20	4.800													
Prototype testing	18	4.320													
Field testing	16	3.840													
Investment		4.505													
Subcontractor Services	30	16.291													
Other Services		18.368													
Total	254	92.924													

Figure 5 : Overview of work plan and effort

The First User acquired his knowledge on ASIC technology through several training measures and coaching during a limited period of time. Then the design was done almost entirely by the First User, with only minimal support from the subcontractors, but of course with the support provided by the design tool supplier and by the semiconductor vendor, which was well sufficient to successfully finish the project.

The functional specification of the system and the technical specification of the component were carried out by the First User with the assistance of the subcontractors. They made suggestions how to use VHDL for specification and design purposes and what measures had to be taken in order to improve the ESD behavior of modules used in industrial environment.

During the implementation phase the entire design was divided into sub-modules, each with designated functionality and interface. These sub-modules were described in VHDL on RT-level subsequently. Partitioning and VHDL coding of the design was supported by the vendors of the synthesis tools that were used for FPGA- and ASIC synthesis. The First User took part in 'Advanced Chip Synthesis' courses (1,5 K€ per participant) in order to become familiar with the VHDL subset that can be used for synthesis, various coding alternatives and their impact



on the later synthesis results, the correct definition of timing and area requirements and the effective use of the tools. The ASIC vendor offered additional support regarding to all technology specific questions. Each design step was verified by means of VHDL simulation.

Figure 5 : Design Flow

In the meantime a FPGA rapid-prototyping board had been created (Figure 6). The entire design could be downloaded on the FPGA and tested under real operating conditions. In order to improve the knowledge about PCB layout regarding to ESD problems the First User took part in special layout courses offered by the vendor of the PCB layout system (2,25 K€ per participant) . In these courses the participants gained experience and a good understanding for the problems arising, for example, from insufficient shielding in industrial applications. The acquired knowledge and practice could be used to optimize the PCBs used for prototyping, test purposes and the later mass production.

The final VHDL code was released for ASIC synthesis after a detailed review. The VHDL code was synthesized to a technology specific netlist. The necessary libraries were provided by the ASIC vendor. An optimization of the netlist was done until all constraints were met. VITAL simulations were used to check the correct functional and timing behavior. After another review the final netlist was passed to the ASIC vendor for layout. Costs for layout and sample production amounted to 18 k€. This was the only part of the work, which has not been done by the First User. It was somehow comparable to a PCB supplier.

Before the layout was done the delays caused by the placement of the cells on the chip and the wiring between the cells could be estimated only. After layout the real delay data was back annotated in Standard Delay Format (SDF) which could be read by the VHDL simulator. Again functional and timing requirements were checked by means of VITAL simulation. As there were no deviations of the desired functionality the layout was released for prototype

production.

The ASIC prototypes were tested on the PCBs also used for the later mass production. Several in-house tests as well as field tests in co-operation with potential customers were carried out to check the accuracy of the prototypes. All tests were passed successfully and the design could be released for production.

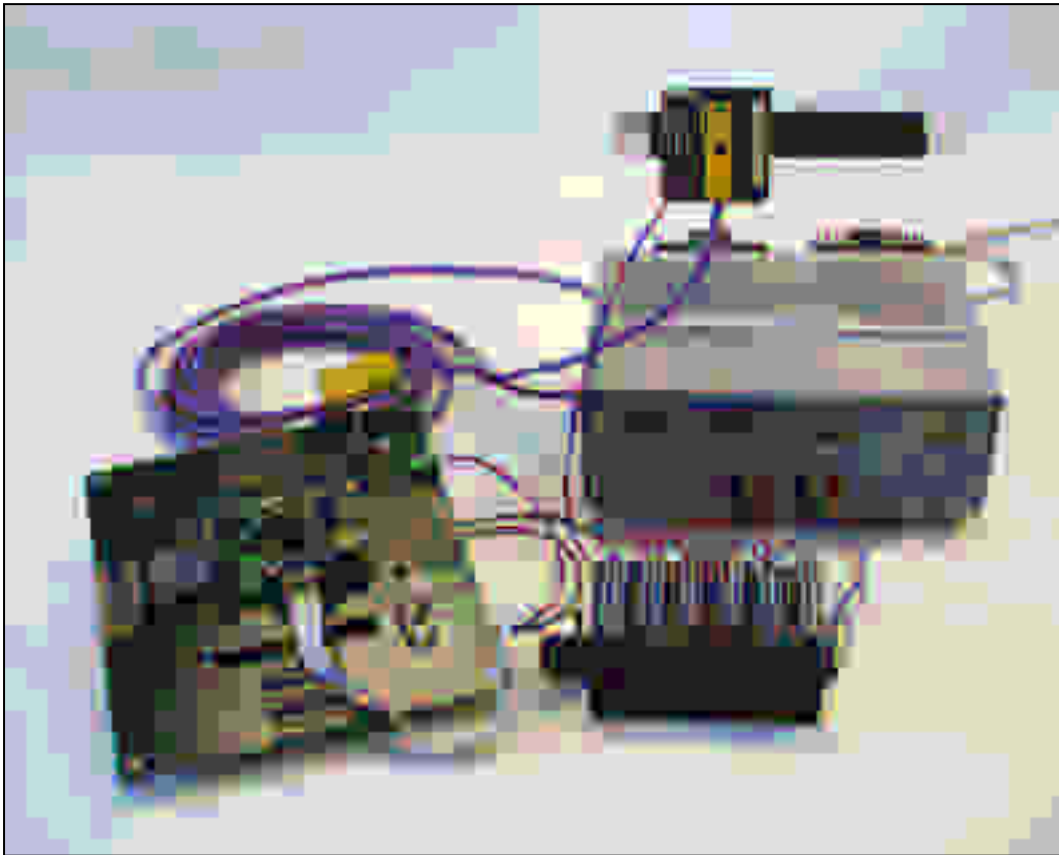


Figure 6 : Rapid prototyping board

The development of an gate-array takes significantly longer than the development of a comparable FPGA, that is, the FPGA offers the opportunity to be on the market in less time. There is also the risk of a possible redesign of the gate-array when functionality or timing of the device is not simulated carefully or the system environment is not modeled properly.

10. Subcontractor information

With assistance from the TTN VIPA planned the general project approach. The plan required a basic training company, design tool supplier and a service provider for layout and manufacturing of the ASIC. The training company should be independent from tool suppliers and semiconductor vendors. They should also be in the neighborhood if possible. Asside from technical aspects of the design tool, the tool supplier should provide support. Otherwise an additional subcontractor may be required. The semiconductor vendor should have a suitable technology and should also provide the ASIC library and possibly support for the design tool, which was selected. They should also offer suitable conditions for series supply. Sharing the risk for redesigns may be important, but with sufficient measures to control risk, like FPGA prototypes and MPW this was less important.

VIPA took part in design and management classes offered by the Fraunhofer Institute for Integrated Circuits and by the suppliers of the tools used during the AE for simulation, synthesis and board layout. VIPA decided to gain additional knowledge and experience in these special fields in order to be able to realize future ASIC projects with less or even

without external support.

VIPA asked several ASIC vendors for a quotation and finally decided to do the project with NEC. NEC offered a wide range of suitable Gate-Array-masters and excellent support at an adequate price. They provided VIPA with libraries for simulation and synthesis and gave advice about how to use their vendor specific tools for buffer insertion, delay estimation, etc.. Therefore VIPA's project team was able to carry out all design steps by themselves except the layout of the Gate-Array. Layout and prototype manufacturing were done by NEC.

It took about 10 weeks from the production sign-off to the delivery of the first devices. NRE must be paid after delivery of the prototypes. The risk of a possible redesign was taken by VIPA.

11. Barriers perceived by the company in the first use of the AE technology

As former projects had been done by schematic entry only, the staff had to overcome the start-up problems associated with the new design methodologies used in the AE. They had to be motivated to stop thinking about logic gates and wires and adapt to a more functional and behavioral view of the system. This behavioral view of the system could be easily translated to VHDL. They had to recognize that it makes no sense to just describe a schematic in VHDL.

Former FPGA and PLD designs were often done by some kind of trial and error. The designer did the design entry, programmed the device and tested the correct function of the device on a testboard or simply in the target application. It's obvious that an ASIC cannot be developed this way. The RTL coding, the pre- and post-layout data and even the specification of the circuit have to be verified and validated by means of simulation.

It's been difficult to find the synthesis environment and the ASIC technology that fits best for this project. There are a lot of ASIC vendors but only few of them could offer a master-package-combination that meets the requirements of this project. Therefore a lot of inquiries and meetings were necessary to find an adequate solution.

As the AE was VIPA's first ASIC design and the first design done with VHDL the entire design environment (VHDL simulator and ASIC synthesis tools) had to be purchased. Therefore some greater investments had to be done in advance in order to start the project.

12. Steps taken to overcome the barriers and arrive at an improved product

The staff involved in this project took part in several courses and workshops in order to improve their knowledge and experience in the new design methodologies and the managerial requirements of this project. The engineers were motivated to use VHDL as the design entry and to verify each design step by simulation. They were trained to make efficient use of the simulator and the synthesis tools. So there was no uncertainty regarding to the correct behavior of the later Gate-Array. In addition a rapid prototyping with a FPGA was done. Therefore the design could be verified not only by simulation but also by in-system tests at an early stage of the design flow.

13. Knowledge and experience acquired

VIPA gained additional knowledge regarding the efficient use of VHDL for design entry and design verification from NEC and also from the vendors of the CAD tools used in the AE. The microelectronic staff is now able to model the system environment of a circuit in order to validate the specification of the circuit at the beginning and to verify each design step during the entire project. They are also able to describe the timing and environmental requirements of the circuit. This information can be used to define the constraints for the synthesis tools. If the initial constraints are not met the engineers learned how to optimize certain parts of the design independent from each other in order to meet the requirements in the end. As the development

of a Gate-Array and the development of a Standard-Cell-ASIC only differs in which kind of cell library is used for synthesis and simulation, VIPA is now able to carry out Standard-Cell-projects, too. That is, the goals regarding knowledge transfer and acquisition of experience defined in the AE could be reached.

Summarizing the points mentioned above VIPA gained additional knowledge in:

- ASIC project management (Gate-Array and Standard-Cell-Designs)
- effective use of VHDL for specification purpose
- VHDL coding for synthesis (ASIC / FPGA)
- functional verification by means of RTL simulation
- design constraining / design optimization
- timing verification (VITAL simulation / SDF)
- design verification by means of Rapid Prototyping

14. Lessons learned

During an 'Advanced Chip Synthesis' workshop the members of the project group dealing with synthesis and optimization of the design learned to make efficient use of special features of the synthesis tools such as constraining the design in a way that the timing requirements could be reached while the overall area could be decreased. They learned to re-organize the registers in the design in order to improve the performance of the circuit and how to forward-annotate links-to-layout. These links are used by the ASIC vendor to do an initial floorplanning of the design in order to meet the timing requirements.

VIPA gained additional knowledge about PCB layout especially when the design is timing critical and is used in industrial environment. Industrial applications have to meet special requirements regarding to electromagnetic radiation, reliability and performance. The layout as well as the quality management and testing staff was trained to be able to keep and observe the required layout rules.

15. Resulting product, its industrialisation and internal replication

The overall system performance could be increased while the unit costs and the size of the interface device could be decreased significantly. The following table shows the comparison of the gate-array implementation to the former FPGA solution for a 4-channel Analog Output module:

System Performance	+ 33 %
Test cost	- 20 %
Size	- 70 %

Figure 6 : Example of Product Improvements

All product improvements planned during the AE definition could be reached. With these improvements the final product should be able to win the competitive edge over similar products on the market.

The gate-array prototypes have been tested successfully on several types of intelligent I/O modules and were released for mass production. Now the Gate-Array is used on all intelligent I/O and function modules in order to decrease the costs and to increase the performance of these modules. All modules have been fully functional and first sales could already be realized in 1998. The improved modules are fully compatible to the existing products.

Meanwhile VIPA carried out another Gate-Array project and started a Standard-Cell-Design using the knowledge and experience gained during the AE. The Gate-Array is a common interface device that can be used on all digital I/O modules of 'SYSTEM 200V'. The Standard-Cell-Design is an implementation of a fieldbus slave application. We are still in contact with the sub-contractors from the AE for additional improvements of our design techniques. Again the whole design flow is based on VHDL, so the entire design environment established in the AE and even parts of the AE design itself can be re-used.

In order to keep the simulation and synthesis software always up to date we signed maintenance and support contracts with the vendors of these tools. This offers the ability to use state of the art tools efficiently and to get adequate support at any time we need it. Furthermore, we can take part in additional workshops and courses to maintain and further improve our knowledge and experience.

Several steps have already been carried out to commercialize the improved product. VIPA advertises the improved products in technical journals and did internal workshops for VIPA's salespersons and representatives. In addition VIPA will carry out external workshops for customers in order to make them familiar with the new products. This process of industrialization and commercialization will take about three months and will cost about 12 KEuro.

16. Economic impact and improvement in competitive position

As the costs for several types of modules could be decreased significantly the entire product became more competitive. A cost reduction of up to 30% in some configuration could be gained by reducing the number of PCBs per module to one. Because there are a lot of competitors in the field of modular automation systems it's necessary not only to offer a high-quality product but also to develop and manufacture this product economically. With the ability to use one Gate-Array on several modules the unit costs as well as the storage and development costs could be decreased. The ASIC will be an important step in improving VIPA's competitive position and will help to increase the market share of VIPA products. The customers will get a faster and more reliable modules with additional features at the price of the old product.

Due to decisive performance improvements the actual sales realized in the last quarter of 1998 and the first quarter of 1999 surpassed the expectations. If this trend continues the number of sold intelligent I/O modules will be doubled in 1999. Figure 7 shows the expected number of sales of the old products marked in green and the additional sales because of the product improvements in purple. The numbers for 2000 and 2001 are extrapolated from the actual numbers in 1998 and the first quarter of 1999.

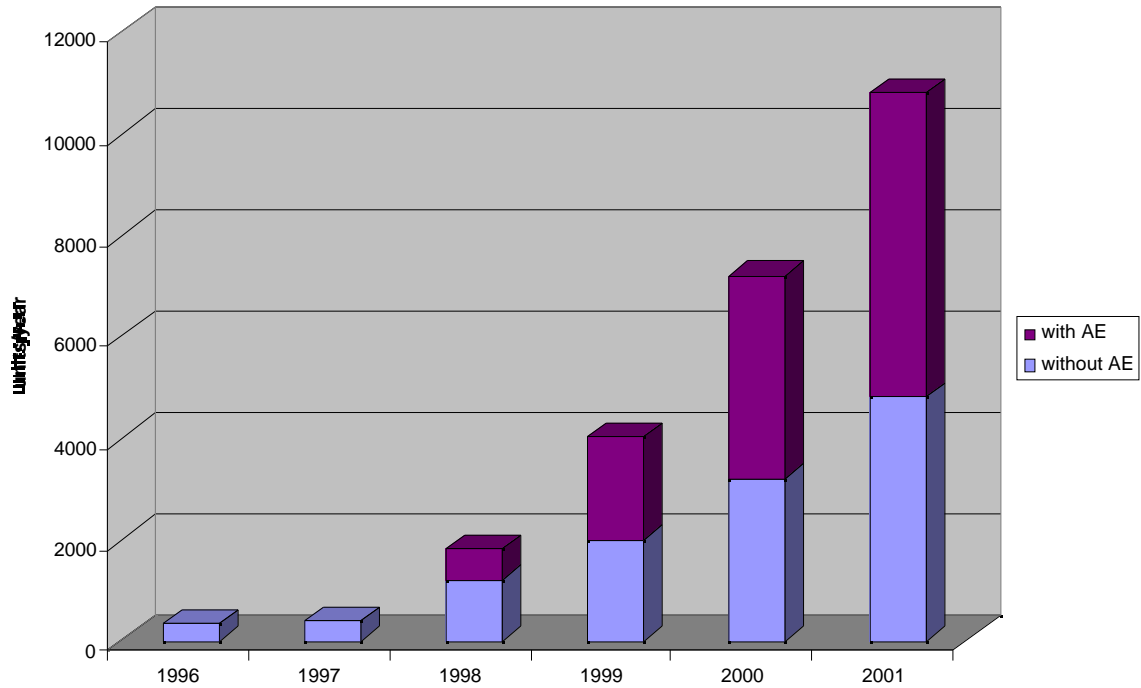


Figure 7 : Number of additional sales (intelligent I/Os) due to product improvements

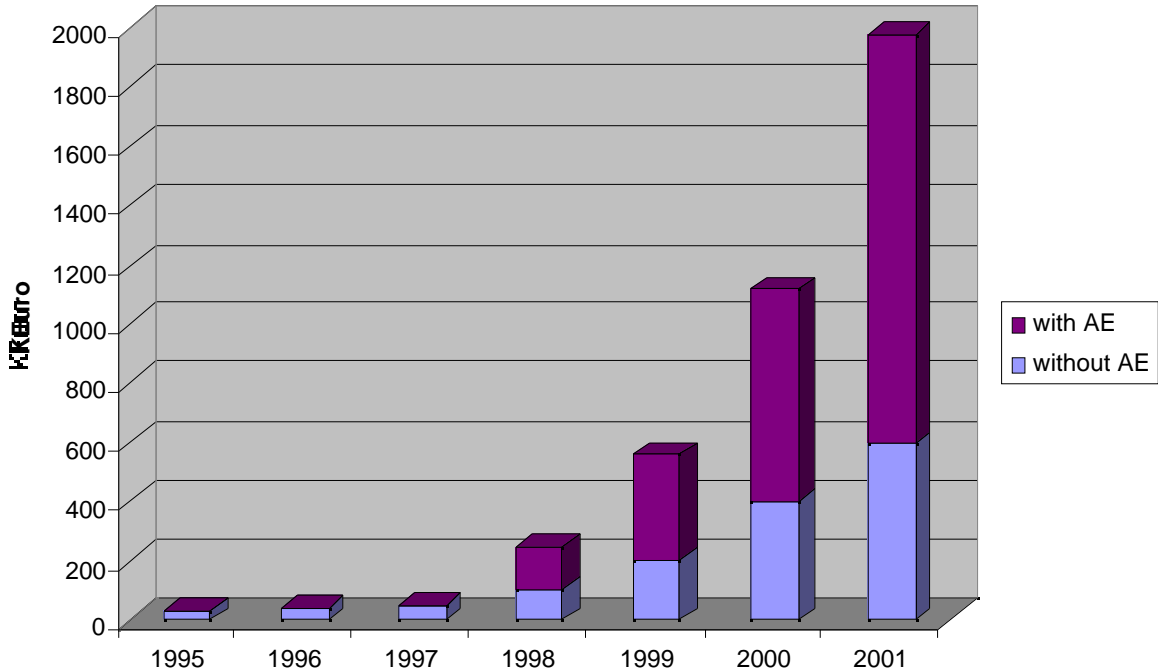


Figure 8 : Expected increase of profit (intelligent I/Os)

As there is also a reduction of the costs per module the increase of the profit that can be realized with the improved modules is even higher than the increase in the number of sales.

As there were significant improvements and savings upon the former implementation of the

modules the payback-period should be less than two years and the estimated return-on-investment is about 500%. The lifetime of the product will be approximately five to seven years. The predicted increase of the market share is about 10%.

17. Target audience for dissemination throughout Europe

This project shows a way to acquire ASIC expertise with very concise support by subcontractors. This not only helps to minimize external costs but also allows better protection of application know-how.

The experience gained within this Application Experiment might be of some interest for every company considering the first or the advanced use of VHDL and programmable logic devices or application specific integrated circuits. This refers not only to automation industry but to all industrial fields where the use of the design and test methodologies mentioned above will help to shorten time-to-market and reduce development and production costs for new products.

Major application areas can be found in PRODCOM 29 (Tools and Machinery) and 31 (Electric Equipment) industries.