FUSE Project 2071

Profibus control module:
ASIC Gate Array reduces cost and guarantees supply

Demonstrator Document

Abstract

Weidmüller Interface (WI), a company with 1140 employees, develops and produces interface modules used for automation solutions. The product portfolio ranges from electro-mechanical components like terminals and connectors (interfacing just with wires) to I/O modules that communicate via fieldbus.

One of the company's products which is sold in high quantities is a field bus I/O module. Before the Application Experiment its main component, the fieldbus controller, had to be purchased from a direct competitor, the price was relatively high. Thus, the technical objective of the Application Experiment was to replace this component by an own ASIC having exactly the functionality needed in WI's I/O modules. This makes WI independent on its competitor and results in lower manufacturing costs. In this way the main goal of the Application Experiment was met: to increase Weidmüller's market share and turnover in this market segment by reducing the price of the product WINbloc which is sold worldwide it is used in PROFIBUS applications to interconnect terminals, machines or other participants in complex production networks.

Before the Application Experiment (AE) WI had know-how and experience in the design of PCBs, the development of circuits with discrete electronic components (up to micro- and fieldbus-controllers) as well as hardware and software for standard fieldbus systems (e.g. PROFIBUS, CAN, LON).

Within the Application Experiment, basic knowledge in the management of digital ASIC projects was transferred to Weidmüller. From the technical point of view, WI's specialists learned the top level design of digital systems with VHDL and automatic synthesis, but also gate level design methodologies and test methods. In parallel, the involved specialists got an overview of available design tools.

The main lessons learned concern management problems to evaluate design tools and libraries, but also best practice in VHDL based top level design suitable for automatic synthesis.

The designed ASIC realises a PROFIBUS-DP interface plus additional functionality. Compared with the competing component, only the necessary features have been implemented, i.e. the ASIC has a reduced functionality, but an optimised structure and a lower power consumption, a smaller package and a better EMC behaviour.

Thus, the major benefits of the AE are the cost savings for our product and the improvement of the competitive situation. Last not least, an ASIC design group was established in the development department.

The total costs up to the prototype stage were 92 kECU, the duration of the project was 12 months which included a delay of 5 months due to difficulties with tools and libraries, some unforeseen consistency problems in the fieldbus standards and higher design effort resulting from additional iteration cycles and an intermediate FPGA prototype. For the industrialisation, a second chiprun outside the EUROPRACTICE MPW Services was necessary resulting in additional industrialisation costs of 75 kECU for the electronic part and additional 30kECU for changing of WINbloc module.

Assuming a product life time of 3 years, the total ROI of the FUSE investment will be about 500%, with a payback period will be 6 months.
Keywords
Digital ASIC, Gate Array, VHDL, Viewlogic, Fieldbus, PROFIBUS, Machine control, Communication interface

Signature
4  1410  555  1410  3  3120  3  31  D

1. Company name and address
Weidmüller Interface GmbH & Co. (WI)
Electronic Competence Center
Ohmstraße 9
D-32758 Detmold

2. Company size
Weidmüller Interface GmbH is a company with about 1140 employees located in Detmold/Germany. 110 co-workers are employed in the electronics department, 35 of them in the electronics R&D department, the others in the production. Two design engineers and a design manager were involved in the AE.

Within the worldwide acting Weidmüller group it is an independent company with a long tradition in the manufacturing of interface modules for automation technology. The total turnover of Weidmüller Interface is about 450 M€ per year.

3. Company business description
Weidmüller Interface (WI) develops and produces interface modules used for automation solution. They range from electro-mechanical components like terminators and connectors (interfacing just two wires) over electronic components providing galvanic isolation or any kind of protection to I/O modules which communicate via field busses. In addition tools and installation products are manufactured and sold.

The typical customer is a company which offers automation products such as tooling machines, automation solutions for buildings or any product which requires to connect a bigger number of electric signals.

Weidmüller by its nature is a supplier of such connecting components that are used by its customers to build up complete automation solutions. Weidmüller's target markets are machine, process and building automation. Transportation is another sector WI's products are marketed on. About 20 % of the company's revenue is made with electronic components. The remaining part is dominated by plastic and metal manufacturing technology.

WI is responsible for research and development, product definition, marketing and manufacturing in the Weidmüller group. Sales are carried out by a number of sales companies that are located worldwide in all major countries.

Before the Application Experiment (AE) WI and the staff involved in the AE had know-how and experience in the design of PCBs, the development of circuits with discrete electronic components (up to micro- and fieldbus-controllers) as well as hardware and software for standard fieldbus systems (e.g. PROFIBUS, CAN, LON).

The following two figures describe the structure of the Weidmüller group and their product lines.
Fig. 1: Structure of Weidmüller GmbH
Fig. 2: Products and services
4. Company markets and competitive at the start of the AE

Weidmüller's market can be defined as third-party market for industrial automation devices, i.e. the company sells components to companies who combine them with other (separately bought control units) to an automation solution. The competitors in this market are other third-party sellers as well as the companies selling complete solutions. Such a solution contains both, the central control unit and the controlled fieldbus nodes. Even if the FU does not sell control units it might be possible to attract original solution-buyers for the fieldbus nodes of Weidmüller. This is done primarily by price due to quite comparable features of the various offers in the market.

Considering the complex and overlapping market segments in the industrial automation business it is quite problematic to define the market size the FU acts in. The estimation for the complete centralised industry automation market for the year 2000 is 70 million US$ for Europe, 33 million US$ for the USA and 44 million US$ for the Asian market. Although no reliable market study exists from which Weidmüller's market share for industrial generic I/Os can be derived exactly it can be said that Weidmüller's market share in Germany and Europe is somewhere between 4 % and 10 %. The main competitors are Siemens, Phoenix Contact and Wago-Beckhoff. Their estimates market shares are shown in the picture below:

Concerning PROFIBUS the competitive situation is somehow delicate. Mostly, a bus system has been introduced and is dominated by a single company. In the PROFIBUS case this is Siemens, also the biggest seller of control units for automation. This makes Siemens to the first choice in terms of complete automation solutions as well as for single fieldbus nodes. Therefore Siemens is a very strong competitor in the fieldbus business.

On the other hand, before the Application Experiment the only reasonable way to build I/O modules was to use a PROFIBUS controller ASIC developed and sold by Siemens. Thus getting access to an own ASIC solution not only promises independence from a single source and pricing. It also gives a clear signal to the market that Weidmüller will not be just a follower trying to differentiate on certain features but a leader controlling the full range of technology and competence to bring I/O-modules to the market.

In our case there was no pressure from the side that market shares with the old product would have been declined. As can be seen in the chart, it has been sold successfully for years with increasing tendency (Basis:1997=100%; 60000 pieces). However, there was a strong requirement to reduce manufacturing costs and to become more competitive by introducing a new and own solution.
This is very important, because the market for fieldbus applications will increase in the next years continuously for about 10...20% per year. Of course the change from a technology follower to a leader is a risk. Therefore, the compatibility of the solution must be proved by a third party and it must work stable and reliable under any kind of conditions.

5. Product to be improved and its industrial sectors

The product to be improved was part of the WINbloc family. WINbloc is an industrial I/O-system supporting the major fieldbus systems (PROFIBUS, CAN, Interbus-S) with a variety of analogue and digital input and output circuitry. The number of different I/O modules for the WINbloc system is around 20. Due to the subject of the AE only the PROFIBUS system will be further considered.

A PROFIBUS-based fieldbus connects a number of I/O-modules, so called “slaves” with a Control-Unit called “master” by means of a two-wire media. The master is usually a PLC (Programmable Logic Controller) with PC-based solutions coming up in this field. Compared with a traditional solution, the main advantage of a fieldbus application is the reduction of the necessary wires and connectors. In the old systems, every sensor or actuator is directly connected to the PLC. A typical example of a PROFIBUS system is shown in Fig. 3.

![Diagram of PROFIBUS system]

Fig. 3: Example of a PROFIBUS system

Fig. 4 illustrates the structure of a slave device.
The input- and output circuitry of every slave is controlled by the master with a program which is executed in a loop continuously. The inputs of the slaves are read into the master. Based on their state the output data is calculated. These output data are sent to the slaves that set their output circuitry accordingly. This process is described in the next figure.

A WINbloc–based slave always consists two functional parts:

1. a fieldbus specific submodule (named bus coupler).
2. the I/O submodule

Both submodules are connected using an interface standardised for the WINbloc-system. This offers a wide range of products supporting any convenient combination of fieldbus and I/O electronics. The both submodules are placed into a plastic housing and plugged on a base module that contains the terminal block for connecting sensors/actuators with the slave circuitry. A photo is shown below.
A number of WINbloc-modules can be combined easily in a row without external wiring to connect the fieldbus. This offers cost advantages for the customer. Such a combination of different WINbloc-modules is shown in Fig. 7.
The environment WINbloc devices operate in is usually a harsh one. High ambient temperatures and poor options to remove self-generated heath urge the need for low power consumption and a wide operating temperature range. Also the electro-magnetic compatibility (EMC) is not easy to maintain due to strong influences e.g. because of large electric drives and strict standards for emitted radiation.

Currently the most important fieldbus coupler in terms of volume is the submodule connecting I/O electronics to PROFIBUS. The most important component of this submodule is the LSPM2 PROFIBUS controller of Siemens. This component determines the logical behaviour on the PROFIBUS, the power dissipation, the EMC and the cost of the bus coupler.

For the WINbloc bus coupler this meant good PROFIBUS performance, rather high power consumption considering the small plastic housing, a high development effort to maintain EMC and considerable costs.

Therefore, the objective of the Application Experiment was to develop an own solution which

- meets the Profibus standards
- implements only such functionality which is required by Weidmüller
- reduces power consumption and maintains EMC conditions
- reduces manufacturing costs.

Our goal was not to increase the direct Profibus functionality, but to become

- more competitive by a price reduction of the product and
- independent from the main competitor in this application field.

Thus, the product innovation allows to overcome a lot of cost generating problems. With an own ASIC, the market segment can be penetrated in a way competitors cannot follow easily.

6. Description of the technical product improvements

As described, the basic idea for achieving the improvements was to implement only those features which are really used in the WINbloc system. It does not require all features of the SIEMENS LSPM2.

Developing our PROFIBUS ASIC WPS1 (Weidmüller PROFIBUS Slave), the following main improvements should be achieved:

1. Space

The housing for the WPS1 is a smaller one (package TQPF64 instead of QFP80). In addition to the 32 bi-directional ports, the WPS1 has only two diagnostic pins.

An additional space saving was achieved by avoiding or by reducing the number of external shift registers which are needed for device initialisation. Any PROFIBUS device needs a 16 bit identification plus a 7 bit address which results in 3 external 8 bit shift registers. Because 8 bits of WI's identification numbers are fixed, it was possible to implement half of the ID code hard coded without a shift register. In this way, only two are necessary.

If the WPS1 is used in an application which uses less than 16 bi-directional ports a mode is implemented which allows to use 16 of the 32 bi-directional ports for this device initialisation, i.e. no external shift registers are needed any more. This space saving is especially useful in applications with a limited number of I/Os.

Furthermore the WPS1 integrates several less important external components (pull-ups, pull-downs, inverters). The basic structure of the bus coupler is provided in the next drawing. Figure 8 shows the complete system with ASIC and the achieved component/space reductions.
2. Power dissipation

In industrial automation space, packaging and wiring density are key factors for competitiveness. Thus, housings must be as small as possible. In order to meet requirements for electrical isolation and because of cost issues plastic housings are the only choice for I/O modules. Unfortunately, smaller housings mean a reduction of power dissipation, i.e. the internal power consumption had to be reduced.

Without additional effort, a typical WINbloc module can dissipate about 1 Watt. The previous PROFIBUS controller LSPM2 had a share of 350 mW. The new WPS1 ASIC reduces the power consumption to 50%. The key issue to achieve this goal was to reduce the clock frequency for those parts of the design, which do not really need it. The resulting multiclock system is more complicated, but has many benefits for power dissipation and gate count.

3. EMC

When the WINbloc family was developed it was fairly difficult to design a PROFIBUS coupler which supports the highest transmission rate of 12 MBit/s. It was necessary to clock the device with 48 MHz. The clock generator caused severe emission problems at 48 MHz and above. It took several design iterations to get a compliant hardware which resulted in high manufacturing and component costs for the old product.

The WPS1 solves the problem by incorporating a PLL. Although the WPS1 needs the 48 MHz for its high-speed sections too, only a 4 MHz quartz is necessary to clock the design. The high frequency is generated internally and is kept inside. The use of a simple quartz instead of an oscillator resulted in additional cost savings.

4. Cost reduction

Costs are always a strong argument. The component to be replaced is single sourced and must be bought by Weidmüller even for more than 10€ per piece (even for high volumes). The objective was to get an own ASIC from the manufacturer for less than 5€. As stated above, further savings could be achieved by the reduction of external components.
The resulting ASIC fits in a Gate Array Master of around 12,000 usable gate equivalents.

7. Choices and rationale for the selected technologies and methodologies

Technology

A PROFIBUS controller is a pure digital system without any mixed-signal requirements. Standard CMOS technology is sufficient. However, at least a 1.0 µm technology was needed because of the 48 MHz clock necessary in the system. With this preselection in mind, three kinds of technologies were taken into consideration:

1. FPGA

The most obvious advantages of FPGAs are the direct in-system verification of the prototypes, the missing non recurring engineering cost (NRE), no engineering effort for test structures and no delay to production as prototypes are identical to volume. According to the gate count estimate of 10,000 to 15,000 the use of FPGAs was possible.

But FPGA gate counts tend to be much higher, especially if a synthesis based design methodology is used. Only hand crafted designs will meet comparable gate counts. The problem gets even worse in the 48 MHz part of the design. Although possible FPGA designs in this frequency range need some special skills.

Also some of the design goals would have bee affected using FPGAs. First of all the cost issue. Without substantial cost savings the production will not be switched to the new component. Even if the FPGA hasn't any NRE costs, the final price (lower than 5€) cannot be realised even for a high number of pieces.

In addition some of the technical design goals could not be met with an FPGA.

- Packaging choice is limited. The desired QFP-64 was not available.
- No PLL is available. Thus a 48 MHz quartz would be necessary which is difficult to handle. In addition it will consume more power than a 4 MHz quartz.

2. Standard Cell

A standard cell design will overcome the disadvantages mentioned above. Compared to gate arrays, such a design should be smaller resulting in the lowest possible price for the silicon, but this did not become clear when comparing the different offers.

The major disadvantage of a standard cell design are the relatively high NRE (non-recurring engineering) costs. The NRE for a standard cell design is two or three times higher than for a gate array solution. For such a design, for the first prototypes so-called multi project wafer (MPW) runs are used. Such a MPW run requires to follow a certain schedule. If the design is delayed only for a few days, you have to wait until the next run is started.

The standard cell technology is really needed by mixed-signal designs but the PLL is the only mixed-signal issue. Therefore, this technology was not selected.

3. Gate Array

The gate array technology gives a compromise between the best technical solution (standard cell) and the high flexibility of FPGAs. Even two shots for a gate array design are cheaper than one shot in standard cell technology. Also the time from prototype to production is much smaller compared to the standard cell technology.

It shall not be neglected that the gate array technology shares a certain disadvantage with the FPGAs: the design must fit on a given master. If it does not, the next bigger master must be selected and silicon cost will jump to the next step. Another disadvantage in the gate array design flow comes up when the design gets too close to the maximum capacity of a certain master. There are no hard limits, but the place & route step is very time-consuming in this case. Therefore, the availability of different master offered by the ASIC vendor is an important criteria for selecting a partner.

E://use-net/demonstration/31/2071/gemac 2071 weid dfx.doc
The following table gives an overview of various offers we got:

<table>
<thead>
<tr>
<th></th>
<th>NRE</th>
<th>Volume pricing / 10k</th>
<th>Volume pricing / 20k</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>ES2</td>
<td>55 k€</td>
<td>4,40 €</td>
<td>3,95 €</td>
<td>Standard</td>
</tr>
<tr>
<td>FHG-IMS</td>
<td>60 k€</td>
<td>9 €</td>
<td>6,30 €</td>
<td>Cell</td>
</tr>
<tr>
<td>Fujitsu</td>
<td>28 k€</td>
<td></td>
<td>6,60 €</td>
<td>Gate</td>
</tr>
<tr>
<td>GEMAC (ZMD)</td>
<td>22 k€</td>
<td>4,6 €</td>
<td>4,35 €</td>
<td></td>
</tr>
<tr>
<td>NEC</td>
<td>18 k€</td>
<td>4,25 ... 5,50 €</td>
<td>3,30 ... 4,40 €</td>
<td>Array</td>
</tr>
<tr>
<td>Thesys</td>
<td>20 k€</td>
<td>3,20 ... 4,25 €</td>
<td>3,00 ... 4,10 €</td>
<td></td>
</tr>
</tbody>
</table>

Proposed Methodology

The definition/selection of a suitable design methodology was an integral part of the AE. The most important issue when choosing the design methodology was to enable WI to design digital ASICs in the future with lowest risk and in a minimum of time. Although the gate array technology was chosen, the know-how transfer enabled Weidmüller to discuss all available technologies for next projects. Main subject to meet this goal was a high level design methodology using the hardware description language VHDL followed by an automatic synthesis of the gate structure on the basis of the chosen target technology.

The proposed design methodology was divided into three main phases:

1. **Textual specification of the design**
   
   This phase contains the first analysis of the DIN 19245 part 1 and 3 which had to be implemented into the ASIC. Based on these information, a textual specification was written. The next step is to divide the design into different functional blocks to specify the data flow in the design.

2. **Behavioural VHDL description of the design**
   
   A reference model of a PROFIBUS-DP slave was written in VHDL. The used coding style is called “behavioural VHDL”. The only purpose of such a code is to provide a simulation model. In this state the VHDL-simulation tool - Fusion from Viewlogic - was used.

3. **VHDL-description of the design on Register-Transfer-Level (RTL) and synthesis**
   
   The RTL description of the design is the starting point of the process of generating the so-called “netlist” which represents the physical structure of the ASIC. It had been written from scratch based on the partition of the design into different function modules considering the coding guidelines of the synthesis tool. Parallel to this step the synthesis tool was set up. The result of the synthesis step is the netlist. It represents the design in terms of basic cells of the target technology and the interconnections between them.

In parallel to points one to three supplementing VHDL libraries and UNIX-shell scripts were written to implement the best way for test pattern generation, writing protocols of simulation events and batch mode simulations.

4. **Design verification using FPGAs**
   
   The application of a synthesis-tool offers an easy way to switch between different target (also "non-ASIC") technologies. In the AE an intermediate FPGA prototyping step has been used to verify the design. These components allow a very fast and cheap modification of the design and reduce the ASIC design risk dramatically.

   The FPGA based verification step was introduced additionally, because of simulation problems. It was not part of the initial workpackages.

5. **Implementation of test structures and sign off procedure**
   
   Finally, the design was in a state in which the correct function was realised and the synthesis-constraints were properly fulfilled. In addition, test structures were implemented during the sign-off process at a design centre of the manufacturer Thesys.
After the final layout verification and post-layout simulation the FU had to control the correctness of the design and to release the manufacturing process.

It was a vital aim of the FU to gain a maximum in experience and know-how during the AE. So all major design phases were done or closely accompanied by the FU. The subcontractors provided primarily initial know-how and continuos design assistance during the project.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

Because of Weidmüller's traditional main business in the area of electro-mechanical components there is a lot of know-how in plastic technology as well as in bending and punching of metal. The electronics division was founded in 1983 and is small compared to the whole company. It develops and produces passive components (transmitters), active components (converters and couplers) and so-named intelligent modules (multiplexer, fieldbus modules, gateways, system interfaces). There is know-how and experience in design of PCBs, the development of circuits with discrete electronic components (up to micro- and fieldbus-controllers) as well as hardware and software of standard fieldbus systems (e.g. PROFIBUS, CAN, LON). Important design tasks are assuring the EMC compliance and thermal management of the component to be developed.

Besides the PCB layout tools the organisation has no expertise or skills in using EDA tools. This is especially true for ASIC design.

In 1992 an EDA solution was purchased from Viewlogic with intention to do board and system simulation - including a mixed-signal option - before building real prototypes. Unfortunately the design entry and simulation tools never became productive due to the lack of appropriate simulation models. Another reason for the failure was that the functionality of typical circuits is not a major design concern. EMC compliance and thermal management by far are more important. Although not in daily use the tools and the workstations were kept under maintenance i.e. new versions have been set up.

The person in charge for maintaining the Viewloginc design environment participated in the Application Experiment. The second full time electronics engineer had just finished his studies at Manchester University Institute of Science and Technology (UMIST). At the beginning of the AE both engineers had no professional experience as ASIC designers. The project manager already gained experience in managing and co-ordinating microelectronic projects during his former employment before he joined Weidmüller. In our company, he was involved in soft- and hardware design of LON automation components.

9. Workplan and rationale

The workplan was divided into five major workpackages. They are:

Management: Management of the AE and generation of reports. The role of the subcontractors was to give advise to set up a design route suitable for the AE. This happened in form of consultations. After that the FU was responsible for the design route and reporting.

Specification: Description of the system and component behaviour and electrical specification of component. The subcontractor HNI supplied know how in the fieldbus area during various meetings. The subcontractor Thesys was primarily involved via email and telephone in the field of electrical specification.

Training: Setting up a sufficient know how to accomplish a successful end of the AE. The FU booked the training courses and assigned it's people. This was made primary at external facilities which offered suitable courses. The HNI helped to conduct the training and gave support in the field of testability.

Design: Modelling of internal structures in terms of data and control path on register transfer level. Verification by simulation and synthesis of netlists. This was done by the FU at the FU’s site. The HNI supplied on demand expertise on various issues like synthesis
or design. This was made on an informal way. Thesys provided access to tools and services for the insertion of test structures.

Evaluation: In-system of the design using FPGA- and ASIC-prototypes. Set-up of required test environment. The HNI designed an evaluation PCB and supplied FPGA-know how. Thesys delivered ASIC-prototypes.

The following table shows the original workplan as outlined in the technical annex of the FUSE contract. Important milestones were:

- Months 1-3: Specification including a behavioural VHDL model
- Months 4-8: RTL design with synthesis, implemented testability issues
- Month 8: Sign-off
- Month 11: Delivery of the ASIC prototypes
- Month 12: Field test

<table>
<thead>
<tr>
<th>Activities</th>
<th>Month 1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Management</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Specification</td>
<td>Textual</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VHDL</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Training</td>
<td>Synthesis</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VHDL</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Manufacturability</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design</td>
<td>RTL-Design</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Evaluation</td>
<td>Prototype Production</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PCB Design</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Test, Certification</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The real workplan for the project is shown in the next table.
The textual specification was done as planned. During this phase there was an intensive interaction with the ASIC manufacturer concerning the package, the PLL, and several other fabrication-related issues. After the first two months the textual specification was ready. It included the physical behaviour of the component to be designed and its logical behaviour as far as it was not determined by the PROFIBUS standard.

The VHDL behavioural modelling was the first big problem during the AE. By the end of January it turned out that the behavioural model would not become completed within the planned time frame. The reason for the delay was a lot of additional work: In addition to the simple structure of the ASIC, different PROFIBUS standards for layers 1, 2 and 7 of the OSI protocol had to be considered to set up a behavioural description. The benefit from this task was an in-depth understanding of the PROFIBUS standard.

The design work package exceeded the planned time frame by more than 50 days. The reasons were several internal difficulties:

- The nature of the design is bit serial. Therefore very long simulation times for low baud rates were necessary. The consequence was to change the verification approach from simulation to emulation. The required additional effort of 1.5 months.
- It was planned to work with one single simulator, i.e. the simulator doing the gate level simulation should also perform the RTL simulations. Difficulties arose when it turned out that the Viewlogic simulator was not able to use the VITAL library of Thesys. The additional effort for the necessary change in the design route were again nearly 1.5 full-time months for one designer.
- Gate count problems influenced the design. The First User was forced to reduce the gate count of the design during a redesign phase.
- It was decided that the FPGA-prototype was to be pre-certified before sign-off. After some shifts it was examined by the FZI (Forschungszentrum Informatik, Karlsruhe), a PROFIBUS certification specialist. This took additional time.

During the sign-off process with Thesys we gained some experience in generating test structures and test patterns.
The place & route step completed without problems. A final timing analysis and post layout simulation revealed no problems. Thesys failed in delivering the prototypes within the promised time frame (5 weeks after final sign-off). It took them another month instead.

The planned and spent effort for every workpackage is shown in the following table.

<table>
<thead>
<tr>
<th>Task</th>
<th>First User</th>
<th>Subcontractor</th>
<th>Totals</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Role</td>
<td>Effort plan</td>
<td>Effort real</td>
</tr>
<tr>
<td>Techn. Management</td>
<td>Respons.</td>
<td>49</td>
<td>40</td>
</tr>
<tr>
<td>Training</td>
<td>Participant</td>
<td>28</td>
<td>22</td>
</tr>
<tr>
<td>Specification</td>
<td>Respons.</td>
<td>52</td>
<td>53</td>
</tr>
<tr>
<td>Design: PCB / µC application</td>
<td>Respons.</td>
<td>116</td>
<td>155</td>
</tr>
<tr>
<td>ASIC manufacturing &amp; Evaluation</td>
<td>Respons.</td>
<td>20</td>
<td>48</td>
</tr>
<tr>
<td>Totals</td>
<td></td>
<td>265</td>
<td>318</td>
</tr>
</tbody>
</table>

*ASIC prototyping costs

During the preparation phase of the Application Experiment and within the specification tasks, a risk assessment and a contingency planning was made together with the subcontractor and the TTN. The result was the additional intermediate FPGA step in the design flow. This allowed to check the FPGA based hardware under real conditions which guarantees the functional and electrical correctness of the design much more reliable than only a -even very detailed -simulation can do. For the FPGA design several iteration cycles for test and logical modifications were planned.

The implementation of the FPGA design into the ASIC was made using the tested component library of the manufacturer, the subcontractor had the necessary design experiences. From this side, a risk could be excluded.

In a common specification review between First User, subcontractor, the TTN and the ASIC fab all electrical requirements and the structure of the design were checked against the parameters of the chosen 0,8 µm CMOS technology. The result of these discussions was, that there should be no technological risk. For the case of still existing logical errors, a second run was scheduled, which was fortunately not necessary for the prototype, but for the industrialised ASIC later on.
10. Subcontractor information

Our intention in the Application Experiment was to learn how to manage such a project and to become familiar with VHDL based digital ASIC design methodologies. Furthermore, we were interested to gain experience in corresponding test methodologies for both components. The objective was to be able to design digital ASICs ourselves in the future (except layout generation) and to become a qualified partner for a foundry. We wanted to be able to manage such a process from the first ideas up to the product test. That’s why we were looking for a subcontractor with the following competencies:

- experiences in training activities for project management, VHDL based system and digital ASIC design methodology
- know-how in “Learning-by-doing-methodologies” for this kind of work
- longtime experiences to co-operate with ASIC customers
- know-how and references in ASIC design and simulation
- good relations to ASIC manufacturers (not only to one of them)
- application-orientated technology know-how (how to implement and to test such a component in the final product)

Starting from these selection criteria, two subcontractors were chosen:

**Heinz Nixdorf Institut (HNI)**

The group “System and Circuit Technology” within the HNI carries out research in circuit design and development of microelectronic systems. Digital, mixed or analogue ASICs are designed in full custom, Standard-Cell or Gate-Array technologies. The HNI is located in Paderborn only 40 kilometres from Detmold. The main tasks were consulting and training on simulation, synthesis and design organisation issues. The HNI was involved in the final decision which ASIC vendor to choose.

Except the training courses, HNI was not responsible for any decision during the design. Its role was restricted to a consultant observing the progress of the FU and giving design assistance.

**Thesys**

Thesys was the ASIC supplier for the AE and also provided the access to tool licenses (synthesis and test insertion). The insertion of test structures and the generation of test patterns was done in close co-operation at Thesys’ site. The company has it’s own semiconductor foundry based in Erfurt, Germany.

Special penalty clauses going beyond the common terms of business were not included in the contract. Weidmüller owns the ASIC solution, i.e. IPR is clearly defined. There was an additional mechanism included in the contract: In case that the ASIC development work with the subcontractors would have resulted in innovative results suitable for a patent, Weidmüller would have been the ownership option.

11. Barriers perceived by the company in the first use of technology

The staff of the electronics department knew about the importance of microelectronics to innovate products. However no ASIC project was executed before the Application Experiment. It still needed a program like FUSE to encourage the organisation to start such a work. The reasons and barriers are given in the following paragraphs.

**Volume**

WI developed and still produces a huge number of different products. Products are often specialised for certain applications and customers. That means a great diversification in products of only medium volume. But this is typical for the whole market. Compared to consumer or automotive electronics, in most cases volumes in industrial electronics are much lower. Due to economic reasons, the effective
application of ASICs requires to have volumes of 10,000 per year or more. Only few products of the FU are above this barrier or are aiming to cross it.

**Management barrier**

At Weidmüller the usual time constant to get a product to market is between 3 and 9 months. When the marketing department defines a product it always urges the organisation to deliver it as soon as possible. This reliably prevented the use of application specific microelectronics solutions. Incorporating ASICs in products needs more predevelopment or the decision to start an ASIC project in an early stage of the product definition process. This was mainly a cultural and management barrier, as the marketing department is thinking in functions of the product but not in technical solutions.

**Risk of design failure**

The ASIC business (except FPGAs) is inherently risky, as patches cannot heal bugs. In addition the time-to-market pressure, the risk was very high, because the company had never done an ASIC design before. This means higher development times and costs combined with additional risks, altogether resulting in a strong financial barrier. Nobody in the company could guarantee the success of such a project without external assistance in management and design. Therefore we had a strong start-up barrier.

**Barriers during the project**

The First User was not experienced in doing such a design. Therefore, unforeseen problems within such a complicated project development could not be evaluated (real capability of design tools, contradictions between promised technology features and reality, company internal issues,...).

**12. Steps taken to overcome the barriers and arrive at an improved product**

**Volume**

The key element for overcoming the above mentioned barriers was to find the right application. Due to the time-to-market pressure from the marketing department it was impossible to include an ASIC development in a classical product development.

The solution was to find a product for the know-how transfer that surely promised to cross the volume barrier and to check it for cost saving potential. This constellation had the outstanding advantage that the risk of design failure or delay was avoided. Even in the worst case of total failure sales and production of the existing product would not be affected, the PROFIBUS I/O module worked with an ASIC bought from our competitor.

**Management**

To identify a technology which offers the chance to improve the product it was necessary for the FU to know the technological and cost structure of the product. A number of technologies was discussed which were applicable to that product. The common review of the technologies between management, R&D and the subcontractors showed possible improvements in terms of product features and costs.

The knowledge of the cost structure allowed to calculate the financial advantages of the application very clear. Together with a good understanding and estimation of the product’s market it was possible to calculate the ROI an Payback Period quite exact.

In this way, the management barrier was overcome, which is typical for a First User of a technology.

**Risk of design failure**

The design risk was minimised by the continuous support of the subcontractor. Based on training courses in VHDL based design methodologies, ASIC test strategies and an introduction to the tools it
was possible to do the work very self-standing. Continuous reviews of the results guaranteed an optimal design flow and correct results.

So the whole problem was reduced to the financial barrier. This was overcome by a management decision to acquire microelectronics experience which was based on the management related know-how transfer in the Application Experiment (chances of microelectronics, ASIC related issues like price-performance, project planning etc.) and the confidence that such a first design should succeed with external assistance in a reasonable time and a minimized risk.

**Barriers during the implementation phase**

During the execution of the Application Experiment, the project had to face four barriers

1. **Shortcoming of budget**
   For the first FUSE proposal, the original estimate of the project manager concerning the amount of work necessary for the project had been reduced significantly by the intended subcontractor. It suffered another reduction by the external expert who evaluated the proposal. When exceeding the budget it became very important to convince the management that the project was still advancing and under control.

2. **Internal priority of the project**
   As this ASIC project was carried out internally by the development department pressure from the marketing due to problems in other project affected the ASIC design team. Sometimes it was perceived as source of manpower.

   Overcoming this barrier was possible by high motivation of the team members that realised that ASIC design is their own and the company’s future. There must be a high awareness of the importance of such technology projects.

3. **The risk of market entry**
   The risk of entering the market with a component which could eventually not be 100% compatible with its counterpart from the market leader. The certification against the standard by external experts was not enough. It was overcome with extensive tests, because even a correct-by-standard design caused problems.

4. **Partial failure of the proposed design route**
   The used simulation tool – FUSION from Viewlogic - offers three options to simulate netlists. When one option – VITAL – failed, it was possible to switch to another. The chosen simulation type was a gate-level simulation using the Viewsim-option of FUSION. This barrier was overcome by a substantial change in the design because the original VITAL-based simulator input had to be converted into a Viewsim input. This means the textual VITAL input had been converted into schematics. The hierarchy, which connects the single modules, had to be drawn by hand.

   The only chance to uncover such problems in advance would have been to carry out a test project through all project stages. Information gained from the tool vendor are not reliable enough. Considering the substantial effort for such a test project it seems not feasible to do so. Therefore such problems can only be avoided if one knows its design route quite well – and even our experienced design house had problems. Therefore, this problem could not be foreseen.

13. **Knowledge and experience acquired**
   Within the Application Experiment, the planned know-how transfer was completed successfully. All experiences were transferred as planned. In detail, the following skills were acquired by training, consulting and learning by doing. Except the application specific Profibus know-how, they are necessary for doing a typical digital ASIC design flow starting at system level:
• In-depth PROFIBUS know-how
• How to write a good specification
• VHDL design (RTL and behavioural level)
• Synthesis aspects of VHDL designs
• In-depth know-how of the ASIC-tools used in the AE
• verification strategy, set-up of ASIC test sequences
• How to implement a test strategy for the field test of ASIC products

In addition to this rather specific skills an overall understanding of an ASIC design process and its management has been gained. The crucial milestones and phases of such a process are well known by now. The FU had been forced to do some significant changes in the design route. So the FU learned to identify dead ends in a design flow and how adapt to this new situation. Also the interaction with an ASIC supplier including close co-operation in some steps, e.g. implementation of test structures, has been done. The FU has acquired the knowledge to set up and manage a wide range of microelectronic projects with various microelectronic technologies. Furthermore the general experience gained will be quite helpful if a completely new technology will be used. We think, that the company will be able now to introduce also other technologies into the daily business without having the barriers and problems mentioned above.

Our expectations were completely fulfilled, the knowledge gained corresponds to the planned results of the know-how transfer.

To encounter the field of microelectronic design a company has to acquire knowledge in various fields. On the one hand it is the knowledge what to design e.g. how define a certain logic device in VHDL. On the other hand one has to know how to design, e.g. which tools are required in which order (i.e. the design route). The ratio between these both tasks is around one to one. The first part can be quite good covered with literature and training courses. The second part is harder to achieve because the huge number of combinations of tools and their interaction cannot been covered in a specific course. Therefore the design route is usually specific for each company and has to be developed there, too. If a company starts microelectronic projects from the scratch, she will be well advised to take counsel for experienced persons either by employing them or by consultation.

14. Lessons learned

This section covers the difficulties of the project and the related lessons that have been learned in order to avoid the problems in future ASIC design projects. We want to give potential replicants an advice, what can be avoided from the beginning of a project:

1. Management issues:

   The planning of a technology introduction project should be done on the co-operation base with an experienced partner and an own overview you should have before (a short training course, literature, but also own generic structures like holiday planning or writing of product orientated specifications which are similar in each project). A market survey and an economic forecast are necessary to justify the investment costs for the new technology. A workplan must be set-up (including enough time reserves for the daily business). Subcontractors must be selected carefully. They should have enough references in the kind of projects you intend to do. The evaluation of the subcontractors work can be done by results: does it work, are my questions answered?

2. Technical issues

   • A behavioural description of a design is as complex as the design itself

      Even if the behavioural approach seems to be easier than the final hardware design - it is not. To describe the behaviour of a system in VHDL requires much more skills than just to “say how it should behave”. To find a proper abstraction level and a good way to co-ordinate the interaction between the parts of the design needs time and demands different approaches.
On the register transfer level, coding styles and the structure of the digital devices are well defined. This makes coding on the RTL easier.

- **Simulations can take a long time**
  The verification of a ASIC design using a simulator might take a long time. Even if the RTL simulation goes rather fast it is to expect that the netlist simulation affords much more time. It is time-consuming to write the test bench i.e. to create a suitable simulation environment for the design.

  One company starting with microelectronic design might consider to buy sufficiently fast computers for simulations or to use FPGAs for design verification in the “real world”.

- **Don’t use schematics for complex systems. Design with VHDL at system level**
  The use of schematics may be fine to show the structure of a design block. But schematics can only be manipulated by hand. In addition they cause problems when importing and exporting netlists.

  One company starting with microelectronic design might consider to use schematics only for visualisation purposes. They should be a dead end in the design flow.

- **Use point tools instead of integrated design solutions**
  The design tools from Viewlogic were all integrated into the so named POWERVIEW framework. Although nice to handle in the beginning it becomes inflexible when the design complexity grows. Also a graphical user interface (GUI) prohibits the automation of tasks with batch jobs.

  One company starting with microelectronic design might consider to use GUIs only for setting up scripts or purely interactive tasks. Also the use of point tools makes it easier to switch to another tool if one shows flaws.

- **Single simulator approach**
  The netlist produced by the synthesis step should be fed directly to the simulator to avoid any difficulties with netlist conversions and schematics.

  One company starting with microelectronic design might consider to use either Verilog or VITAL to keep the data base for simulation purposes text based.

- **The first project with a new technology might exceed the budget**
  When planning a budget, the reliability of the results depends heavily on the experience of the employed people (process and technology knowledge). A new technology – because it is new – will cause serious uncertainties. If the budget is exceeded one has to decide to stop the project or to increase the budget. Commitment for a new technology is not only required to start a project but also to keep it going till it’s (successful) end.

  One company starting with microelectronic design should keep this mind. If no extension of budget is possible when problems should encounter, the chances for a successful finished projects are seriously reduced. An experienced partner should be contacted as early as possible.

- **Always expect a redesign**
  It is a rule that more than 90 % of the ASICs work fine for themselves, but only around 20 % work correctly in the intended application/system. Even with thoroughly testing and simulating a misunderstanding cannot be avoided all the time. For example textually defined standards always allow an interpretation. (This was a lesson learned in this AE).

  One company starting with microelectronic design might consider to expect a redesign - a second chip run with all delays and costs – as quite likely.

- **Tools can show flaws**
  Not every tool in the design shows the performance / reliability as promised by the vendor. If one tool is really suitable for the proposed role in the design flow can only be checked with a full scale project. Minor test projects and inquiries of the vendor can reveal some problems but one cannot
be sure that all problems remain uncovered. Also the effort for test projects might be quite high and therefore better placed on the real project.

One company starting with microelectronic design might consider to specify the task of a certain tool in advance and to start inquiries about this to vendors, other users, new groups and so on. A minor test project is an option too.

### 15. Resulting product, its industrialisation and internal replication

#### Industrialisation

The result of the Application Experiment was a working prototype. However, the PROFIBUS controller prototype WPS1 unfortunately revealed a flaw in compatibility with one program-block of a Siemens-PLC. Although standard compliance has been certified operating with a Siemens PLC, problems revealed in one case. The reason for this was a standard detail, which can be interpreted in several ways and is evaluated only in an optional program-part of the PLC. Nevertheless, the feasibility of a PROFIBUS ASIC was proven and the project gained a lot of interest within the company. So it was no question that the redesign was started to get the redesigned PROFIBUS controller – now called WPS2 - into production.

Taking into account that the flaw was well hidden the additional decision was made that the compatibility – the most important design goal due to the reputation of the company – has to be maintained under all conditions. Therefore an intensive evaluation program had been set up to gain even more knowledge about PROFIBUS-DP masters and slaves in general and the LSPM2 in special.

The following schedule for industrialisation was set-up and realised:

<table>
<thead>
<tr>
<th>Calendar week</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>KW 19/98</td>
<td>sign off for WPS2</td>
</tr>
<tr>
<td>KW 24</td>
<td>arrival of chip prototypes</td>
</tr>
<tr>
<td>KW 25</td>
<td>tests of chip prototypes</td>
</tr>
<tr>
<td>KW 26</td>
<td>redesign of bus coupler</td>
</tr>
<tr>
<td>KW 25</td>
<td>tests of bus couplers prototypes</td>
</tr>
<tr>
<td>KW 42</td>
<td>preliminary approval of chip 1st volume order</td>
</tr>
<tr>
<td>KW 47</td>
<td>1st volume production</td>
</tr>
<tr>
<td>KW 49</td>
<td>internal and external field tests</td>
</tr>
<tr>
<td>early 1999</td>
<td>production switched to WPS2</td>
</tr>
</tbody>
</table>

The usual time of 13 weeks between final approval and volume production could be reduced to five weeks by ordering a risk production. That means that Thesys not only processed 2 wafers to deliver prototypes, but e.g. 10 wafers. The processed silicon is not packaged and finally tested until the final approval.

The total industrialisation costs of the redesign (including NRE costs) were around 75 kECU. No new tools were required, because there was no change in the design route.

As WI has chosen the gate array technology again, the prototype supplier Thesys also delivers production volumes. He gave also the necessary assistance to introduce the design into production.

The WPS2 replaces the Siemens ASIC called LSPM2 in the WINbloc modules for Profibus. Because compatibility was one major design goal the marketing and production test stay the same. Due to the fact that the product is already launched, time-to-market is unimportant.

The effort to change the WINbloc-modules towards the WPS2 results in additional industrialisation costs of around 30 kECU, i.e. the total industrialisation costs are 105 k€.
**Internal replication**

Within the Application Experiment, a small ASIC design group consisting of 2 - 3 engineers was established which is now able to replicate the know-how with a next ASIC design. It will not be necessary to get support from the subcontractor HNI as the skills acquired are sufficient to do it on its own. But still access to synthesis facilities like those of Thesys will be required in future projects, as WI cannot afford those tools. It should be stated here that despite the overall experience with Thesys was really good, WI is not bound to this vendor. The design route implemented is compatible with most ASIC vendors and is also applicable for FPGAs.

As a consequence from the problems experienced during the design flow the EDA (Electronic Design Automation) soft and hardware needed some "reshaping". First of all the workstation hardware has been replaced by a Sun Server. The server approach fits very well to WI needs as it provides maximum computing resources in one big piece. NT-based solutions would be distributed, therefore it would be impossible to use all bought computing power for one big simulation. Any member of the design team can access the Sun Server using an X-Windows emulation on his PC. As ASIC design is not graphics intensive, this approach is absolutely feasible. So it is not necessary to equip any workplace with a high powered Windows NT workstation.

The software owned by WI was also upgraded. Especially Verilog simulation capabilities have been added. This capability would have been nice during the AE.

A second ASIC project has already been launched dealing with a mixed-signal design. The resulting ASIC shall be used in another high volume application.

**16. Economic impact and improvement of competitive position**

Although the awareness for the importance of microelectronics and FUSE funding were the triggers for starting the project economics is the ultimate measure whether ASIC design is useful or not. During the project this was the key motivation factor to hold on and to bring the project to a successful end.

Unfortunately, no absolute figures on WI's cost structure can be given here. Only relative numbers can be given which will not result in any pressure from customers or competitors. More detailed figures may only be revealed in a confidential environment.

The intention of the AE was to increase the FUs market share by reducing the price of the product. Secondary there might be improvements in the competitive situation due to the presentation of technological competence. But such effects are nearly impossible to predict. No really new markets will be entered due to the very specific application of the AE.

The market for industrial fieldbus systems is still emerging and even without the product improvement WI would achieve a significant increase in sales figures. Realistic projections show 50 % per year. The product improvement will bring Weidmüller at least 20 % more orders per year as projects may be won which have been lost before due to price reasons. This results in the diagram shown below. The volume is given relative to 1997 (100 %).
Relative increase of turnover for old and new product (1997=100%)

This results in the following additional turnover, only coming from the additional sales (1997=100%):

This corresponds at least to additional profits in the same order, regardless the price reduction which is the source for additional profits. The payback period, i.e. the time in which the FUSE investment is returned by profits is quite short. Based on the present prices and sales numbers it will be about six months. We estimate that the overall costs of the AE will be returned within two years, if sales prices remain constant. This forecast is not calculated with the FUSE cost structure, which includes only direct costs. The real cost structure of the FU is much higher as it includes all overheads like building and equipment cost. On top of this it includes the cost for the redesign and the industrialisation, which are not part of the application experiment.

The return of investment is hardly predictable because sales figures can only be roughly estimated. On the one hand new products entering the market can reduce WINbloc-sales, on the other hand the FU might develop new products based on the ASIC and gains higher profits compared to a LSPM2-based solution.

Assuming a product life time of 3 years, the return-on-investment for the FUSE funding (92 k€) will be about 500%. Because of our market knowledge and the existing sales figures we are confident to reach this goal. The payback period is about 6 months.
17. Target audience for dissemination

Weidmüller is the typical representative of a mid-sized company, originally coming from the mechanical/electromechanical sector. The company has many experiences in lower microelectronics technologies. Expertise in PCB design according to EMC regulations and the design and manufacturing of electronic components for industrial applications. Expertise was existing in PCB design according to EMC regulations and the design and manufacturing of electronic components for industrial applications. Except from the management point of view, the company had nearly no psychological barriers to introduce new innovative technology levels at all. The factors preventing this up to now were missing skills and not available resources to manage and to make such a project.

That’s why the methodology used for know-how transfer in VHDL-based digital ASIC design, its technical contents as well as the management experiences of the company can be very useful for further dissemination. Possible target companies can be:

• From the management point of view:
  – Companies with a similar technology level, and the same pressure to improve their products (independent from the industry sector)
  – Demonstrating the benefits of this AE and the steps taken to overcome the barriers will help them to initialise such a project, too.
  – Furthermore, the management activities and experiences are a good example that can be used for common training activities in this field.

• From the technical point of view
  Companies that want to introduce hierarchical, VHDL based, digital ASIC design with already existing knowledge in common digital design methodologies.

  This target group is independent from the industry sector.

• From the application point of view
  Companies in the areas
  • Electrical Equipment (Prodcom Code 3100, especially 3120 Electricity distribution and control apparatus)
  • Industrial Process Control Equipment (3330)
  • Instruments and appliances for measuring, checking etc. (3320)

A replication within Europe should be also possible for the same target groups as described above. The ASIC introduction will be more and more necessary also for companies with main businesses besides the “microelectronics main stream” in order to survive. On the other side, just these firms have a lot of barriers as we had. The experiences we made are useful for them. That’s why this AE has a good added value for the FUSE portfolio. The First User is willing and interested in attending workshops in order to disseminate its experiences and make it available to any interested company.