

**FUSE demonstrator document**  
**FUSE Application Experiment EPC1 1003**

**Monitoring TTN: IAM F&E GmbH, Braunschweig, Germany**

**Mixed-signal ASIC for Drive Control**  
**ASIC achieves cost reduction of 15 – 50 %**

**Abstract**

Hauser Division with 215 employees and a 1997 turnover of 25M€ develops, manufactures and sells servo drive controllers and automation components. Products are sold to automation companies or end users that have own resources for planning and building automation systems. As part of the FUSE project, a mixed signal ASIC has been developed that implements all peripheral tasks of a drive controller and – together with a digital signal processor (DSP) – forms the basis of the controller's microelectronics hardware. The controller is used for control of inverters that supply power to drives, which then move parts of machines or goods. This way speed, torque and other parameters of the drive can be controlled.

The ASIC is used to improve the COMPAX family of digital drive controllers for synchronous and asynchronous motors. The old COMPAX was based on one DSP, several digital ASICs and a number of separate analogue components. The product series has many uses, but is employed mainly in applications with fieldbus communications, the packaging machine industry becoming increasingly its main user.

The use of a mixed signal ASIC enables a reduction in material and production costs on one hand and a reduction in size of the microelectronics components on the other. In addition, reliability is increased through a reduction in the number of system components. Functional expansions in ASIC permit a flexible use of the controller in a variety of applications, while a flexible interface to the CPU and the ASIC's clock frequency permit an improvement of the closed loop algorithms with powerful high-speed DSPs. This is achievable thanks to higher sample rates and more complex control algorithms.

The duration of the project was 26 months, 10 months more than planned; it commenced in August 96. The project costs were estimated at 250.000 €, and the payback period at 1 to 1.5 years. The figures result in a return on investment of 250%. In the course of the project, the FU was able to gain experience in project management, design flow and test generation. This experience will help to improve further products. The FU worked in co-operation with a design house and a supplier of semiconductors as subcontractors.

Production costs of a digital servo drive can be considerably reduced with use of the new ASIC. Whilst production costs of a single axis unit is reduced by approx. 15%, the effect is even more distinct for a two-axes unit where the reduction

amounts to approx. 35%. For a 3-axes control the costs for required micro electronics may be reduced by up to 50%.

### **Keywords**

Mixed-Signal ASIC, axis drive controller, servo controller, comparator, pulse width modulation, inverter, packaging machine

### **FUSE Sinature**

5 0192 556 0311 2 3330 2 33 D

## **1. Company name and address**

HAUSER Division of  
Parker Hannifin GmbH  
Robert Bosch Straße 22  
77656 Offenburg

Co-ordinator of the experiment  
Manfred Stern  
Tel.: +49 781 509 120  
Fax: +49 781 509 129



## **2. Company size**

Hauser has a total of ca. 215 employees. These employees are active in the Components, Systems and Machines business unit (BU). The components BU comprises the subdivisions electronic components and mechanical components. Today, Hauser sells several thousand drive axes per year, which are generally used as compact individual axes in a variety of machine and system applications, but also find use as components in complete Hauser automation systems. On this basis, the company achieved a turnover of about 25 M€ in 1997.

The electronics subdivision has ca. 50 employees in its development, production, marketing and sales departments. About 15 employees are active in electronics development, which is divided into microelectronics, software, power electronics, PCB design and housing design. In the microelectronics area, technologies such as microprocessors and microcontrollers, FPGAs and digital gate arrays are used. The majority of microelectronic PCB components is manufactured using SMT.

Three years ago, Hauser became a member of the worldwide Parker Hannifin Corporation based in Cleveland, USA. In the Automation group, Hauser is responsible for electro-mechanical motion control. The industrial activities of the Parker group are mainly in the hydraulics, pneumatics and fluid connector sectors.

## **3. Company business description**

The Hauser Division represents the industrial sector of for motion automation in industrial production processes and transfer tasks of the Parker group. Basis for

the activities is the use of electrical drive technology with control electronics, servomotors, gear boxes and mechanical feed devices. Its core business is development, production and marketing of electronic and mechanical components. The components are sold to OEM and end customers, that build or install automation equipment. Components are used in automated machines for handling and packaging of goods as well as for tooling machines.

Electronic activities focus on the development and manufacture of simple control systems and complex servo controllers. Mechanical work covers the development and production of mechanical linear units. Functional elements such as AC motors and gear boxes are offered under the Hauser name in co-operation with third parties. A common marketing and sales structure applies to both areas.

Beside the components business, Hauser is also active in the system and textile machine market. Both areas use the existing product range of the components section, and are therefore customers of the electromechanical component product offering.

#### **4. Company markets and competitive position at the start of the AE**

Especially in Germany, but also in other European countries, the drive engineering market is extremely competitive. In Germany alone, approximately 50 manufacturers are trying to market their products, including several large companies (Siemens, Indramat, Bosch, Lenze, etc.), a large number of medium-sized manufacturers and a smaller number of small companies. In terms of its turnover, Hauser is firmly positioned as a medium-sized company with a market share of about 5%.

Due to its early entry into the digital drive market, Hauser has made a name for itself as a supplier of advanced powerful drive controllers. This also is the major strength of Hausers products. They are valued for high performance for specific applications and for high quality. This technological advantage has been reduced in recent years by other suppliers' migration towards digital technology. This situation was made even more significant because a considerable number of competitors have made the move to digital technology in a joint project. The result has been a significant increase in competition and an accelerated drop in prices. The current price for a typical axis control is around 250 €. This price is multiplied by the number of axis required for the entire system.

Currently manufacturing costs of Hausers high performance controllers for customer-specific solutions are too high to be competitive against major companies. Also the low-performance controllers are still too expensive for the evolving market of extremely price-critical applications for small devices and consumer applications. Over the past years the sales figures could be maintained due to high quality and good service, but the economic situation for these product segments worsened. After three years the sales figures are beginning to drop and revenue can only be maintained by savings of production costs. Therefore, Hauser needs a new device that allows design of cost effective implementation of high-performance customer-specific solutions and a new device that can be used for price critical applications with a fixed configuration. A cost reduction of the basic building blocks of at least 10% is required. Additional savings will then allow to spend extra effort on the adaptation respective configuration of the device to customers needs. The two markets of low-cost controllers and highly customer-specific controllers appear to be an important market opportunity for Hauser Division.

Despite this situation, Hauser currently is still able to maintain its position because of its growing expertise and its experience in the software field. Negative influences are expected to be a price drop in the short term and predatory pricing in the medium term.

Due to continuing advances being made in the field of microelectronics, the number of competitors is expected to grow even further in the medium term: on one hand, Far Eastern suppliers are already making inroads on the European market with aggressive pricing policies; on the other it is expected that suppliers of related products, especially of frequency converters, will want to enter the market sector. Even with the predicted market growth of approximately 10%, there will not be enough room for all suppliers: competition will continue to grow.

Beside the COMPAX family – the subject of the FUSE project – Hauser offers a series of analogue servo control devices. The OEM products area is also responsible for a significant proportion of the total turnover, representing ca. 25% of the electronics turnover with its customer-specific drive controllers. In addition to hardware components Hauser also sells control software for its systems.

Moving material is a central aspect in production systems. In the future, there will be even more sophisticated handling systems that require drives and drive controls. Handling systems in totally automated machines and plants and in the private domain may offer new market opportunities for Hauser division. With new concepts for small and inexpensive drives and controllers, which are only possible with highly integrated, flexible and powerful controllers, Hauser division plans to participate in this increasing market. Products in this market segment support Hauser division in maintaining and possibly extending its market share even with increasing competition.

## **5. Product to be improved and its industrial sector**

The product to be improved is the COMPAX family of digital drive controllers from Hauser. COMPAX is a first generation digital drive controller, whose hardware is based on a digital signal processor (DSP) system and a digital application-specific integrated circuit (ASIC). All active functions are implemented by software. Beside the main components – DSP, memory and ASIC – a larger number of discrete components are required. The complete peripheral and optional functions are implemented in the controller by means of a plug-in module system. Particularly the conversion of analogue measurement values, such as phase currents, intermediate circuit voltage, temperature, etc. is very component- and cost-intensive.

Due to its plug-in technology, COMPAX is very flexible and can be configured for a variety of application tasks. The main drawbacks of this flexible approach are the resulting size of the assembly and the high manufacturing costs. The resulting costs, together with the growing competition, have limited the market success of the series in the simple servo applications sector.



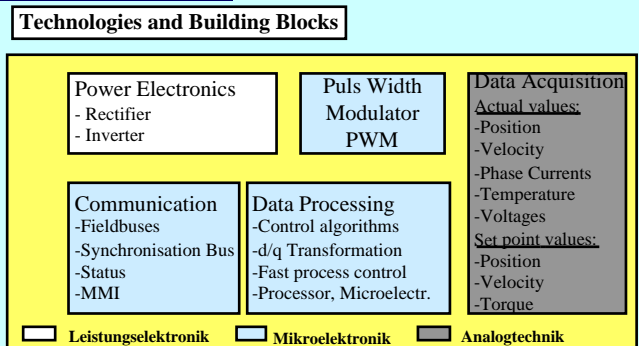
The initiation of the PAP concept was sparked off by discussions with customers – manufacturers of multi-axis machines – who, due to the increasing cost pressure, cannot see a satisfactory solution in the products available today. Through the use of PAP drive controllers in multi-axis robot applications it will be possible to expand the market segment supplied by Hauser. In terms of price, installation space requirement and performance, the concept fulfils the requirements to satisfy various manufacturers of robot controls and robot systems.

The most essential components of the existing COMPAX are the communication unit, the Host System and the DSP System. The communication unit, consisting of a plug-in-board, is available in Interbus S, Profibus or CANBus versions. In addition to the various CPUs another major component is a Gate-Array which includes the digital I/O and serial communication, a complex Gate-Array with PWM-function Up/Down Counters and a R/D-converter for positioning detection.



Original COMPAX controller card  
a

## PAP-Project - Servo Drive Building Blocks



Building Blocks and Technologies of Servo Drive architecture

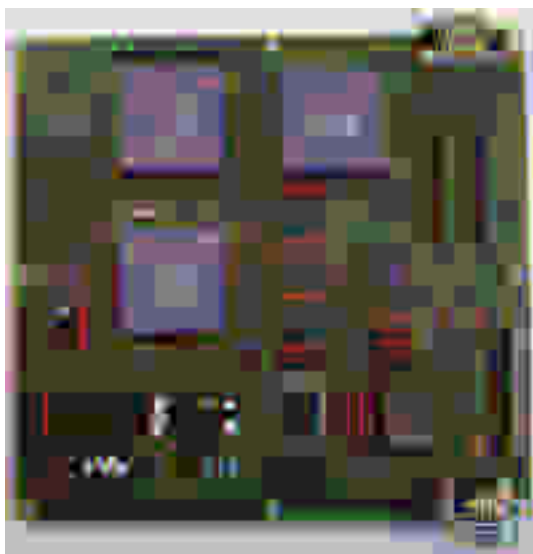
The competition in this market is increasing. Therefore, Hauser has to improve performance and functionality of its products and lower production costs by preferably about 10% per axis control.

## 6. Description of the technical product improvements

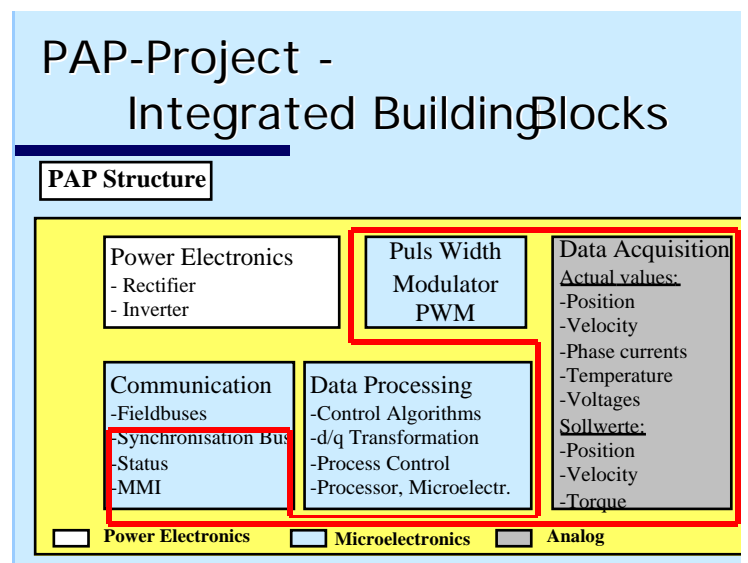
The salient technical advantage of the new COMPAX family is that a more flexible, faster hardware system can be achieved with a significantly reduced number of components.

In particular, the advantages are:

- Manufacturing costs: Fewer components and standardised SMT permit a reduction in manufacturing costs. The cost saving results from a reduction in material costs and shorter manufacturing and testing times. The elimination of analogue calibration and the design-for-testability in particular result in shorter production times. A reduction in manufacturing faults and a higher production throughput are largely the result of the reduced number of components. All improvements together lead to a cost reduction of about 15% per axis for most control systems.
- Product performance: The greater flexibility of the PAP ASICs means that the new COMPAX can be easily adapted to the requirements of a particular application. Additional functions in the digital part of the ASIC permit the use of COMPAX in new applications. The increased clock frequency of 40 MHz and a faster interface to the signal processor (DSP) have enabled a significant increase in the DSP's arithmetical performance. The practical implications are improved control dynamics, better, more complex control algorithms and new control structures.
- Scalability: The mixed signal ASIC provides a flexible interface to the processor and to the analogue measurement devices. The CPU – adapted to the corresponding task – can be selected from a multitude of processors (8, 16, 32 bit) and signal processors to suit the task. On the analogue side, the PAP's internal ADCs and DACs can either be used, or external high-performance converters be connected via the integrated interfaces. The PAP architecture thereby provides elements of a universal drive controller toolkit, with which a servo controller, optimised for any application, can be developed and manufactured easily and quickly. This property offers advantages in addition to those of the COMPAX family, which can in future also be employed in previously analogue controllers.



New three axes PAPGA prototype



PAPGA integrated Building Blocks

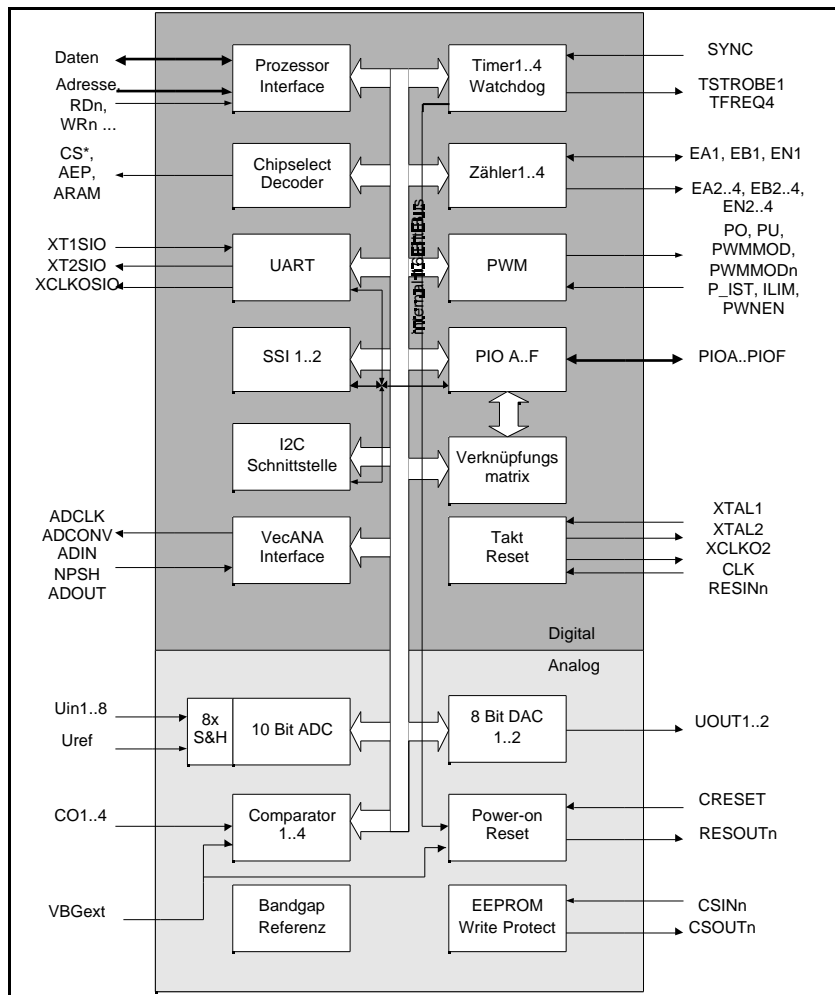
The PAP architecture, as sketched in the above block diagram makes it possible that a number of hitherto discreet components are integrated in one single chip. Essentially the new system only consists of the CPUs and the PAPGA-ASIC. PIOs, serial interfaces, PWM, A/D- and D/A converter and the R/D-converter function, all are integrated in one single component. In the above picture they are enclosed by a red line. To allow simple adjustment to the corresponding application requirement the communication system continues to be a separate unit. For this reason the communication function in the PAP-system has been designed as a plug-in board.

As demonstrated by the block diagram use of additional PAP-ASICS with one DSP allows the realisation of two- or three-axes controls. Only the ASIC itself plus the connection plug to motor and resolver are required for integration, whilst the CPUs may be jointly used for several axes. The resulting price savings and reduced component dimensions are considerable. A higher internal frequency for the digital part and a higher analogue sampling frequency of the PAP-ASIC in comparison to the existing product allow better control of dynamic processes. Free selection of processors allows maximum flexibility.

	Existing product (example)	New product
Analogue interface	Off-chip	On-chip
Analogue sampling frequency	120µsec	7µsec
Analogue inputs	3	8 (multiplex with S&H)
Digital (internal) clock frequency	20 MHz	40 MHz
Processor	Internal (16 bit)	External (freely selectable 8, 16, 32 Bit)
Interfaces	proprietary	Standard (e.g. I_C)

Comparison of old controller and new Mixed Signal ASIC

The mixed signal ASIC is realised in 0,8 µm technology. The chip area measures approx. 85 mm<sup>2</sup>, the digital part dominating with approx. 80% of the space. The chip is integrated in a PGFP-housing with 208 pins. The most important analogue components are the 8 A/D channels, 2 D/A channels and several programmable comparators.



**Blockdiagram of the Mixed Signal ASIC**

## 7. Choices and rationale for the selected technologies, tools and methodologies

A mixed signal ASIC approach was used as the basis for product improvement. The design is partitioned into about 80% digital and 20% analogue functionality. Due to the need to integrate both digital and analogue functions in a single component, alternative approaches such as FPGA were not considered. A possible alternative would have been the multi-chip module (MCM) technology (ASIC with DSP together). This approach was investigated. It was shown, however, that it would not stand up to an economical investigation due to the high degree of integration and the expected turnover volume. It is evident that the chip manufacturers (DSP, digital ASIC, etc.) are not prepared to consider co-operation below an annual supply volume in higher five-figure numbers. Without this volume, the MCM approach fails. MCM could be regarded as a further future improvement, if the commercial requirements can be fulfilled as well as the technical ones. For volumes lower than 10.000 units per year the MCM solution is not interesting.

A further possible option would have been the division of the PAP functions into an analogue and a digital ASIC. The main arguments against this approach are the resulting price and the required circuit board area.

- For part of the chip design available library elements of the semiconductor manufacturer were used. The A/D converter is a new development by the Design-House since the manufacturer was unable to provide a library element with the required specifications.

The design was done in close co-operation with the subcontractor. Different tools as used by the subcontractor were used for individual design steps like design entry, simulation, layout electrical rule check etc. E.g. the digital design was done using workstation-based synopsys tools for VHDL entry and simulation. The design rule check after layout was done using the tool Dracula/Diva.

The design was done in a bottom-up manner. After specification of the entire system the submodules were designed and tested individually. At this level also first optimisation measures were applied. However the advise on whether and how to optimise was mostly given by the subcontractor, who could compare the results with his experience. The modules have been optimised with respect to timing and size. The timing can be measured as register performance, which gives the maximum delay between any two FlipFlops in the module. The size can be measured by gate equivalents or silicon area. Then, after availability of all submodules they were combined to a system design and interaction and overall functionality was verified. At this level optimisation measures to improve module interaction and reduce overall size. In parallel the analogue part was mostly prepared by the subcontractor. After successful verification the layout of the design was prepared. Then the physical design again was verified. This is mostly done by comparing pre- and post-layout simulation results. Finally an electrical respective design rule check was performed. Then the design was handed to the semiconductor vendor for production.

The more detailed design flow in a mixed-signal-ASIC project comprises 12 steps. Every design step includes different actions and is closed in most times with a review.

The design steps are as followed:

	<b><u>Reviews (Reviewer)</u></b>
1. specification	specification-review (PL, SV)
2. design handbook	design-handbook-review (SV)
3. test specification	test specification-review (PL, SV)
4. schematics/simulation of module	concept-review (PT)
5. schematics/simulation of the systems	design-review (SV)
6. floor planning	
7. layout of modules	module-layout-review (PT)
8. layout of the system	
9. post layout-simulation modules/system	end-review (SV)
10.GDS II-chip finishing	GDSII-review (AL)
11.measurements	measurement-review (PT)
12.documentation	

The temporally sequences doesn't follow the numeration of the points above.

For production a 0.8 $\mu$  CMOS technology was chosen, which is a good trade-off between analogue functionality and density of implementation of the digital partition.

## **8. Expertise and experience in microelectronics of the company and the staff allocated to the project**

As manufacturer of electrical drive devices, Hauser, with its COMPAX series, was one of the first companies to introduce digital control systems in the early 90s. The COMPAX controller distinguishes itself by the standardised implementation of control algorithms for position, speed and current loop in software and by the combination of microelectronics and power circuit in a single unit.

In the second half of the eighties, major development work was undertaken in the conceptual development of signal processing architecture (selection of the DSP, design of position, speed and current measurement methods), in developing a basis for the establishment of software algorithms for the various control tasks and in the development of a power output stage based on IGBT technology. The controllers are suited to the control of AC motors, both synchronous and asynchronous (induction).

Today, Hauser offers a family of diverse digital drive controllers for synchronous and asynchronous motors in the power range of 1 to 15 kW. Core of the Hauser controller is a digital signal processor (DSP) working in conjunction with a peripheral component using digital ASIC technology and a separate microcontroller as the host processor. For each drive axis, a DSP, a peripheral ASIC and the associated host processor system (for control and monitoring tasks) is required. Only with the digital peripheral ASIC was it possible to produce the completely digital drive controller in a usable form at a competitive manufacturing cost.

Hauser has many years' experience in the electric servo drive sector. In a broad field of applications encompassing textiles, general automation and handling tasks as well as applications for the semiconductor industry, the company was able to build up a wealth of application expertise. This knowledge, together with the know-how in digital control technology and the availability of powerful hardware, helps to secure the company's position in a market characterised by intense competition. Hauser involved engineers and technicians from its design and development department in this project. For years Hauser has been in the position to supply programmable technologies such as FPGAs and digital ASICs. Whilst the FPGAs are designed in-house and were also implemented internally, the ASICs were designed in co-operation with sub-contractors. An example for such co-operation was the VeCon project, which was done by a group of drive control companies. Hauser's engineers, production and logistics staff was capable of handling these and other standard products. Data sheets were available and components were purchased through distributors. In many cases components were selected with respect to availability of a second source.

As a result of the digital ASICs design company Management acquired a profound know-how of the handling of development and design complex projects. This included a certain amount of uncertainty during the design process. For Hauser it was impossible to be sure of reaching a certain milestone within a given time. Measures for forecasts and control of development timing had to be acquired. Engineers also learned the basic design tasks for digital ASIC design and got an insight into the tasks for analogue ASIC design. Experience in close co-operation with a subcontractor were also improved.

## 9. Work plan and rationale

The workplan consisted of the following workpackages and tasks:

Workpackage 1: Management

Task 1: Project management

Task 2: Dissemination

Task 3: Reporting

This workpackage was almost completely done by Hauser with some assistance from the TTN. The overall effort was planned to be 10 days but turned out to be actually about 20 person days.

Workpackage 2: Specification

Task 1: Functional specification of system

Task 2: System specification of component

Task 3: Technical specification of component

Specification was mainly done by Hauser, but the subcontractor provided much of the technological expertise. Result of this workpackage was a specification on which the further project was based. The specification was signed and agreed on by both partners. The effort was planned to be 20 person days and turned out to be 25. Subcontractor costs amounted to 9 K€.

Workpackage 3: Training

Task 1: Management training

Task 2: Specification training

Task 3: CAD training

Task 4: Design training

Task 5: Evaluation training

The training workpackage includes the basic training courses on the technology. Specific training was also done in the design and evaluation workpackages as training on the project. The effort was estimated to be 15 days but actually 25 were required. The subcontractor effort amounted to 23 K€.

Workpackage 4: Design

Task 1: System level design

Task 2: Subsystem level design

The design workpackage includes design of the ASIC and of the PCB for the prototype. This package was done in close cooperation with the subcontractor. Hauser did the system design and much of the digital ASIC design whilst the subcontractor did the analogue part and assisted Hauser with the critical digital functions. The effort was planned to be 90 person days, but turned out to be 135. The subcontractor costs amounted to 13 k€.

Workpackage 5: Evaluation

Task 1: Prototype production

Task 2: Test set-up

Task 3: Functional testing

Task 4: Prototype testing

Task 5: Field testing

The evaluation workpackage includes the actual production of prototypes and evaluation of the results during different tests. The effort for evaluation was estimated to be 30 person days, but actually required about 55. Subcontractor costs include the production of the ASIC samples and amounted to 30 k€.

Task	Effort for Hauser (person days)	Subcontractor costs (k€)
Management	20	0
Training	25	23
Specification	25	9
Design	135	13

Table of actual effort and costs

Due to unexpected difficulties and problems which occurred during the project time the project plan had to be modified. The following diagram shows the actual plan in comparison with the estimated plan with its major changes and deviations.

Acti	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	Rem
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
1																											
	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	X	X	X	X	X	X	X	X	X	X	X
	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	OX	X	X	X	X	X	X	X	X	X	X	X
2																											
	OX																										
		OX																									
		OX	OX									X	X														10
3																											
	X	O																									2
			OX																								
							O																				
							OX																				11
4				OX	OX				X	X	X	X	X														3,8
				X	OX	OX	O				X	X	X							X	X						4,9,14,16
5																											
							X	X	O	O	O		X	X		X				X	X	X					5,12,15,17
								X	O	O											X	X					6
							X	X	X		O	O				X											7,13,18
																OX	OX										19
																OX	OX										20

X – actual, o - planned

Major deviations between original and actual plan.

1. Dissemination after the project time.
2. Specification of system and ASIC one month earlier than planned.
3. Redesign of test PCB necessary because of some errors.
4. ASIC design ahead of plan, one month earlier.
5. PCB and ASIC production one month earlier than expected.
6. Test set up ahead of plan
7. Functional test of ASIC started earlier but took one month more than planned.
8. Delays in software development due to ASIC errors.
9. Re-Design of ASIC started due to unexpected errors.
10. Change in ASIC specs necessary due to the test results, re-design aspects and testability of the chip.
11. Test pattern and design training
12. Production of second samples
13. Test of second ASIC samples
14. Additional re-design (metal layer)
15. Production of new ASIC samples
16. Re-design of the ASIC because of problems in the A/D converter stage
17. Production of ASIC samples for prototype testing
18. Functional tests of the new ASIC samples
19. Prototype testing of the ASIC in the test bed PCB
20. Field test of the system on a test stand

The third samples of the ASIC arrived in December. The tests showed still a clear deviation in the analogue part of the chip. But apart from that the digital functionality

worked. A PCB with the ASIC has been completed. It was decided to make a new re-design to overcome the malfunction in the A/D converter section. Thus a new re-design cycle with design, prototype manufacture and several test levels have been initiated. The FUSE project has been concluded in September 98.

A number of redesigns are not uncommon for mixed signal ASIC designs. In our case the design of the fast A/D converter was very challenging and insufficient performance and functionality contributed significantly to the overall project delay. Deviations from the actual plan may have been less with more effort spent on risk analysis and contingency plans. However, basic risks like one possible redesigns have been considered and taken into account for contractual and some planning issues. However, the actually required three redesigns have not been anticipated. Therefore, the schedule had to be extended from 16 to 26 month.

For coming projects, Hauser will put more emphasis on the risk analysis:  
Which are the parts that contribute to the overall risk?  
Is there a work-around if certain components do not perform as intended?  
How high is the effort and are costs if parts of the system need to be redesigned?  
Especially with high requirements on analogue components risk analysis should also include the possibility of complete failure of a certain approach and technology. Risk analysis should also include a careful review of requirements and on how much certain requirements contribute to the risk of additional costs or failure of the project.

Throughout the project there was a close cooperation between Hauser and the subcontractor to assure knowledge transfer. Initially Hauser attended general training classes on digital and analogue ASIC design. Basic knowledge was deepened during training on the project. Hauser tried to implement the functions and was assisted and advised by the subcontractor.

## **10.Subcontractor information**

A number of demands must be made on the subcontractors to guarantee a calculable project schedule in a mixed signal development project.

The primary requirements are:

- **Experience of design house with MS technology**

The selected design company must have sufficient experience in the design of mixed signal ASICs. There is a significant difference between this and a design company having digital design experience, but being new to the field of analogue design and MS design. The integration of analogue components in an ASIC is more than just an extension of conventional ASIC design: it is a completely different world, governed by different laws with different risks and problems, a different production process with special requirements and specific requirements for the testability of the resulting component. A design company that cannot provide appropriate references must be rejected for the purpose of this project.

- **Experience of semiconductor manufacturer with MS technology**

To a limited extent the above also applies to the semiconductor manufacturer. The subcontractor should be familiar with the production process and the design tools and libraries must be stable.

- **Co-operation among subcontractors**

Whether the two subcontractors – designer and semiconductor manufacturer – have shared experience with the selected technology and design tools influences the risk associated with an MS project. Proof of a successful co-operation provides an indication that both partners speak the same language and that the interface between the two subcontractors is clearly defined.

- **Incorporation of design and manufacturing flow**

Even if the subcontractors are responsible for design and production, the FU must have sufficient detailed knowledge in these areas. Only with this knowledge can the FU perform its function as a competent discussion and negotiating partner and realistically evaluate all possible risks and costs.

- **Advance planning**

The method of testing the series components must already be specified in the definition phase. If this aspect is not taken into consideration, unpleasant surprises regarding redesign and costs can occur when series production begins. The testing procedure must be clearly defined in the specification manual.

- **Contractual safeguards**

The success of an MS development project depends to a large extent on the precise definition of the obligations and responsibilities of the individual project partners. The party responsible for redesign – and therefore the associated costs – in case of problems must be clearly defined. Without this definition, a project such as this can easily turn into a bottomless pit. To avoid delays in the project, a contract penalty could be agreed for late delivery. Even if it proves difficult to come to a contractual agreement regarding this issue, the effort will pay off since it will reduce the risk of delays and additional costs. It should also be understood that all resulting designs would become the exclusive property of the FU. This is one of the prerequisites for handing the design over to another design partner if desired.

In our experience, the contract definition is of greatest importance. Support from the TTN in advising the FU would be desirable in this activity. The subcontractor for ASIC design that was selected by Hauser has been doing knowledge transfer projects for small and medium sized companies for a number of years. They offer training classes on general aspects of ASICV design, like VHDL coding and others, supply consulting and perform contractual design of digital, analogue and mixed signal ASIC design as well as PCB. The subcontractor already had some projects for drive control applications. The semiconductor vendor selected as second subcontractor offered favourable conditions for the numbers of pieces required by Hauser. This may be a major problem with other semiconductor vendors that will not supply ASICs in small quantities of less than several 10k pieces a year.

For contractual safeguard of such a project it is absolutely essential that the handling of exceptional situations as they occur during required re-designs is clearly defined. I.e., it is of importance to unambiguously state the responsibilities

for the development result and the commercial responsibility for potential additional costs.

## **11. Barriers perceived by the company in the first use of the AE technology**

The mixed signal technology is a relatively new area of semiconductor technology. This means that a number of prerequisites for its application – especially in small and medium-sized companies – are missing. Important arguments against the use of this new technology under the given circumstances are:

- **Risk:** The reader of relevant technical literature will be aware of the risks associated with the development of a mixed signal (MS) ASIC: a high likelihood of several redesign cycles, a limited number of design companies with experience in MS design and a limited number of semiconductor suppliers capable of producing MS ASICs in sufficiently small batches and sufficiently experienced in the production of MS ASICs. An additional risk is represented by the achievable accuracy of the analogue components within the ASIC. Deciding on an MS design under these conditions therefore means committing to pioneering work.
- **Missing know-how:** Especially small and medium-sized companies do not, in general, have the subject knowledge required to estimate the risks of an MS design with sufficient accuracy. This applies to both the evaluation of the design and test tools and knowledge of the underlying conditions for ASIC manufacture itself. Because MS technology is still relatively new, the best general method of managing a project such as this and the precise processes associated with the development work are often not known.
- **Financing:** A relatively high capital investment is associated with the design process, prototype production and test program development. The high costs are partly due to the fact that the technology is relatively new. Another factor, however, is the limited number of design companies and chip manufacturers and the resulting lack of competition. Together with the high technical risk, the necessary capital investment represents too great a risk for medium-sized companies.
- **Cultural barriers:** Together with the insufficient available know-how, the developer is presented with an additional risk. Development engineers must be able to evaluate a problem, develop solutions and implementing these solutions using technological means. This requires a sufficiently detailed knowledge of the technologies and tools required to develop the solutions. In the case of MS technology, both of these requirements are missing: the tools are too expensive, as is the acquisition of the necessary knowledge. The decision to play a pioneering role in a new technology means that the participating development engineers must – at least to some extent – be dependent on third parties. This is not something developers are prone to do and requires a considerable measure of trust in the project partners (design company, chip manufacturer).

The combination of the above barriers would suggest that the move towards mixed signal technology is almost impossible to make for small and medium-sized companies.

## **12. Steps taken to overcome the barriers and arrive at an improved product**

That a significant product improvement can be achieved with an MS ASIC has never been in doubt: the advantages of the new technology were known, the objective and subjective backgrounds were the risk, missing know-how about the development process, financial issues and the fact that one would have to „surrender“ oneself to third parties to attempt the project.

An important step towards overcoming these barriers were discussions held with the TTN, who provided support mainly on the two critical points of **subcontractor** and **financing**.

- **Risk:** Steps to minimize the risk have been discussed with the TTN as an independent partner. The risk of redesigns was shared between Hauser and the subcontractor according to the responsibilities for certain functions. Hauser also minimised the risk by selection of an experienced subcontractor. Wherever design risks could not be controlled alternative plans (workarounds) have been considered.
- **Missing know-how:** The knowledge barrier was overcome by discussions with the TTN, general training courses and training on the project during joint implementation of the system with the subcontractor.
- **Financing:** Financial risks were limited by defining milestones to possibly stop the project when major objectives could not be met. Investments were limited by using some equipment from the subcontractor.
- **Cultural barriers:** The FUSE program gave the design engineers the freedom to acquire experience. Also selection for the program was a major psychological aspect.

Under consideration of these aspects and due to the fact that, thanks to the TTN's recommendations, the question of subcontractors and existing reservations could be cleared, the main barriers to the project were eliminated.

In the course of the project it became evident that the planned approach with one MPW run and easy adaptation in a redesign in the analogue area of the ASIC was not possible. The result of the first MPW run could not be used because basic design problems came to light. The approach chosen to resolve this dilemma was to create a new project plan together with all partners and to establish an alternative development plan. These problems resulted in a delay, which meant that the originally planned product release date could not be met.

Knowing the potential risks in a mixed signal ASIC project on one hand and looking to the benefits by using this technology Hauser Division will in the future still try to implement this technology. The decision to go for a mixed signal chip has to be done on a clear cost - time and risk assessment. Finally the technology can be handled and is a useful and powerful tool to reduce cost and size of new products. Thus the technology is worthwhile to be utilized even without funding.

### **13. Knowledge and experience acquired**

The main experience acquired in the course of the FU experiment are in the areas of

- project management of mixed signal ASIC project,
- processes of a mixed signal ASIC project,
- design flow of a mixed signal ASIC project,
- familiarisation with the discrete process steps and
- estimation work with respect to risk, required time and costs.

Further insights were gained with time in the areas of

- test program development and,
- basics, tasks and use of the development tools.

This set of necessary experiences have been defined with the help of the TTN and building up of knowledge on these subject was especially monitored during the project.

The greatest challenge – resulting from changes in the project sequence – proved to be project management. The original planning was based on the assumption that one multi project wafer Run should be sufficient to obtain engineering samples that conformed to specification from a digital point of view and would also basically work from an analogue point of view (except for minor parameter deviations regarding accuracy, drift and linearity). It became evident, however, that far more time and iterative stages were required to advance the project.

Initial experience showed that the scope of the specification – benefited by the flexible implementation possibilities with programmable logic – can easily grow in the course of compiling the specification manual. Here not only the feasibility of an additional function, but also the implementation of associated parameters (risk increase, project duration and resulting chip costs) had to be taken into consideration. Self-discipline is required in the specification manual phase to avoid the risk of exceeding the project schedule.

In a project such as the one being discussed here, it is vital that the two subcontractors – design house and semiconductor manufacturer – work together closely. Despite the fact that the schedule had been discussed in a joint meeting at the start of the project and the responsibility for the information flow management between design house and foundry had been transferred to the design house, this interface was one of the weak points in the project. Data transfer and necessary additional work were often only carried out after the FU lodged a complaint with both project partners. This poses a problem inasmuch as the FU is a relative newcomer to this technology and cannot, therefore, readily recognise and evaluate necessary actions and resulting risks for the project.

The FU is now able to manage a mixed signal ASIC design in the future and can assess the corresponding costs and risks.

#### **14.Lessons learned**

The most important insights gained in the course of the project can be summarised as follows:

- Co-operation with the subcontractors

It is vitally important for a project of this nature that the rules of play between the project partners are clearly defined. The interface between FU, design company and semiconductor supplier must be clearly described and the obligations of each partner specified. Potential points of friction between the partners should be

expected in the areas of project management, prototype testing and responsibility for test standards. It is important that all agreements are formulated in a clear contract. Here, the participation of the TTN is invaluable, since the FU cannot evaluate the potential dangers on its own.

### **Precise specification of tasks, project contract**

- Experience of project partners with each other

Although both subcontractors have participated in joint projects in the past, the PAP project was the first mixed signal project in which the design company and the semiconductor manufacturer took part together. The FU was not entirely aware of this at the outset of the project. In the course of the project, significant delays and problems arose because the design company was not familiar with the tools and libraries of the semiconductor manufacturer. On many occasions, the two partners worked on different assumptions, spoke two different languages.

### **Ensure that your project partners have experience with the application and the technology**

- Specification manual

The specification manual must not only provide a detailed description of the functionality and the electrical properties of the chips, but also specify the underlying conditions for testing and parameters such as technological limitations, chip size, max. test times, etc. At the same time, the FU must limit itself regarding the scope of functionality. Without a certain discipline by the FU, there is a danger that growing requirements lead to time overrun and excessive costs.

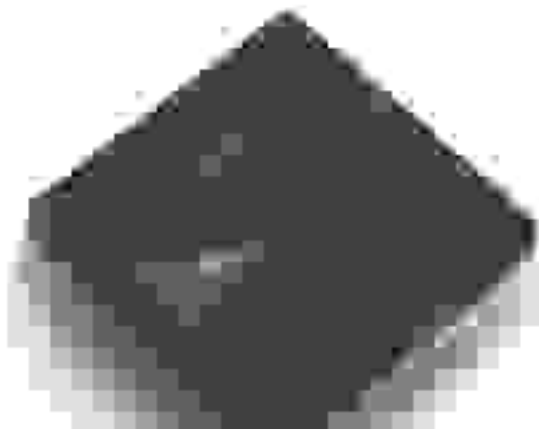
### **Comprehensive and clear specification manual**

## **15. Resulting product, its industrialisation and internal replication**

With the component resulting from the FUSE project, the Hauser division will be able to implement a number of product improvements. The main advances resulting from the integration of the component into COMPAX are reduced manufacturing costs and an expansion of the options available for the device. In addition to the expansion of an existing product, two further actions are planned:

- Two-axis drive controller for special applications. This will be developed jointly with an existing customer. The aim is to develop a customised system for the customer's machine. The two-axis approach, which was consistently taken into account in the PAP project, results, in this case, in a further size and cost reduction because only one processor is required for administration and real-time control of the two ASICs and therefore the two control systems.

- A further customer project deals with robot technology: a three-axis drive controller is to be developed for a welding robot. The reduced unit size and manufacturing cost also come into play here. Material costs are further reduced by the use of a single processor system for all three axes.



These two customer projects could not have been implemented at the desired commercial and geometrical conditions without the PAP Figure 1: PAP Mixed Signal Chip, Plastic Packaging

approach. The range of target applications can therefore clearly be extended with PAP.

For chip production, a continued co-operation with the semiconductor manufacturer – who has to date acted as subcontractor – is planned. The reasons are the partner's focus on medium-sized customers and the fact that the personal contacts and know-how established in the course of the project are expected to facilitate a quick commencement of series production.

Serial production of the ASIC is scheduled for the 2<sup>nd</sup> Quarter 1999. At this point in time, in addition to integration into existing single-axis controls the ASIC will also be integrated into a double-axes control. Prototypes of this double-axes unit will be available by the 3<sup>rd</sup> Quarter 1999. The costs for this industrialisation, including marketing and setup of service for our customers may well reach 100 – 200 k€.

## **16. Economic impact and improvement in competitive position**

The most important improvements that can be achieved with a mixed signal ASIC in COMPAX are cost reduction, space area savings and increased reliability. Beside these commercial benefits, the increased flexibility of the peripheral functions should also be noted. Here, past years' practical experience has been implemented so as to be able to solve future problems systematically and effectively.

As a result of the development, Hauser now possesses a modular system of hardware components. The PAP system provides all functions required at the interface to the power circuit (pulse width modulator, phase current measurement, measurement of intermediate circuit voltage), to the motor (speed, position, temperature measurement) and to other drive controllers (synchronisation, master-slave coupling, etc.). Through integration of the required functionality in a mixed signal ASIC, a significant cost saving can be realised.

This cost saving results from two factors:

- integration of discrete functionality in a highly integrated component and the associated reduction of required components;
- the elimination of redundancies in a multiple axis system.

The elimination of redundancies in a multiple axis system has a significant influence on costs. With the PAP system approach, redundancies are eliminated because all intelligent signal-processing functions are concentrated centrally on a single powerful DSP, while all passive, axis-related functions are implemented in the form of ASICs. As long as the central DSP's processor throughput is sufficient, any number of axes can be added by adding further PAP modules to the system.

The PAP approach also results in a reduction in material costs associated with the microelectronics, which are responsible for a large percentage of the cost of a high performance servo controller. Compared to the conventional Hauser solution, the material cost savings for microelectronics for a three-axis controller is ca. 50%. This saving makes a drastic system price reduction possible in cost-sensitive multi-axis applications.

Especially in the multi-axis applications area, the PAP approach will improve competitiveness by reducing material and manufacturing costs.

A cost estimate results in the following comparative figures for the proportion of microelectronics in a digital drive controller:

	Single axis system cost	Three-axis system cost
Existing technology	100%	100%
PAP approach	85%	50%

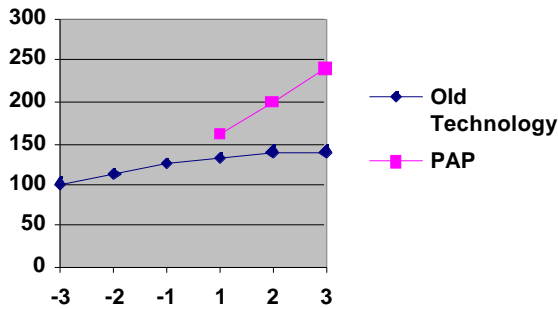
The greatest cost benefit is achieved in three-axis systems because – in contrast to existing technology – redundancy is eliminated with the modular PAP concept. It is evident, however, that a cost advantage can be achieved even with simple single-axis applications.

While the substitution of COMPAX and analogue controllers can be implemented immediately and the increased annual production quantities therefore already achieved in the short-term, the additional axes, which can be achieved by expansion of the market share, is expected to take about three years.

Total project costs of 250 k€ considerably exceed the costs of the FUSE approach. On the one hand the development costs increased due to the required re-designs. Further additional costs were incurred during implementation of the serial production by the semiconductor manufacturer, such as i.e. the generation of a test program for the individual test of serial chips. In addition to the actual FUSE project costs, investments for items such as production implementation- and initialisation and for market introduction of the new product must be taken into consideration. However, with mean cost saving of 15% per single-axis unit and an estimated saving of 50% for a three-axis controller comparing with the total costs of the project - consisting of development, initialisation and readjustment costs in production, marketing and sales – the break-even point should be reached after 1 to 1.5 years and a return on investment should be 250% for a minimum lifetime of 5 years.

The following table shows the impact of the new PAP development on the expected turnover generated by products based on this architecture. The availability of PAP products will allow to nearly double the turnover compared with the situation of having products based on the current non-PAP-technology. The major effect comes from the introduction of new multi-axes drives.

Year	Turnover <b>without PAP</b> [%]	Turnover <b>with PAP</b> [%]	Ratio
-3	100 %	100 %	1
-2	112 %	112 %	1
-1	125 %	125 %	1
1	127 %	133 %	1,05
2	127 %	200 %	1,57
3	127%	240 %	1,89



Comparison of sales figures (relative)

For the purpose of evaluating market share, the market growth is estimated at 10%. In defence of the relative market share, a sizeable increase in turnover is estimated. In view of the expected intensification of competition, this is an ambitious but – because of the newly acquired technological advantage – by no means unrealistic goal.

With the PAP ASIC, Hauser has a modular system that can be used not only to improve the COMPAX product family: customer-specific projects, too, can be developed with the PAP architecture. The PAP approach will therefore prove beneficial in the conversion of the analogue HBV products and the OEM range. For the customer this will result in a reduced number of boards in the system with improved size, reliability and costs and a wider range of products that are especially suited for specific applications and the option for cost effective customer-specific solutions. Products may be optimized for specific applications or with respect to the price if technical specifications allow so. With the new PAP technology prices per axis may be lowered from 250€ to about 150€ or performance can be increased.

## 17. Target audience for dissemination throughout Europe

The use of mixed signal technology is a powerful instrument for reducing item costs and component size while at the same time improving product quality and reliability. In principle, this technology can lead to advanced solutions in a broad field of target applications that use a microprocessor system and/or interface on one hand and feature a certain amount of analogue functionality on the other. Typical products, beside the digital drive controller introduced in the project, are general control devices (temperature controllers, Process controllers, etc.), sensors with a digital interface and integrated intelligence (moisture, temperature, pressure, flow sensors), distributed actuators with simple to intermediate functionality (digital interface, analogue input/output with signal preprocessing) and numerous other products for a broad field of applications. However, one should be aware, that MS-ASIC technology bears certain risks, especially in the analogue part. Therefore, great care should be taken with respect to planning of costs and time, selection of partners and contractual issues.

This project shows a good approach for selection of functionality of the overall system for implementation as mixed signal ASIC. All components that where

expected to be replaced by more powerful devices in the future where considered separately. During specification the objective to cover a wider range of different products with the same ASIC was evaluated carefully against cost for unused functions for some of the applications.

This document may provide information to any company in the domain of industrial automation with products that interfaces to drives and sensors. In general this is the PRODCOM code 3110 class 'Electric Equipment'. Hausers experience shows that mixed signal ASICs are a suitable technology for certain applications and that a project can be handled with limited risk.