Fuse Demonstrator Document AE  25888

FPGA for EDAC (Error Detection and Correction)

Abstract

CINDATEC develops, manufactures and distributes state-of-the-art applications using computer hard- and software for industry sectors like aircraft/spacecraft, medical equipment, engineering services etc. The company was founded in 1991 and in 1998 had 8 employees, 6 of them involved in hardware and software design.

One of CINDATEC’s main products is a transputer-based fault-tolerant computer used for applications with high data security requirements. The technical basis of this fault-tolerant system consists of a redundant hardware and an implemented specific system software. Because of market requirements the existing product had to be improved. Characteristic features of the new system are a better fault tolerance and data security reached by the introduction of the new Error Detection And Correction unit (EDAC), the flexibility for different interfaces and a more cost effective solution.

The main objective of the project is an increase of turnover in this product area, but also additional market shares by selling the FPGA based EDAC component itself. In order to achieve this, CINDATEC introduced FPGA technology and VHDL into the company’s business. The staff involved in the AE were trained in system-oriented design and simulation, its synthesis and the implementation of the designed system into Field Programmable Gate Arrays (FPGA). The use of this technology is optimal for the project and offers high flexibility, short development and market introduction periods and the advantages of a customer-specific ASIC solution also for a small number of pieces.

After first training activities, a very practical-oriented “Learning-by-doing” methodology was chosen. For the development process, the V-system supporting VHDL was used. The simulated design was implemented in a XILINX FPGA XC4013. The introduction of these technologies allowed the combination of fault-tolerant systems with error detecting and correcting components.

CINDATECs specialists acquired knowledge in the management of development projects using microelectronics technologies, in the field of digital VHDL based system design and its implementation in FPGAs. They are now able to replicate this in future developments.

The manufacturing costs have been reduced by 60%, which is a main driver to improving the competitive situation of CINDATEC’s EDAC. Furthermore, the component itself can be sold now separately, thus opening up a new market.

The project had a duration of 11 months, a break of two months included as opposed to the 9 months planned. The cost of the AE was 56 kECU, as planned. In addition a further 150 to 200K ECU was spent on productionising the EDAC, and will take around 1 year. The payback period is expected to be in the range of 12-18 months, and the ROI between 200 and 300% assuming a 3 year product life cycle.

A number of lessons were learnt during the AE. These included ensuring that the market for the product is monitored during the development phase. In this AE the FPGA solution will be modified to make it compatible with the PC.
1. Company name and address

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2. Company size

CINDATEC (the First User, FU) was founded in 1991 and had at the beginning of the AE 8 employees, 7 of them full-time, 1 external consultant and 1 temporary member (students, trainees). Seven of them are engineers of which six engineers are involved in software and hardware development projects for different applications. Two employees work in the manufacturing and test department.

The company has experience in digital design using standard components.

Five employees were involved in the AE: the Manager of the company, one Scientist, and three Designers. They have expertise in the management of software projects as well as hardware design based on discrete digital components. In all tasks, the AE was executed with close teamwork.

3. Company business description

CINDATEC’s business fields are development, manufacture and application of computer systems for advanced application areas, for instance for applications in space technology with high safety and security requirements. The existing fault-tolerant computing system which was the subject of the AE was initially used in this area.

Furthermore, CINDATEC works in such fields like home communication systems (European Installation Bus – EIB), devices/computer networks (Tools for network controlling and handling), and medical applications (electroretinogramm – ERG).

CINDATEC’s products normally have to be adapted to the customers’ needs, i.e. the system specification of the products must be modified. Therefore, manufacturing, installation and maintenance are user specific in many cases.

Marketing and sales activities are carried out by CINDATEC for the full product range. Additionally, a part of these activities is outsourced.

4. Company markets and competitive position at the start of the AE

As described, CINDATEC develops, manufactures and distributes state-of-the-art applications using computer hard- and software for industry sectors like aircraft/spacecraft, medical equipment, engineering services etc.

CINDATEC has special expertise in hardware and software development of fault-tolerant computers and their application in different areas. It is one of the main business fields of the company. In the regional market the market share of the existing product is less than 10%.
Several projects have been realised in other regions of Germany and in Europe. This was possible, because CINDATEC is able to react very flexibly and fast to the needs of a customer – an advantage of being an SME.
Actually, the number of possible applications for fault-tolerant computer systems increases very rapidly. Starting from applications in space technology and aviation or computer applications in medicine and industry, up to communication technologies and data transfer processes, error detection and correction methods often must be implemented.
Market investigations have shown that between about 15 and 30% of all computer applications work with fault tolerant solutions in some form. Because of the increase of data to be processed and the increasing influence of computer-based methods in nearly all areas (high safety sectors included) this figure will more than double in the next 3 to 5 years. Precise estimates of the overall market size cannot be given, but there are hundreds of thousands relevant computer applications worldwide. The share for Europe is in the range of one third of them.

Competitors in the area of fault tolerant solutions are large computer companies from all over the world. Also some smaller companies have their market niche in the development of customer specific solutions. The activities of the small company are normally related to software development, using standard hard- and software components.

The position of CINDATEC is characterised by the application of special error detection and correction procedures. The company sells their products for high security applications (airspace, medicine).

Using the result of the AE, CINDATEC can enlarge the number of potential customers in high security applications and can also open a completely new market segment by selling the error detection and correction component itself, for all applications where an error check of data (e.g. in data transfer processes) should be done. The customers can implement the EDAC into their products. Thus, the number of potential applicants and as a consequence the market is much higher. The goal is to improve the market position according to this new potential.

The current market situation of "fault tolerant computers" is characterised by

- Double Computer systems.
- Computers with auxiliary power systems.
- Systems with reflected memory.

using different technologies starting from solutions on the basis of discrete components up to high-integrated products.

These solutions are "fail-save", i.e.

- the actual data just before the appearance of the failure are saved
- after the appearance of the failure the system goes to a defined state, but:
- the data during the failure state are lost,
- the system must be started again, and there is no data processing until the start.

Classic Fault-tolerant Computers have no data loss in case of a simple failure, and continue the work without an interrupt.

The better solution uses Byzantine Fault Tolerance and gives the safety for correct working even if a "malicious" failure should occur, that means it is a failure state, where one computer works with a falsified algorithm. Such solutions have not been offered before.

CINDATEC develops Fault-tolerant Computers using parallel computer systems with a non-hierarchic operating system and the possibility of Byzantine Fault Tolerance. This requires a special system configuration. Using the new EDAC-IC, the system will have better properties in performance, reliability and price.

Without the innovative CINDATEC would lose an important part of its turnover in the field of fault-tolerant computer systems. We assume a decrease as follows (basis: 1998=100%):

1999: 50%  
2000: 25%  
2001: 10%

The reasons for these extreme expected losses are:

a) changed component basis (trend from transmitter to PC)
b) dramatic drop in prices with each new processor generation

c) usual continuous functional enhancement of products

Additionally, the modified product will result in higher sales figures because of a higher reliability and increased functionality of the components and the product itself as well as a better price – performance – ratio.

5. Product to be improved and its industrial sectors

The component will be used in CINDATEC’s fault-tolerant computer system that is typically used in application sectors with high safety and security requirements, e.g. companies and organisations/institutions with failure-sensitive areas. Typical applications are in aircraft and spacecraft, the chemical industry or those fields, where a computer failure might cause a danger for persons.

The existing competitive solutions on the market are “fail-safe”. CINDATEC’s target solution within the AE will be fault-tolerant for more than one error (e.g. additionally occurring after a first memory failure).

This fault-tolerant computer system consists of several modules which operate independent. Each of these modules is a complete computer (lowest replaceable unit - LRU) with CPU, memory and some modules with connections for data exchange, input and output.

The principle of the fault tolerant computer system is shown below:

The existing product realises the principles of Byzantine Fault Tolerance, i.e. the generation of coincident input data and the check of the results are performed via a data exchange between the different computer modules of the system. This principle guarantees a correct work under all possible fault conditions. The fault-tolerant functions are generated up to now with suitable software in each module. The existing solution checks input data, the operation results as well as simple memory errors. If such a single error occurs, the whole hierarchical system is not anymore able to eliminate any other failure at the same time. The partial substitution of this software system by a hardware solution with improved and enlarged functionality is the objective of the AE.

Block diagram of the existing module

![Block diagram of the existing module](image-url)
Main parameters of the existing module:

- Processor: T800
- Speed: 30 MHz
- Processing capacity: 20 MIPS
- Memory: 4 MB DRAM
- Error detection/correction of Memory: Not
- Serial Communication: 4 Links at 20 Mbit/s
- Error detection of Links: CRC-Checking by Software
- Error correction of Links: Not
- Power consumption: approx. 15 W

The total solution comprises 34 IC's, and has a total manufacturing cost of around 150 ECU.

6. **Description of the technical product improvements**

The main functional objective of the AE is the increase and improvement of the fault-tolerant properties of the whole computer system combined with a more cost-effective solution. At the same time, a modification of the interface conditions for different applications must be easily possible.

The functional objective of the AE at component level is the partial substitution of the existing software based error detection and correction algorithms by FPGA hardware. The main advantage of this solution is that an occurring error can be corrected in parallel to the running data exchange processes because the system is still able to detect and correct a second error.

The subject of the AE is a part of the error detection and correction unit of CINDATEC’s fault-tolerant computer system. Especially, the EDAC generates in case of a memory write command an additional check word. When the memory is read, the check word is generated again and compared with the first one. If there is a difference, an error correction will be done. Additionally, an error signal is generated.

The development is based on the application of a XILINX XC4013 FPGA within the EDAC component. It consists of the following functional blocks:
• Processor interface
• Memory interface
• Link Interface
• Error detection and correction unit for DRAM
• state machine for memory access control
• error detection unit for serial communications
• write registers for configuration,
• read registers for state tests

The next block diagram shows the structure of the improved system:
The main parameters of the improved module are as follows:

Processor: ST20450
Speed: 40 MHz
Processing capacity: 32 MIPS
Memory: 8 MB DRAM - Work Memory
4 MB DRAM - Check Memory
Error detection/correction of Memory: Correction of 1-bit Memory Errors
Detection up to 2-bit Memory Errors
Serial Communication: 4 Links at 20 Mbit/s
Error detection of Links: CRC-Checking by Hardware
Power consumption: approx. 7.5 W

The photograph gives an impression of the overall result of the AE.

The main advantages of the improved product are lower cost plus the additional functionality described above. It uses 1 FPGA and costs around 50 ECU.

7. Choices and rationale for the selected technologies, tools and methodologies

For the realisation of the EDAC systems different options were available:
• discrete PCB solution with µC
• ASIC
• FPGA

Timing conditions, complexity and production costs prevented the use of a discrete conventional board realisation.
Furthermore, the EDAC has to be designed for a flexible range of applications. In this case, the basic concept of the EDAC system must be adapted. This excludes in a first approach the possibility of an ASIC realisation.

The chosen FPGA solution is the most effective because it combines the necessary flexibility with the required performance, also for small number of pieces for one special type of the fault-tolerant computer system.

It is planned to sell the EDAC component itself, because - due to its flexibility - it can be used for other applications outside our fault-tolerant computer, too. In order to guarantee a later migration to an ASIC (if for one special modification a high number of pieces should be required), a top-down design methodology using VHDL at system level was selected. For this system design only language elements suitable for automatic synthesis were used. Based on a complex hierarchical simulation with VSYSTEM the gate level description of the system was automatically generated.

After a new simulation and the implementation of additional subblocks, the logic structure was implemented into the selected FPGA. The used Foundation System guarantees a continuous design flow.

The simulated and verified VHDL design can be converted to solutions using different hardware technologies, using the library elements of the different manufacturers. This reduces the design risk for an ASIC implementation dramatically.

For an SME the cost factor of used design tools is very important. Workstation and PC-based program systems are available on the market. For the AE, PC based design tools were selected regarding a later in-house application.

We have chosen for the fabrication of the EDAC a XILINX FPGA type XC4013, because it optimally matches the technical requirements, especially regarding

- Time parameters and frequencies
  The FPGA has to communicate with a 40 MHz processor
- Gate counts
  The design has a complexity of about 7000 gate equivalents, including about 400 Flip-Flops

The EDAC board with the FPGA was designed in mixed technology using conventional and SMD components. The reason for choosing this technology was the required small PCB size and optimal production costs.

As already described, the FPGA solution will be sold also as an OEM component to other users to be implemented in their own customer systems. In order to prevent design theft, the design will be retargeted to an antifuse FPGA (e.g. ACTEL type) in this case. This is another reason to design the system with VHDL using its portability capabilities. The design on system level can be easily transferred either to an ASIC or to another FPGA type without additional design risk.

In several iteration steps of design and simulation the timing of the logic of the EDAC was optimised to work properly with the 40 MHz Processor (Transputer). The design was tested in all phases of the AE. In the design task, the whole VHDL system description as well as the subblocks were simulated. To carry out this simulation, a test-bench for the EDAC was designed in VHDL. After conversion to gate level the functional behaviour was simulated again using test sequences that guaranteed a high fault coverage rate. After implementation into the FPGA structure a simulation with real time conditions (regarding best and worst case conditions, too) completed the simulation process.

Finally, the transputer board with EDAC was tested in a PC environment.

8. Expertise and experience of the company
Already prior to the AE the company had expertise in hardware and software of fault-tolerant computers and their application in different areas.

CINDATEC has know-how in software solutions. Programming knowledge under the operating systems DOS, Win95/98, WinNT or UNIX is available. The engineers of the company use Delphi, C++, Pascal, OCCAM, Assembler and other languages for the development of application-specific software. The hardware base including workstations, transputer-based multi-clusters, and more recently PCs with now have high performance levels.

For the customer-oriented realisation of such systems, CINDATEC is experienced in PCB design and manufacture in through-hole or SMD technology, together with the use of CAD systems used for this purpose. ORCAD is available at the First User’s site.

The company had no experience in the management of FPGA projects, system design using VHDL and FPGA or ASIC design methodologies. In detail, the following knowledge was lacking:

In the management sector:

- Overview about available microelectronics technologies and corresponding selection criteria
- Planning of FPGA based developments, cost estimations
- Choice of best FPGA types for a defined project
- Selection of tools to be used
- Interfaces to subcontractors

In the technical sector:

- Specification
- System design and simulation methodology with VHDL
- Top-down design approach
- Usage of design and simulation tools (V system, XACT Foundation)
- Generation of test sequences
- Product-oriented test methodologies

9. Workplan and rationale

The work plan was structured to ensure that CINDATEC were able to carry out a significant amount of the design work, with assistance from the sub contractor. In order to achieve this formal training courses were planned early in the project, and more on-the-job training offered by the sub contractor during the design phase.

The following table describes the efforts planned in the submission with those really spent in the project.
<table>
<thead>
<tr>
<th>Task</th>
<th>Planned</th>
<th>Actual</th>
<th>Subcontractor Effort (Spent as planned)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. Technical Management</strong></td>
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<tr>
<td>Project management, reporting necessary during the whole project</td>
<td>30</td>
<td>31.25</td>
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<tr>
<td><strong>2. Training</strong></td>
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<tr>
<td>Technical management</td>
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<tr>
<td>Design and simulation</td>
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<td>FPGA design/Basic knowledge</td>
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<td>VHDL</td>
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<tr>
<td><strong>3. Specification</strong></td>
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<tr>
<td>Adaptation of the system to the technology requirements</td>
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<td>39.50</td>
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<tr>
<td>Selection of FPGA types</td>
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<td>Specification of the complete system and corresponding subsystems including their interfaces</td>
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<td><strong>4. Design</strong></td>
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<td>VHDL description of the system</td>
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<td>Generation of test sequences</td>
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<tr>
<td>Simulation and modification</td>
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<tr>
<td>Programming of the FPGA</td>
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<tr>
<td>System test of the FPGA and modification</td>
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<tr>
<td>Design and manufacturing of the testboard</td>
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<td><strong>5. Evaluation</strong></td>
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<tr>
<td>Integration of the prototype into the PC</td>
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<td>85.75</td>
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<td>System test under practical conditions</td>
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<td>Consequences for iteration</td>
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<td><strong>Total</strong></td>
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* Assistance by TTN
### Workplan for AE as planned

<table>
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<tr>
<th>Time in months</th>
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<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
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<td>Design</td>
<td>CINDATEC/GEMAC</td>
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<td>Kick-off</td>
<td>Specification</td>
<td>know how transfer ended</td>
<td>Prototype</td>
<td>Computer module</td>
<td>End of Experiment Ready Product</td>
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</table>

### Workplan for AE as executed

<table>
<thead>
<tr>
<th>Time in months</th>
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<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
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<th>8</th>
<th>9</th>
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</thead>
<tbody>
<tr>
<td>Technical Management</td>
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<tr>
<td>Training</td>
<td>GEMAC/CINDATEC</td>
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<tr>
<td>Specification</td>
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<tr>
<td>Design</td>
<td>CINDATEC/GEMAC</td>
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<tr>
<td>Evaluation</td>
<td>CINDATEC</td>
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<td>Kick-off</td>
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<td>Specification2</td>
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<td>Prototype</td>
<td>End of Experiment Ready Product</td>
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</table>

Some explanations:

It was necessary to ask for an extension/break of the project for 2 months due to illness of one of our main specialists involved in the AE.

In the specification task it was necessary to make some changes regarding the first approach. The first design based on the optional application of different transputer types resulted in a pin number for the EDAC exceeding those of the available FPGA types. That’s why it was necessary to restrict possible types of transputers and to re-specify the whole system again (“Specification 2”).

The effort spent in the design phase was less than planned, because the learning-by doing methodology was very effective for us, and we could process the design phase much more effectively than expected. The result was that we saved the time which was foreseen in the contingency plan for additional design cycles or iterations, respectively.

One reason for that is also the good support by the TTN/subcontractor.

In the following table, the division of work between First User and subcontractor is described:
<table>
<thead>
<tr>
<th>Task</th>
<th>First User</th>
<th>Subcontractor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Management</td>
<td>Project related management</td>
<td>Online assistance as necessary</td>
</tr>
<tr>
<td>Training</td>
<td>Participation in training</td>
<td>Management Training (Project planning, VHDL and FPGA design methodologies, test strategies, tools)</td>
</tr>
<tr>
<td>Specification</td>
<td>Function and technology related tasks</td>
<td>Assistance in technology related tasks</td>
</tr>
<tr>
<td></td>
<td>Specification Review</td>
<td></td>
</tr>
<tr>
<td>Design</td>
<td>Top level design in VHDL</td>
<td>Design Assistance starting with permanent help at the beginning and ending with &quot;assistance on request&quot;</td>
</tr>
<tr>
<td></td>
<td>Generation of test sequences</td>
<td></td>
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<tr>
<td></td>
<td>Simulation</td>
<td></td>
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<tr>
<td></td>
<td>Automatic synthesis of gate structure</td>
<td></td>
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<tr>
<td></td>
<td>Implementation into FPGA, simulation with real time conditions</td>
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<tr>
<td></td>
<td>Design review</td>
<td></td>
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<td></td>
<td>Board design</td>
<td></td>
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<tr>
<td>Evaluation &amp; Test</td>
<td>FPGA Test (PCB based)</td>
<td>Assistance</td>
</tr>
<tr>
<td></td>
<td>Field test (product oriented)</td>
<td></td>
</tr>
</tbody>
</table>

**Table 2: Division of work**

In summary, the project overran by 2 months to 11 months.
10. Subcontractor information

The CINDATEC GmbH is a system and product oriented company. We had experience in hardware and software development of fault-tolerant computers and their application in different areas. In the field of microelectronics, the company was experienced in PCB design and manufacturing in through-hole or SMD technology as well as the use of CAD systems. There were no experiences in VHDL based system design methodologies or FPGA applications available, neither from the technical nor from the management point of view.

Our intention in the AE was to learn just this in order to be able to manage and to execute such a project in the future ourselves.

That’s why we were looking for a subcontractor with the following technical competencies:

- experiences in training activities for FPGA design and technical management
- know-how in “Learning-by-doing-methodologies” for this kind of work
- proven experience in cooperation with partners like us
- know-how and references in VHDL based top-down design and simulation strategies
- application-oriented VHDL and FPGA know-how (how to implement and to test a FPGA in the final product)

In addition we wanted a sub contractor located near to us.

Starting from this selection criteria, GEMAC was chosen as subcontractor. The company is a SME with 55 employees, and has specialists who are experienced in all kinds of application-oriented design work built up over 15 years. This includes customer-specific electronics on PCBs, hybrid circuits, MCMs, FPGAs, digital, analogue or mixed signal ASICs and microsystems.

The company fulfils all criteria mentioned above and has all necessary design tools available.

GEMAC’s experience in the application-oriented design activities with customers similar to us was advantageous. The training activities and the subsequent design assistance used on the longtime-knowledge of the specialists, and were very efficient. Two specialists for digital design and one management expert were involved in the AE.

The subcontractor was also very flexible in his work. Depending on the actual requirements, problems and project situation, a very dynamic style of cooperation was possible that helped us to keep to the project in timescales.

The responsibilities and the division of work changed over the project time. In the first training activities, we had to learn and GEMAC was responsible for the know-how transfer.

Starting with the “Learning-by-Doing steps, the situation changed. The work was now characterised by a kind of “decreasing assistance” (which was given, whenever needed).

The locality also enabled us to react very fast to difficulties coming up in all processes. For instance, the training was split in several parts according to the project schedule. It was possible to get technical assistance whenever a problem occurred very fast and not only as planned in the workplan and defined in the contract.

As a result of the AE the subcontractor is already familiar with the technical problems of our company. This allows an effective information flow and optimal project work. GEMAC will be able to give direct assistance in any future projects, on design, prototyping and serial manufacture as requested.

The detailed division of work and the effort was already described in the last section. As can be seen in the ratio between the efforts spent, it was a real cooperation between the two partners.
The contract defined all steps of the project; especially training activities and the design assistance to be delivered by GEMAC as defined in the workplan described above. Additionally, the licence issues for the FPGA tools were contained in the contract. CINDATEC is the owner of the developed solution.

11. Barriers perceived by the company in the first use of the AE technology

CINDATEC is a company which was founded in 1991 and can be regarded as a typical representative of SME’s in East Germany. CINDATEC has

- its origins in the R&D landscape of the former GDR
- knowledge in the area of computer sciences and technologies
- knowledge in the design of digital, analogue or mixed systems at the level of discrete logic, analogue components and standard PCBs
- special knowledge in the field of software

In the last years the firm got know-how in selected fields of computer applications like the fault-tolerant computers. The products that were developed based on the technologies available at the company up to that point. But we recognised that the application of new technologies like FPGA would be useful for the innovation of the company’s products. Some new product features, e.g. the necessary flexibility to adapt the system to the special requirements of a customer, would have been not possible without the implementation of this technology.

But there was an important barrier: The first use of new technologies without own experience is very risky, time consuming and expensive. Even if were possible to go through such a learning process starting from a training course, via first design steps using trial and error through to a test of the developed solution, the effort, the risk and the costs are much higher than to use a subcontractor assistance for the first project (like the FUSE AE). This includes support in management, training, design and evaluation.

Based on the experiences in the company, CINDATEC was already familiar with the management of design projects using microelectronics technologies. However, there was a lack of information concerning the issues of a FPGA application (e.g. time schedules, price estimations, selection of tools and components).

Software tools and hardware are necessary to make a development like FPGA for EDAC. The possibility to make the wrong investment is very high without advise. Within FUSE it is possible to test the necessary hard and software for such a project without a financial risk. With the experience and knowledge coming from the AE qualified decisions can be made for future replications or iterations if necessary.

In summary we can say that the general understanding for microelectronics technologies was not the problem for us. It was the uncertainty as to how the application of FPGA technology could help to innovate our products with low risk, limited effort and within a reasonable time.

Also with no experience in the financial planning of FPGA projects, we had a management barrier and – regarding the high costs and risks if you will do it at your own – a strong financial barrier as well.
12. Steps taken to overcome the barriers and arrive at an improved product

The AE project proposed was structured in order that the barriers would be overcome. The first barrier regarding how to plan such a project was already overcome in the preparation of the project proposal. In several meetings with the TTN the possible workplan, tools, estimated project costs and subcontractor interfaces were discussed in detail. A more project-related know-how was transferred in the management-training course after the start of the AE. The next phase was to seek the best partnership to help us learn the FPGA technology.

All necessary equipment and know-how for our AE were available from the chosen sub contractor. With our subcontractor we found excellent experts for training and design activities of VHDL-based digital customer-specific developments. We got very good support in the specification task to adapt our wishes and requirements to the capabilities of the technology. Of course the main effort was spent by the subcontractor for design activities (necessary iteration steps included). The best way to overcome the barriers was the application-oriented “Learning-by-Doing” design methodology we used.

It was not a problem to carry out the technical management in the AE because all partners were experienced in handling technical projects. However, any missing know-how for FPGA projects was transferred within the training course for Technical Management.

The phased workplan with description, milestones, deliverables was the way for overcoming some technical know-how barriers. The tool selection problem could be solved within the AE. We are now familiar with the technical features of the design tool and its capabilities. Based on this knowledge, we will not make the wrong decision when buying our own design tools.

The design risk, the necessary manpower and the long development times without external assistance were overcome within the AE using the continuous support of the subcontractor.

13. Knowledge and experience acquired

CINDATEC is now able to plan and execute FPGA projects. This is the most important experience resulting from the AE and this knowledge will be used for new projects. This next design can be done more effectively and without errors which resulted from the learning curve of us as a beginner.

The methodology to achieve these goals together with the subcontractor has already been described. Based on the initial training courses, followed by own design and management activities, we learnt:

- **Planning of FPGA projects**
  This includes feasibility studies and market investigations in our industry sector, a cost-benefit analysis, and the selection of possible FPGA types and tools.

- **Management of FPGA projects**
  The company is now able to define workplans, interfaces to manufacturers and component distributors, can react to necessary project modifications, can organise the daily management, and has setup an internal documentation guideline for FPGA projects.

- **System specification of FPGA projects**
  CINDATEC knows now the technical features and capabilities of FPGA technology and can adapt the functional requirements of the products to the technology capabilities within the specification task.

- **System design using VHDL**
  The experience acquired contains VHDL design methods, simulation strategies, and the use of language elements to be used for automatic synthesis.

- **Test strategies for VHDL-based designs**
  That means the definition of test-benches, test methodologies, and test sequences with a high fault-coverage rate.

- **Implementation and test of FPGAs in the final product**
14. Lessons learnt

Observe the market continuously.
The development of a planned technical solution takes time. On the other side, the markets are changing very rapidly. Even if a project has been started, the market should be investigated continuously in order to be able to react to changing conditions (e.g. regarding available components, the new capabilities of upcoming new computer technologies).

The right selection of a subcontractor for a first VHDL/FPGA project, but also for the application of other technologies is very important for a successful development. In most of the cases, it will not be possible to finalise such a project without external assistance successfully. Internal knowledge, necessary investments, available staff at the company etc. are barriers that can be overcome in a first application only with an experienced subcontractor.

Description and simulation of an FPGA at system level is one thing and place and route the design in silicon the other. During the synthesis we recognised that the high timing requirements, high clock rates (40 MHz) and the implementation of complex bus structures have consequences for the design.

Depending on the logic to be implemented, the available logic blocks can be routed theoretically nearly to 100% (simple system structures). In case of more complex internal bus structures, the share of usable CLBs is lower, e.g. in the range of about 70% in our case.

Because of the bus structure, a second design iteration was necessary in order to be able to fit the design to the selected FPGA type.

Design tools should be tested in a first project before making a buying decision. Don’t trust to promises of tool distributors, test yourself.

In our mind, the V System is applicable for VHDL based designs. It offers a good functionality and has a reasonable price (full version: about 7.000 ECU). It is easy to use; a handbook which describes the system in a clear way is available. The tool delivers reliable results which reflect the reality.

The introduction of VHDL is easier, if the specialists are already familiar with software methodologies. The VHDL language with its functional and structural approach is based generally on these principles.

Basis for own design activities were the training courses delivered by the subcontractor and the tool handbooks as well. For a first introduction of VHDL based design methodologies, the following material can be recommended:

Lehmann/Wunder/Selz: Schaltungsdesign mit VHDL
Franzis-Verlag
Peter Ashenden: The VHDL Cookbook
University of Adelaide/Australia

FPGAs offer a high flexibility for the design in general. This concerns:
Ability to change the implemented system structure as a result of test activities
Customer specific system modification
Modification of internal system structure (e.g. change from transputer based solution to a PC oriented application)

CINDATEC has now the necessary in-house skills to use these inherent capabilities of FPGAs.
For the implementation of the component into the product you often need additional software and hardware tools (e.g. adapters, generators, laboratory equipment, special programs, interfaces). Don’t forget this in your cost and time planning.
For the evaluation task enough time and possibly also a redesign of the PCB should be planned. Murphy is everywhere and causes changes in the system in any case. If possible, this process should be combined with the implementation of additional features and technical innovations. In the result of the project execution, new ideas concerning the system and new market requirements may exist. In our case, the redesign for serial production will be done with a new processor.

The industrialisation of the product is not an easy task. We will have to do a PCB redesign when going from the prototype to the serial production in order to guarantee the best solution for an optimal price-performance ratio and to reach all aimed parameters for the version to be manufactured. This requires additional investments. Don’t forget the costs for the market introduction of the product (advertisement, fair presentations, ...). 

The enormous efficiency of the present PC’s and there low prices force us to revise our Transputer-based fault-tolerant computer system. The next generation of the product will be based on industrial PC-components. This requires inevitably the redesign of the used FPGA.

The ready prototype is only the first step. For industrialisation and marketing we have to plan additional investments.

15. Resulting product, its industrialisation and internal replication

The result of the AE consists of the following parts:

- verified VHDL description of EDAC
- programming data for XILINX XC4013 FPGA
- PCB with processor, memory and EDAC IC.

The EDAC as the “intelligent connector” of processor and memory performs the error detection and correction. This offers the possibility for more fault-tolerant functions in our final product. In detail, we are now able to detect and to correct one additional memory error.

One main step in the industrialisation process will be the evaluation of the existing processor solution in order to define the final configuration of the system. This might cause a modification in the contents of the XILINX FPGA to adapt the functionality to the technical features of the processor. This is—if applicable- at the same time a kind of internal replication of the acquired know-how.

According to the market’s requirements, the industrialisation process will contain a redesign for a PC based solution. We will have to modify our general Fault-Tolerant-Computer solution implementing the new designed EDAC system before the product can be introduced to the market. It is now planned for end of 1999. The estimated costs for industrialisation will be in the range of 150 to 200 K ECU. This includes personnel costs (30...50%), prototyping costs (10%), services (10...20%), direct preparation of manufacturing (15...20%), and marketing and sales (20...30%).

Furthermore, we are planning to use our FTC system for other sophisticated applications of our daily live where computer mistakes consequently lead to terrible consequences. This and the application of the know-how resulting from the AE in other projects will cause additional market shares, safe employment and improve our competitive position. So we have to realise with the highest priority planned applications in PC based medical equipment and in space tasks. Here the first of our partners have already asked for EDAC-based solutions. This business would not have been possible without the results of the AE.

The concept of EDAC itself will be evaluated regarding other possible applications. Because of the universal character, the component itself will be offered to other companies to be used in their equipment.

The new EDAC system (FPGA and complete board) will be marketed in different ways:

- Distribution of complete systems as a standard PC based solution (interface component between PC and memory)
- Distribution of the FPGA for the use in specific solutions of our customers

Besides our own sales activities, the product will be marketed via external distributors.

We are also thinking about an ASIC - development for a new product. However this will be done only in combination with the introduction of another processor solution (PC). For this purpose, the connections to our subcontractor will be used.

16. Economic impact and improvement in competitive position

The check of memory faults during the FTC’s system work time is an absolute high qualitative improvement for a FTC system.

The modified product will allow a better sale because of

- higher reliability of the product
- higher reliability of components
- better price - to - performance - relation.

This shows the comparison of the direct material costs between the old and the AE solution:

The FPGA substitutes 34 medium integrated standard ICs. The material costs for the applied IC’s in the ”old” solution are about 28,50 ECU, but the real costs are much higher, because the IC’s with minimal delay time must be sorted out. Additionally, there are costs for the manufacturing, assembly and test of the PCB of about 42 ECU. In summary the effective total cost for the old solution is more than 150 ECU.

The direct material costs for the AE solution will be about 50 ECU, i.e. a cost reduction of about 100 ECU.

As a result of the successful AE an increase of the turnover was expected within three categories of sale. These three categories are:

1. The existing product, i.e. Fault-tolerant Computers.
2. The memory components themselves for error detection and correction purposes in other solutions
3. The new EDAC - IC itself

We assumed the following turnover for our new FPGA based product compared with the turnover of the old one (100%):
The figures for the memory components and the EDAC IC’s are also related to the turnover of the existing product.

This results in a payback period of 12 to 18 months calculated from the date of industrialisation. The ROI, assuming a 3-year product life will be between 200 and 300%.

Furthermore, the company will have additional advantages resulting from the now existing in-house skills in FPGA design, which will allow to respond to market changes very rapidly based on the flexibility and rapid time to market features offered by this technology. Based on the EDAC system and the wide range of possible applications we believe that the AE for CINDATEC will have a lot of good long-term results.

17. Target audience for dissemination throughout Europe

CINDATEC is the typical representative of a small company coming from the R&D departments of the former GDR enterprises. The situation for other companies in this area is similar: They have a basic know-how in microelectronics and normally no psychological barrier concerning the introduction of microelectronics technologies. An important barrier for most of them is the knowledge transfer process itself that is very risky and time-consuming when doing it without assistance. On the other side, the introduction of FPGA (and sometimes ASIC technology later on) is a need for a lot of them to keep the advantage of a small company: the flexibility to react very fast to the needs of a customer.

The methodology to plan and to execute a successful knowledge transfer from a sub contractor to a FU is escribed well in this demonstrator. Also the financial advantages and the increase of competitiveness are obviously to stimulate other companies.

Experiences with the high level design language VHDL, the corresponding simulation tools (V System) and the acquired know-how in FPGA technology (type selection, programming, application and test) can be topics for training activities in the technical area.

The advantage of this AE is that the processing of such a project can be clearly demonstrated. Especially the continuous work with the subcontractor, the relevance of a proper planning and the positive experiences with the tools can be shown.

On the other side, the AE is a good example to show the fast changing market in the field of microelectronics applications and the fact that besides the effort for the prototype development an additional effort for industrialisation is required that should not be underestimated.

The replication of methodologies is not only restricted to companies from the industry sectors aircraft/space technology, information processing and electrical engineering and consulting. The basic principles for the knowledge transfer are similar also for companies from other industry sectors having a start situation equal to CINDATEC. The benefits and improvements in the field of computer technology and information transfer processes and data safe data transfer and handling processes are convincing arguments.

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<td>100</td>
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Table 3: Expected turnover
Hence the AE can be used for management as well as technical training for companies in all industry sectors, especially information technology, process control, medical equipment, aircraft and space technology. The companies should be seeking to introduce FPGA technology and VHDL based system design methodologies.