FUSE Demonstrator Document

Data Access Arrangement ASIC for fax/modem devices

AE No. 24613

Associated TTN : INTRACOM S.A.

July 1999

A.E. ABSTRACT

CRYPTO S.A. is engaged in the design, production and marketing of a full range of voice/fax/data modems since 1984. It designs and manufactures modems and has a full range of products for the data telecommunication needs of the national and international market.

The objective of the FUSE AE was to develop a Data Access Arrangement (DAA) ASIC which interfaces the modem data pump voiceband analog signals with the external phone line. This totally solid state new technology replaces line transformers and electromechanical relays, providing a full featured DAA, for all types of voice/fax/data modems and it is compatible with PTT homologation requirements in any country of the world.

In the previous modem product line, the DAA was being implemented using standard components on a PCB. The new line of modems achieved an average 16% cost reduction compared to the older version and assisted the company to booth its business expecting its sales to raise up to 70.000 pieces until 2003 while with the older version the sales couldn't pass 23.000 pieces for the same period. In case that a customer of our company is interested only for the new DAA part and not for the whole fax/modem product (i.e. fax/modem manufacturers), Crypto can offer a module DAA component based on the two ASIC chipset. All the DAA functionality is included in this single module component which can be inserted as a single component, during modem assembly, to the modem main PCB. Discussions are already in progress with far east fax/modem manufacturers that they are interested for this new DAA module.

The main lesson that we acquired from this AE is that giving a proper amount of effort at the start, in the extraction of detailed specifications and in design and simulation phase, is essential in an ASIC development project.

The AE duration was 18 months. Taking into account the effort of 526 person days and the project's cost of 119 KEuros, the payback period is estimated at about 38 months and FUSE ROI at 185% for the entire 4-year period of the products lifetime. The total industrialization cost is approximately 219 KECU.

KEYWORDS AND SIGNATURE

Keywords : fax/modem devices, ASIC technology, mixed analog/digital, telecommunications, telemedicine, teletraining

Signature : 5-14204501420-4-3002-1-30-GR

1 COMPANY NAME AND ADDRESS

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2 COMPANY SIZE

CRYPTO's turnover is 900 KECUs (1998). CRYPTO employs 18 people. Those are by department as follows: 1 General Manager, 4 Administrative, 3 Sales, 4 R&D (2 full time and 2 part time), 4 Production (part time) and 2 for Service and Technical support.
In the project were engaged the 4 R & D Electronic Engineers and the 2 Technicians. All engineers and technicians have microelectronics expertise in the voice/fax/data telecommunication area.

3 COMPANY BUSINESS DESCRIPTION

CRYPTO, as it was referred, is engaged in the design, production and marketing of a full range of voice/fax/data modems since 1984. It is the only Greek company which designs and manufactures modems and has a full range of products covering all customer data telecommunication needs.

The robust design of CRYPTO products ensures reliable and error-free connections under the hardest line-conditions. CRYPTO modems provide the multi-country support feature, in order to meet individual country telecom approval requirements.

To attract and retain strong customer relations, CRYPTO strives to offer the best possible service, products of excellent quality, quick delivery times and competitive prices. Our company emphasizes in R&D and quality control as two critical areas of activity for remaining competitive in the marketplace.

CRYPTO in the domestic market, is well known in the commercial, governmental and institutional areas for product reliability and provision of the best technical and sales support. Our company is the official supplier of the Greek X.25 Public Data Network Hellaspac, having installed the last 4 years 3,500 modems.

In the international market, CRYPTO started exporting at the beginning of 1994 aiming to build a network of Distributors, VARs and OEMs for the voice/fax/data modems.

4 COMPANY MARKETS AND COMPETITIVE POSITION AT THE START OF THE AE

At the start of the AE the Greek market was penetrated by cheaper imports from brand name products and no name products, manufactured in Far East countries, which, although lack in the functionality and abilities of the locally produced units, manage to sell due to their lower price. The main competitors that are active in the Greek market are:

1. US Robotics (US),
2. Bocca (US),
3. Multitech (US manufactured in Taiwan), and
4. Microcom (US manufactured in Taiwan)

through their local distributors, having end user prices at around 183 ECU (28.8 Kbps modems).

The sales price for the locally produced CRYPTO 28.8 Kbps modem was higher than 200 ECU. At the start of the AE the net profit was at 15% due to the high cost of material and time, which was spent for testing and adjustments. In the following table the CRYPTO's modems market share is given over past 3 years (1995-1997). It is obvious that it was continuously reduced and we had to act immediately.

Year	Market share
1995	24%
1996	15%
1997	9%

The introduction of the new DAA part will help our company to reduce our product's cost and achieve higher profits. To the best of our knowledge two other solutions have been recently introduced with respect to the DAA circuit:

- the Redback RB02.1 hybrid, by Pascom Technologies Pty Ltd. of Australia, and
- the KRYPTON $K^2$930L chip-set, by Krypton Isolation Inc. of USA.

The aforementioned are, however, only partial solutions to the problem as they do not comply with the optional requirements that our existing discrete modules based DAA satisfies and which are important to most of our customers.

At the start of the AE the market status is given in the next table:

Start of the AE (6/97)		
Total Market size (pcs)		**Crypto's share (%)**
40,000		**9%**
Crypto's models		
	pcs	**%**
Total	**3,500**	**100%**
Databank 288VF	634	18%
Extra 336 ext	1,531	44%
Extra 336 card	301	9%
Compact 288	730	21%
Surfer 288	304	9%
Denotes modem that new ASIC will be fit in		

The competitive models with features and prices are given in next table:

Crypto's modems competition

Crypto's modems	competition	**Speed**	**1997 Retail Price**	**1998 Retail Price**
Databank 288VF professional		**33.6K**	**303**	**242**
	USR courier		303	242
	Multitech		364	273
Extra 336 ext		**33.6K**	**121**	**73**
	Microcom 33.6K		136	
	US R 336K EXT		124	
	ZOOM 33600 SVD,EXT		124	82
	ZOOM 33,6 ext ret		121	70
	BOCA 33.6K		123	
	SUPRA 336 ext ret		100	
	no name		88	33
Extra 336 int card		**33.6K**	**109**	**45**
	USR 33600 INT		109	
	ZOOM 33,6 int ret		103	45
	no name		76	24
Compact 288VF		**33.6K**	**136**	

portable Surfer 288 ext		**33.6K**	**109**	
PLUS 56K ext		**56K**		**182**
	USR MESSAGE			173
Extra 56K ext		**56K**		**93**
	USR 56K V90 V-F-D			100
	ZOOM 56 ext retail V90			86
	SUPRA 56 ext ret			78
	GVC 56 EXT RET			65
	no name			56
Extra 56K int card		**56K**		**66**
	ZOOM 56 int retail V90			80
	SUPRA 56 int ret			50
	no name			37

Just before the conclusion of this FUSE AE the market situation was as follows:

- Modem speed had increased to 56.000 bps
- Modem prices had dropped dramatically
- The market size had increased to 60.000 pcs
- Low cost modem market had increased a lot (in volume) compared with full featured high end modems
- Greek Drachma had devaluated by 15%
- Low cost modems which manufactured in Far East, increased their market share considerably

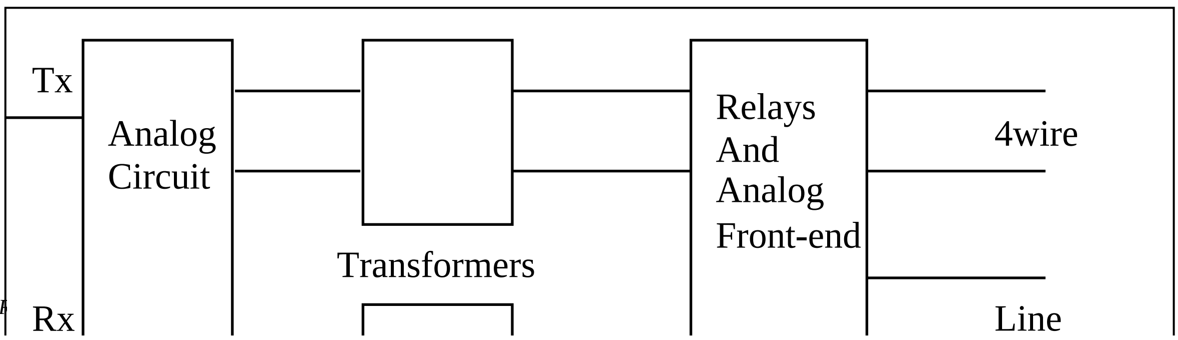
With the new product line we expect to recover a considerable amount of the market share loss.

5 PRODUCT TO BE IMPROVED AND ITS INDUSTRIAL SECTORS

Description of existing Data Access Arrangement

The Data Access Arrangement (DAA) is a circuit consisting of passive and active analogue components, which are combined with digital logic due to form the actual interface between the voiceband analogue modem signals and the telephone line.

The already existing DAA circuit satisfies certain minimum obligatory requirements for the low-end market and also some optional requirements for the high-end market depending upon the specific modem implementation. A block diagram of its internal structure is given.



Obligatory requirements

1. Electrical isolation between telephone line and modem. This value ranges from 1000 VAC to 3750 VAC depending on specific country PTT requirements.
2. Pulse /Tone dialing
3. Phone line DC current loop holding capability with a typical value of 30 mA.
4. Phone line ring detection
5. Conversion of modem 4-wire unbalanced line to 2-wire balanced telephone line
6. Phone line impedance matching

Optional requirements

1. Leased Line support for 2 wire and 4 wire leased lines
2. Caller ID detection
3. Voice support for Voice/Fax/Data modems operating as answering machines or voice mail systems.

The existing DAA circuit as shown in block diagram, is used by our company on modems produced today, satisfies all above mentioned obligatory & optional requirements, i.e. it is a full featured DAA.

Circuit functional description

1. The electrical isolation is achieved by the use of transformers, opto-coupler and electromechanical relays.
2. A relay is also used for pulse dialing.
3. A circuit is used for the dc current loop holding.
4. An optocoupler with associated circuitry performs ring detection.
5. An operational amplifier is utilized for the 4 to 2 wire conversion.
6. Impedance matching is achieved by transformers and resistors.
7. Leased line support for 2/4 wire is achieved by transformers.
8. A relay supports caller ID detection.
9. A relay is used for switching between normal modem fax/data operation and answering machine or voice mail system operation.

Reasons to innovate

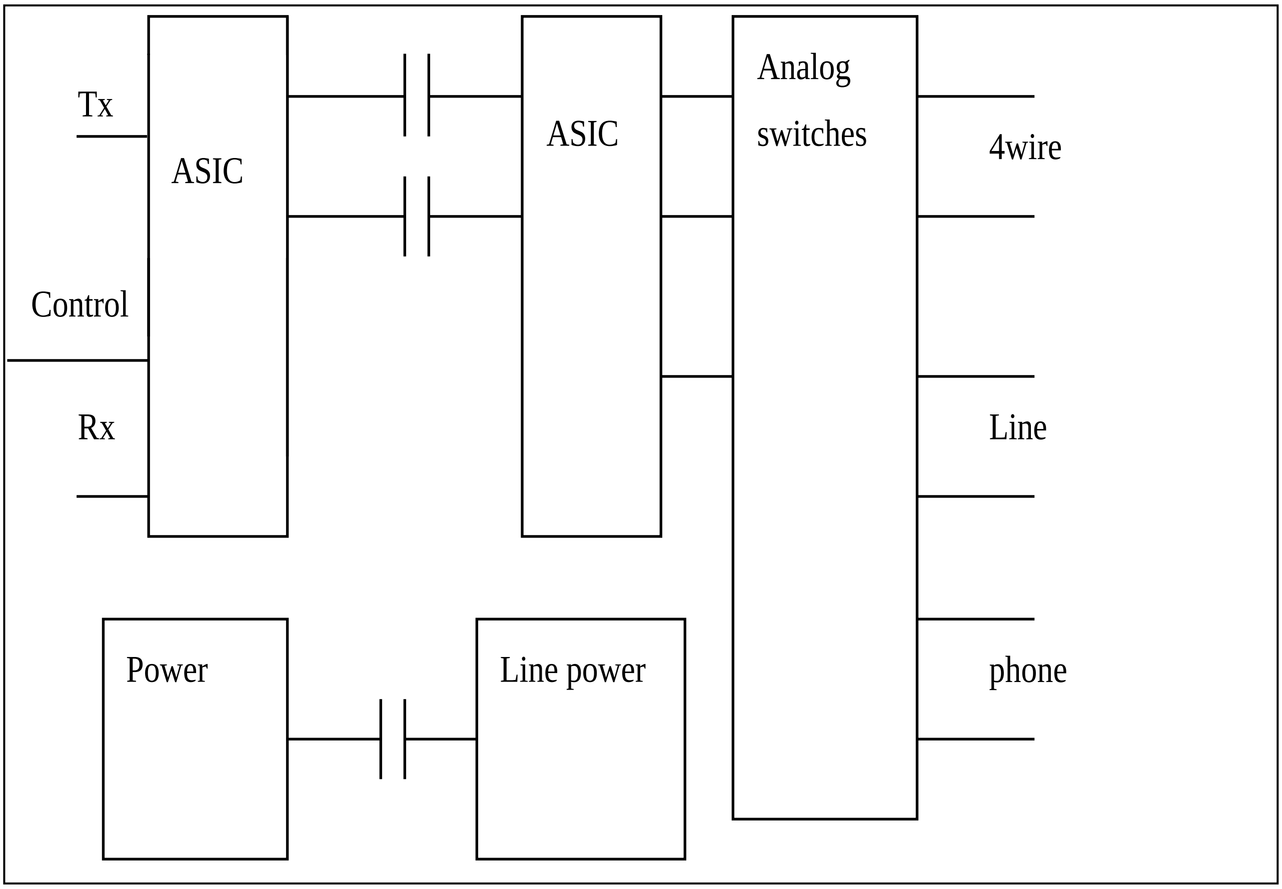
The reasons to innovate were:

- Need for enhanced system performance
- Uniform system performance for all production units
- Shorter Quality control and repair times
- One DAA component for all types of modems in our product line
- Lower power consumption
- Less R&D cost for new modems
- Less homologation time & cost for new modems

The following Crypto products are to be improved by the use of the new ASIC technology:
Databank 288VF, Extra 56K, Extra 336, Plus 56K and PCI 56K internal card.

6 DESCRIPTION OF THE TECHNICAL PRODUCT IMPROVEMENTS

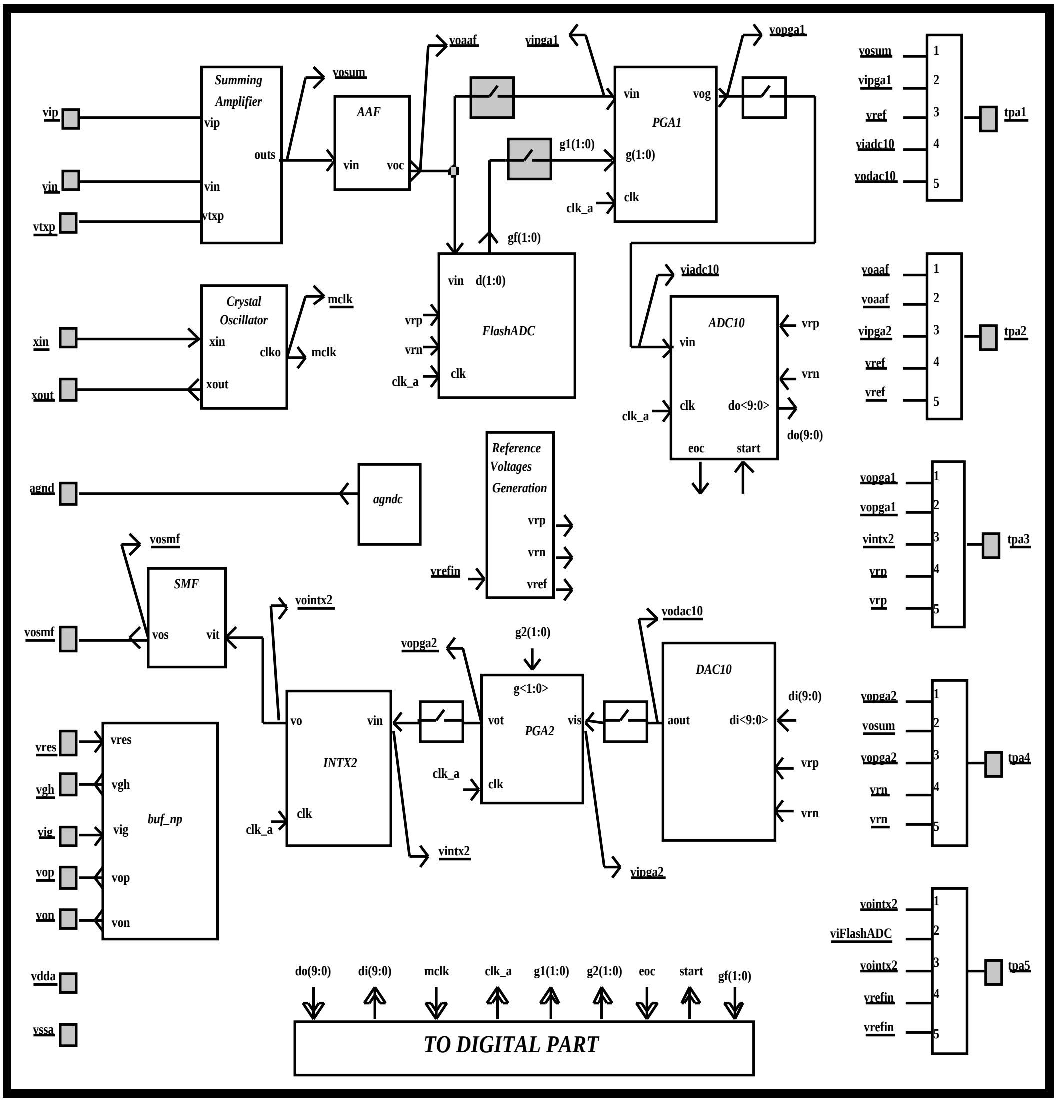
The improved DAA, as shown in the block diagram, is an all silicon alternative to our existing full featured DAA.



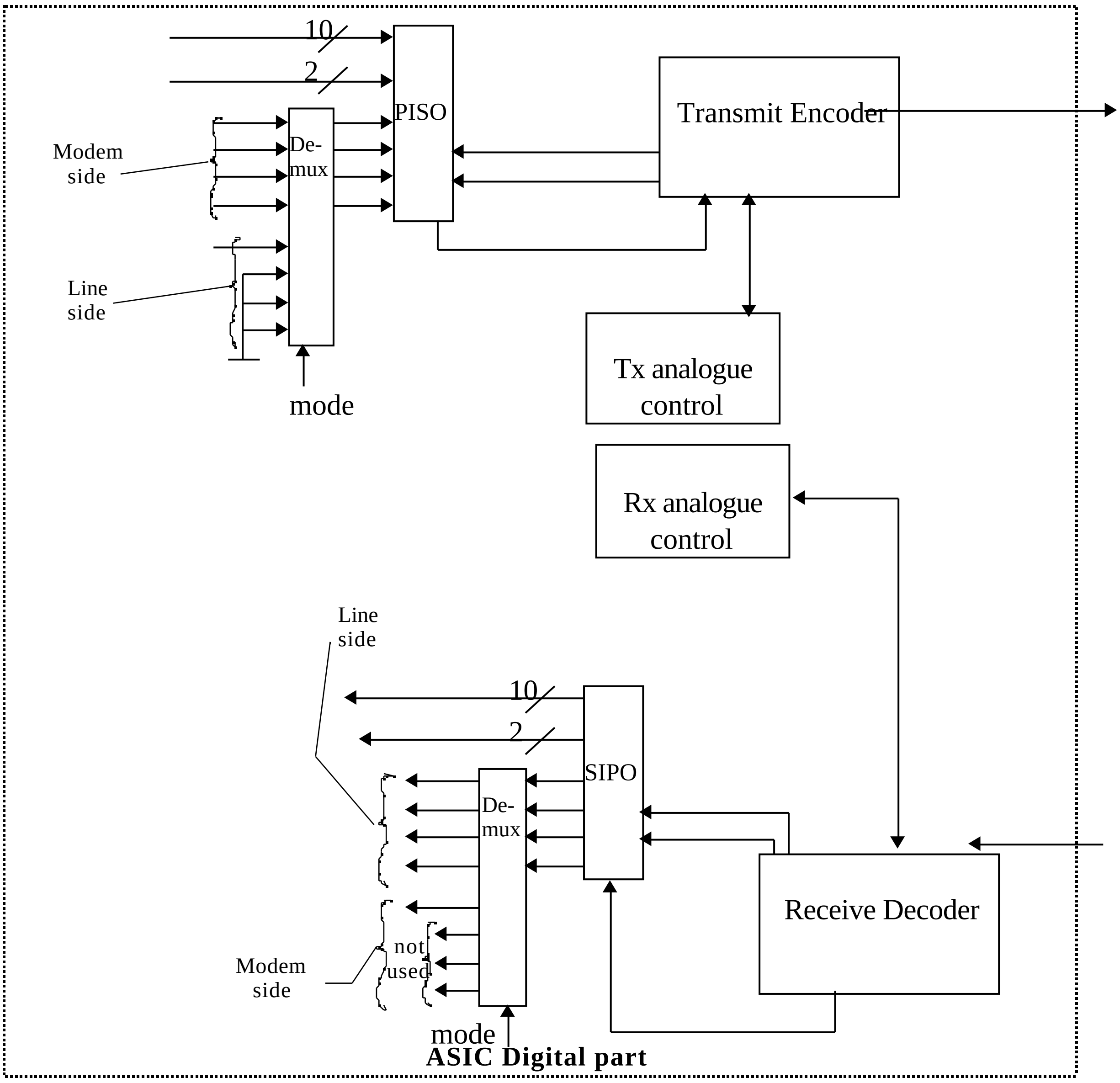
Circuit and Functional Description

As shown in block diagram, two mixed analogue-digital ASICs are used, one at the modem side and the other at the phone line side. These two ASICs are identical. The connection between the two ASICs is achieved through 100pf capacitors which can withstand voltages of up to 3,000 Volts, in order to obtain the required electrical insulation between the phone line and the modem electronics.

The analogue part of each ASIC includes two major blocks : the receiver part and the transmitter part. In the ASIC that functions at the Telephone Line Side the transmitter's input is an analogue signal, that is converted to digital and it is applied to the framer as input. The framer's output (1 bit) is transmitted through the "opto" to the framer's input of the ASIC that functions at the Modem Side. The output of the framer is shorted at the receiver's input and is converted to analogue signal output. The same is valid for an analogue input signal from the Modem Side to the Telephone Line Side.



ASIC Analogue part


10
2
PISO
Transmit Encoder
Modem side
De-mux
Line side
mode
Tx analogue control
Rx analogue control
Line side
10
2
SIPO
De-mux
not used
Modem side
Receive Decoder
mode
ASIC Digital part

The Digital Part is also composed of the Transmitter part and the Receiver part. The main task of the Transmitter part is to receive in parallel the 16-bit digitised data, convert them into serial data and, therefore, compose a frame which will be sent for transmission through the single-bit output pin to the opto-coupler. On the other hand, the Receiver part is responsible for decoding the received serial data frame and convert the data into 16-bit parallel form, through a Serial-In-Parallel-Out block (SIPO).

The peripheral components used, are:

Oscillator
The crystal used has a nominal frequency of 16MHz. This is located at the ASIC of the modem side. There isn't another crystal at the ASIC of the line side. Instead, the 16MHz frequency is transported to the line side, by the use of a 100pF/3000V capacitor. This achieves perfect synchronization of the two ASICs and reduces cost as well.

Power Supply
The power supply required to power the components at the phone line side, is comprised of two amplifiers operating in class B, which connect at the outputs CLK and CLK-b of the integrated circuit. The amplifiers can provide enough power not only for the phone line electronic components, but they can also feed an external telephone set for modem voice operation. The electrical isolation is again achieved by 3 capacitors of 4.7 nF / 3,000 Volts.

Control of Switching between 2-wire and 4-wire
In order for the modem to control the switching between 2 wire PSTN or Leased Line and 4 wire Leased Line and visa versa a 4053 signal multiplexer was used.

Phone Line Switching
For this design we used our own design switches, based on DMOS transistors. The benefits are:

- Contact isolation up to 400 Volts (which is much better than the 125 Volts offered by the commercial relays)
- Very low power consumption
- Very low cost

Telecom dc current loop circuitry
This circuitry is a 20 to 30 mA current source, which is controlled by the Pulse pin of the ASIC. It is used for offhook and pulse dialing functions.

Ring Detect Circuitry
The ring voltage on the telephone line can be as high as 180 Volts peak. Therefore ring detection is done using discrete components, which lower the high voltage and the resulting signal is fed to the ASIC to be transferred to the modem side.

Digital part of each ASIC is approximately 5000 equivalent gates and layout dimensions are 4300x5500 sq.um.

Our product line improvements are as follows:

- **System performance**
  Totally solid state technology has no variation in performance as analog components. Therefore production units have all similar performance between them and most important of all, this is the same performance given by the designed and tested prototype, as produced by the R&D team.

- **Shorter quality control and repair times**
  It is far more easier to test and repair solid state components, compared to analog ones

- **One DAA for all modems of our product line**
  Fewer components means less overhead in our raw material stock and easier assembly

- **Lower power consumption**
  Yields to smaller power supply, resulting in lower manufacturing cost and prolongs operation time for battery powered portable modems and pcmcia modems that draw power from notebook computers.

- **Less R&D cost for new modems**
  Since the same DAA can be used in all modems, this reduces redesign R&D cost and also reduces product time to market

- **Less homologation time and cost**
  Once the DAA is homologated, which is the key component interfacing to the phone line, modem homologation is a simple, fast and less costly procedure.

DAA functionality is very critical for the performance of a fax or a modem device. Although modem technology changes rapidly, basic DAA technology remains almost the same for 20 years now, with the exception of increased speed in terms of bits per second. The component which has to be changed to follow this speed increase, is the telephone line transformer, which has a lot of limitations due to passive components it consists of (core and windings) and the way it is manufactured.

Our totally solid state DAA solution, does not have any of the problems mentioned before, which are associated with the old technology of the passive components. Therefore this new technology is suitable for all the existing fax & modem devices today and it will be compatible with any new ones in the near future, since it covers all basic and optional features of a DAA. In this sense this totally solid state DAA it is not considered a fast changing technology.

On the other hand the totally solid state implementation has a very big advantage, compared to a passive solution. The price of a solid state DAA implementation drops dramatically, as the component production volume increases. Taking into account that our solid state solution is full featured, that means we can sell it to other fax & modem manufacturers (who they have very big volumes) and we can benefit from the volume price drop. (see sections 15 & 16 for cost analysis). It must be noted that almost all the DAA functions are implemented by the ASIC, with the exception of a few components (like some ring detect components) which may require different values by specific PTTs in different countries and therefore are left outside for flexibility reasons.

It is also worth noting that the only other solid state solution available today (US company KRYPTON using a 3-ASIC chipset), uses nearly the same components with larger area and higher pin count, that is 56 components with a pin count of 256, towards our solution of 57 components with a pin count of 245, with much more functionality included in the DAA.

In the next table the difference in component cost is given between the previous DAA and the new one.

Previous DAA	**PCS**	**Price(ECU)**
Components	47	**10.70**
pin count = 77		
New DAA (100 Kpcs)	**PCS**	**Price(ECU)**
Components	55	3.04
ASIC [x2]	2	3.32
module components		0
pin count = 245		**6.36**
		-41%
New DAA (5000 Kpcs)	**PCS**	**Price(ECU)**
Components	55	3.04
ASIC [x2]	2	2.31
module components		0
pin count = 245		**5.35**
		-50%

It is evident that the new DAA with the two ASIC chipset consists of more components than the previous one (57 vs 47), but is also obvious that there is a large difference in their prices and their functionality.

Also the new DAA provides Crypto with another option:
In case that a customer of our company is interested only for the new DAA part and not for the whole fax/modem product (i.e. fax/modem manufacturers), Crypto can offer a module DAA component based on the two ASIC chipset. All the DAA functionality is included in this single module component which have 20 pins and can be inserted as a single component, during modem assembly, to the modem main PCB.

There are many trade offs of the appropriate decision each one related to a different cost center. A detailed DAA cost comparison of the alternative solutions is given to the following table:

Module / Chip Set solution comparison

	Previous DAA	100 Kpcs ASIC Chip Set	5000 Kpcs ASIC Chip Set	100 Kpcs ASIC Module	5000 Kpcs ASIC Module
Component cost	10.700	6.360	5.350	6.810	5.800
Assembly cost	0.667	1.378	1.378	0.014	0.014
Q & A cost	0.128	0.264	0.264	0.003	0.003
Repair cost	0.147	0.304	0.304	0.003	0.003
PCB space cost	3.030	3.030	3.030	0.758	0.758
Homologation cost	0.167	0.167	0.167	0.017	0.017
DAA R&D cost	0.673	0.000	0.000	0.000	0.000
ASIC NRE costs	0.000	0.255	0.005	0.255	0.005
Total DAA cost	**15.51**	**11.76**	**10.50**	**7.86**	**6.60**
		-24%	-32%	-49%	-57%

7 CHOICES AND RATIONALE FOR THE SELECTED TECHNOLOGIES, TOOLS AND METHODOLOGIES

7.1 Technology options

There are a number of technologies that were considered for the realisation of this application experiment. The FPGA technology due to the mixed analogue-digital nature of the design proved to be inappropriate for the needs of the experiment. The use of a FPGA combined with a microcontroller or a DSP with ADC was not implemented for the following reasons:

- It would have a limited replicability in future company's product upgrades.
- Using an FPGA we can not have the required system design safety and reduced size/volume compared to an ASIC.
- Production cost would be very high for the quantities that we are considering for our product.

Furthermore, concerning the rejection of the technical solution of an FPGA together with external A/D components, please note that the mixed ASIC was selected due to the following reasons:

- Enhanced Reliability.
- Easier System maintenance. Another important feature that stems from the use of a single integrated device (ASIC).
- Advanced technology - Improved performance.
- Increased Immunity to Unauthorised Production. By nature an ASIC is an extremely hard to reproduce electronics device.

On the other hand the choice of an MCM fabrication technology was not justified by the proposed circuit's complexity, technical characteristics and specifications in addition to the high fabrication cost. So, the most appropriate technology proved to be ASIC technology which can combine both digital and analogue functions in the same component. The use of 2 identical ASICS was necessary as the 3 KV insulation could not be implemented internally.

7.2 Fabrication Technology of the ASIC

Various fabrication technologies were considered for the implementation of the ASIC, the heart of this application experiment. The BiCMOS technology was not required since the design did not require high current gains or drive high currents at the outputs. Since our analog cells were easily available in many libraries, we could use any submicron CMOS process available in the MPW (Multi-Project-Wafer) runs that were offered by EUROPRACTICE. A number of technologies were examined and quotations were requested to achieve low fabrication cost of prototypes initially and latter low cost for mass production. Finally the AMS 0.8um CMOS CYE technology was chosen as it had a good co-promise between cost and performance features and it was also offered by EUROPRACTICE (Low cost prototyping).

7.3 ASIC Design methodology and Testing

The Design Flow that was followed during the time of the development of the ASIC is given here as well as and the testing procedure. As far as the Digital part is concerned, as soon as the specifications of the ASIC were finalized, the description of the internal blocks that compose the design were described in VHDL Hardware Description Language. A hierarchical form in those descriptions was kept in a way that the lower level blocks, such as state machines, were described behaviorally while upper level blocks were described structurally. QHDL-Lite by Mentor Graphics was used during this process. The VHDL code was compiled and then extensive simulation was performed, using the same tool. All blocks, from the bottom level towards the top level were simulated until the desired functionality was achieved. Note here that QHDL-Lite was also used for the essential Mixed-Mode Simulation that was performed. Models of the Analogue cells were developed, in VHDL, for this reason.

After that, the VHDL code had to be checked whether it was fully synthesisable, and when that was assured it became an input file to the Synthesis Tool SYNOPSYS. The appropriate setup and constraints files were developed in order to fully synthesize and optimize the VHDL code according to the specifications. The VHDL hierarchical design was targeted into AMS 0.8 CYE technology. Timing Analysis was performed onto the produced Digital netlist. Adequate signal buffering was verified and strengthened where needed.

Finally the netlist in Gate Level was generated. For once more extended simulation had to be performed. The CAD tools by Mentor Graphics v.B3 (Design Manager, Design Architect, Design View-Point, Quick-Sim II) were used during the design and simulation of the digital part. The AMS Hit-Kit v2.50 covered the design flow. DFT-

Advisor, by Mentor Graphics was used in order to automatically insert the necessary scan-path into the design.

The Analogue part had been developed in parallel, using cells from the AMS Analogue Library. The ELDO analogue simulator from ANACAD was used for the verification of the analogue cells. After both the Digital and the Analogue blocks were completed, the ASIC schematic was created while the appropriate input, output, i/o and power pads were inserted.

The fabricated ASIC prototypes were tested by our subcontractor INTRACOM CEM. Digital part was tested using the subcontractor TOPAZ-V digital tester and the inserted scan-path. Analogue part was tested functionally after developing a testbench board.

7.4 ASIC to production stages

After the fabrication of the ASIC prototypes a timing period of evaluation of the new product in which the new technology is adopted must be considered. In this period a series of evaluation tests in real operation conditions have to be performed by the FU for the new prototype product. The length of this period and the number of the evaluation tests depend on the complexity of each design (of the new technology) and the variety of the conditions in which the new product will operate in its life-time. During the evaluation period, 'bugs' and weak points of the design may be extracted by the FU and modifications may be necessary on the design or the structure of the new product. In this point, if the modifications that have to do with the design are extensive, a contribution from the subcontractor may be required.

The next step is the collection of quotations by the FU of different silicon foundries for the ASIC mass production, in order the most profitable solution to be found. Factors that play a part in this stage are the volume of production, the complexity of the ASIC, the technology process that will be used and the delivery time.

8 EXPERTISE AND EXPERIENCE IN MICROELECTRONICS OF THE COMPANY AND THE STAFF ALLOCATED TO THE PROJECT

Our engineering team had expertise in PCB design of telecom systems, discrete component systems design, micro-controller programming as well as in system architectures for voice/fax/data modems. However, our engineering team did not have any experience in design and testing methodology of mixed signal analogue/digital ASICs as well as experience in technical management on an ASIC development..
Our engineering team was as follows:

Mr. George Kountouriotis
He holds a B.Sc. degree in Electronic Engineering from University of Patras and an M. Sc. Degree in Electronics and Telecommunications from Chelsea and Kings colleges of University of London, UK.
Mr. Kountouriotis is the project coordinator and he has an extensive experience of 14 years in the Data Telecommunication area.
Today is the managing director of Crypto SA and he was the first engineer, back in 1984, who designed the early Crypto modems. His experience is both in hardware modem design, as well as low level firmware development.
Mr. Kountouriotis was the most experienced person to supervise this A.E.

Mr. Christos Tsakiris
He holds a B.Sc. degree in Electronic Engineering from University of Thessaloniki and an M.Sc. degree in Electronics and Telecommunications from University of London, UK.
Mr. Tsakiris has participated in the hardware and software design of many modem types of our product line.

Mr. George Costomenos
He holds a B. Sc. Degree in Electronic Engineering from National Technical University of Athens.
Mr. Costomenos specializes in the hardware design of our voice/fax/data modems.

Mr. Philip Gemouchides
He holds a B. Sc. Degree in Electronic Engineering from University of Bucharest. He is a hardware design engineer specializing in data telecommunications and power supply design.

Mr. Thomas Georgopoulos
He holds a B. Sc. Degree in Computer Science from University of Patras.
Mr. Georgopoulos expertise is in computer simulation of hardware design and modem firmware development.

The technical expertise which was completely missing from our company and all of our staff, was in the ASIC design area. This is why we had to find a suitable subcontractor in order to obtain the know-how knowledge transfer, required by this AE.

9 WORKPLAN AND RATIONALE

In the following paragraphs the workplan that was followed during the project's execution is given along with the deviations that occurred with respect to the original workplan, the problems that were faced, the rationale behind them and the way that these were finally resolved.

More specifically the whole project was originally organised into 7 main tasks, the description of which and the work performed in each of them along with all associated issues mentioned above are detailed below. The main deviation from the original duration is that the overall A.E. time was extended by 3 months.

TASK 1: Technical Management

The company's project leader was trained by the TTN in the area of the technical management of projects so that CRYPTO was able to co-ordinate the entire application experiment. Application experiment's duration was extended 3 months more than the original provided by Technical Annex due mainly to some technical issues that are analyzed below.

Duration: 16 months (m1- m13 and m16 - m18)
In m14, m15 the fabrication of prototypes ASIC and PCB was performed and technical management was not necessary.

Crypto's Effort: 90 persondays

TASK 2: Training in ASIC Design

On-the-job training of CRYPTO's engineers on mixed analogue/digital ASIC design as well as on testing methodology and tools that were used by CEM engineers.

Duration: 11 months (m1- m11)

Crypto's Effort: 83 persondays

Since Crypto engineers had to understand deeply the ASIC technology and design this task started from the first month, but the total duration was one month less from projected, since all major effort was required at the beginning of the AE.

TASK 3: Specifications

3.1 System Specifications

Architectural study of the overall system and definition of the functional, electrical and interface specifications of the system were performed by CRYPTO.

3.2 ASIC Specifications

CRYPTO in close co-operation with CEM defined the ASIC functional, timing and operating frequency specifications, taking into account the system specifications, the current technological trends and the available technologies.

Duration: 4 months (m1-m4)

Crypto's Effort: 86 persondays

System specifications and ASIC specifications were originally planned as an one month period. In practice this time was extended to 4 months. Additional effort was 32 persondays. The reason is that after extensive research we found out that the

Modem Cost Analysis (100 Kpcs)

Modem	Dealer Price	margin	modem with old DAA cost	component cost(no DAA)	DAA Assy cost	DAA Q&A cost	DAA Repair cost	Space saving cost	DAA Homologation cost	DAA R&D cost	once DAA manufacture cost	modem with new DAA cost	cost improvement with new DAA	market share
Databank 288VF	273	60%	164	153	-1.64	-0.33	-0.33	-2.36	-0.41	-1.64	0.57	153	6%	3%
Extra 56K	85	40%	51	40	-0.51	-0.10	-0.10	-2.36	-0.13	-0.51	0.18	43	15%	50%
Extra 336	61	40%	37	26	-0.37	-0.07	-0.07	-2.36	-0.09	-0.37	0.13	29	21%	9%
PLUS 56K	167	40%	100	90	-1.00	-0.20	-0.20	-2.36	-0.25	-1.00	0.35	91	9%	8%
PCI card 56K	57	40%	34	24	-0.34	-0.07	-0.07	-1.55	-0.09	-0.34	0.12	28	20%	30%

Modem Cost Analysis (5000 Kpcs)

Modem	Dealer Price	margin	modem with old DAA cost	component cost(no DAA)	DAA Assy cost	DAA Q&A cost	DAA Repair cost	Space saving cost	DAA Homologation cost	DAA R&D cost	once DAA manufacture cost	modem with new DAA cost	cost improvement with new DAA	market share
Databank 288VF	273	60%	164	153	-1.64	-0.33	-0.33	-2.36	-0.41	-1.64	0.57	152	7%	3%
Extra 56K	85	40%	51	40	-0.51	-0.10	-0.10	-2.36	-0.13	-0.51	0.18	42	17%	50%
Extra 336	61	40%	37	26	-0.37	-0.07	-0.07	-2.36	-0.09	-0.37	0.13	28	23%	9%
PLUS 56K	167	40%	100	90	-1.00	-0.20	-0.20	-2.36	-0.25	-1.00	0.35	90	10%	8%
PCI card 56K	57	40%	34	24	-0.34	-0.07	-0.07	-1.55	-0.09	-0.34	0.12	27	22%	30%

ASIC now is 41% to 50% cheaper from the existing DAA as a chip set solution and 36% to 46% cheaper than the existing DAA as a module solution. We also have the chance to sell the module solution to other fax and modem manufacturers. We are in contacts with far east fax/modem manufacturers that have the capability of a large production. Our contacts also indicate that a small Asian modem manufacturer produces 30,000 modems per month, while a big one goes up to 200,000 modems per month and there is a lot of interest about our module solution. These figures indicate that the 5,000 Kpcs is not a big quantity for this specific ASIC and it would be possible to get an even lower price for bigger volume.

The estimated time to market for the new modems is considered to be in 4Q of 1999. A more detailed industrialization plan is given in next table.

Duration (months)	Phase	Cost (KECU)
	FINAL PROTOTYPE PRODUCTION	**10**
0,5	Silicon foundry & services final selection, including technology, packaging, testing.	
0,5	Translation of the AMS design implementation to the specific foundry technology.	
1	ASIC prototype fabrication and testing.	
0,5	Modem functional and quality tests.	
0,5	ASIC module prototype and testing.	
	TRIAL LOW VOLUME ASIC PRODUCTION AND B-TESTS	**20**
1	Trial low-volume ASIC production.	
1,5-2	Same quantity modem manufacturing. Beta testing period (by end users in real telecom environment conditions).	
	FIRST CYCLE OF ASIC PRODUCTION AND MODEM MANUFACTURING (200 kpcs)	**25**

Adding the FUSE investment amount (119 KECU) and the NRE cost of 45 KECU the total **industrialization cost** is about 219 KECU.

<u>Internal replication</u>

We intent to use the ASIC-based DAA part in the full range of company's modem product line, (e.g. type Databank 288VF, Extra 56K, Extra 336 etc.) as referred to previous economic tables in this section. Also company's engineers will use their acquired know-how in ASIC design methodology to proceed in future possible upgraded re-designs, depending on new market demands as well as on the availability of advanced ASIC fabrication technologies allowing the integration in an ASIC of other discrete components, decreasing their cost even more. Now we are familiar with ASIC technology and we have been convinced that it can give low-cost design solutions for our products and this was one of the basic benefits as a result of this AE.

16 ECONOMIC IMPACT AND IMPROVEMENT IN COMPETITIVE POSITION

As it was mentioned, the new ASIC technology is applicable to a number of the company modems and the intention is to substitute with the new technology our existing product line for these modems. Therefore the following figures do not refer to a single modem, but to the variant types of modems that we produce.

Before AE

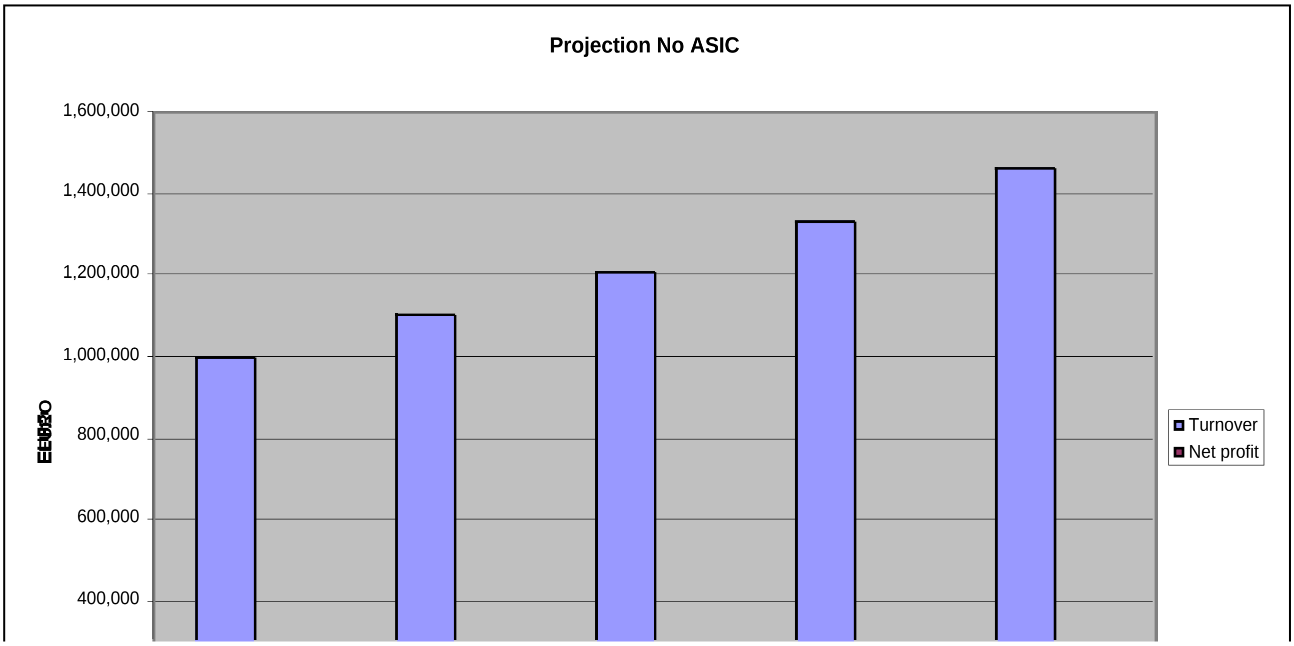
	Market size pcs	Crypto Share %
	40,000	9%
	3,500 pcs	**100% %**
Databank 288VF	634	18%
Extra 336 ext	1,531	44%
Extra 336 card	301	9%
Compact 288	730	21%
Surfer 288	304	9%

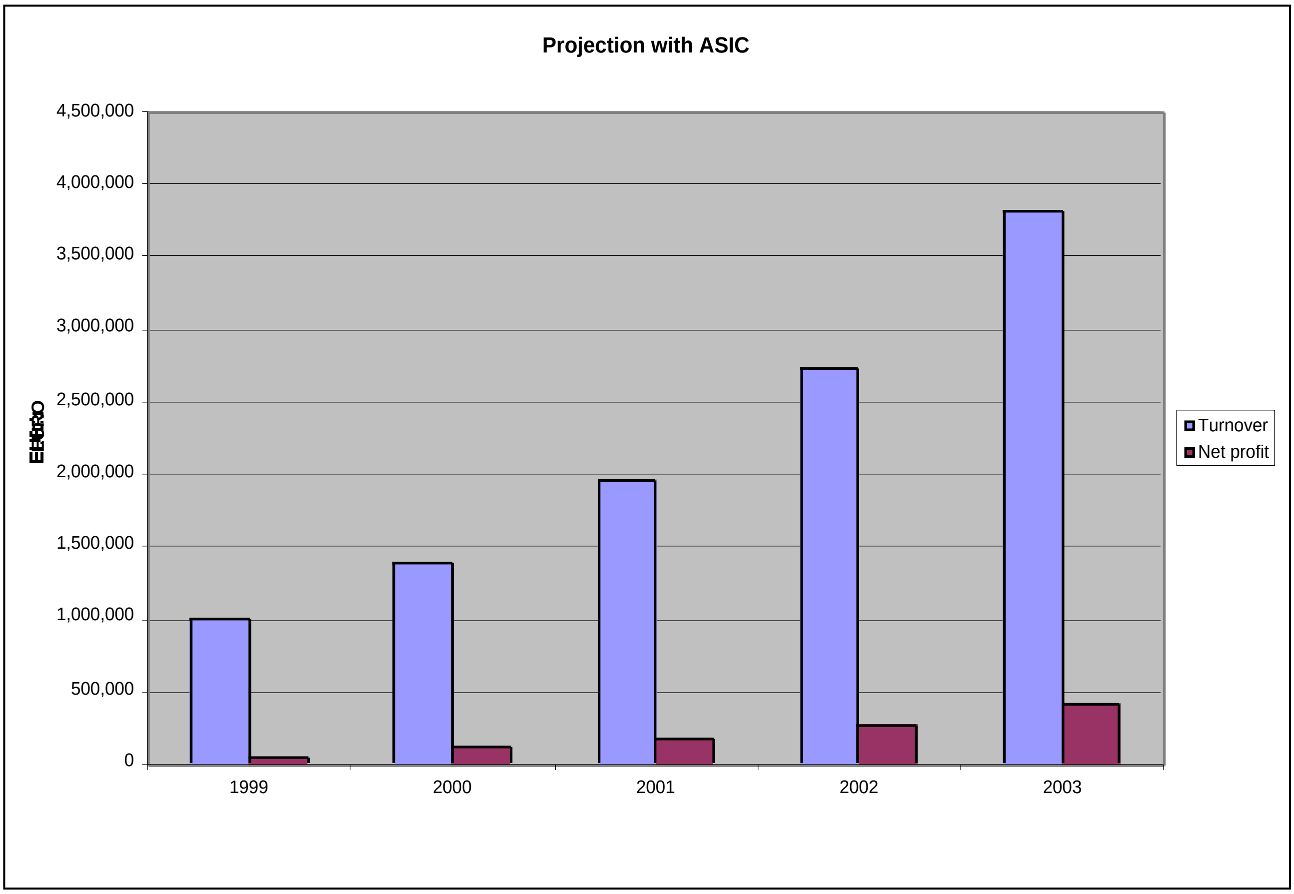
After AE

	Market size pcs	Crypto Share %
	60,000	14%
	8,500 pcs	**100% %**
Databank 288VF	230	3%
Extra 336 ext	3654	43%
Extra 336 card	1069	13%
Compact 288	0	0%
Surfer 288	0	0%
PLUS 56K	729	9%
Extra 56K ext	1930	23%
Extra 56K card	888	10%

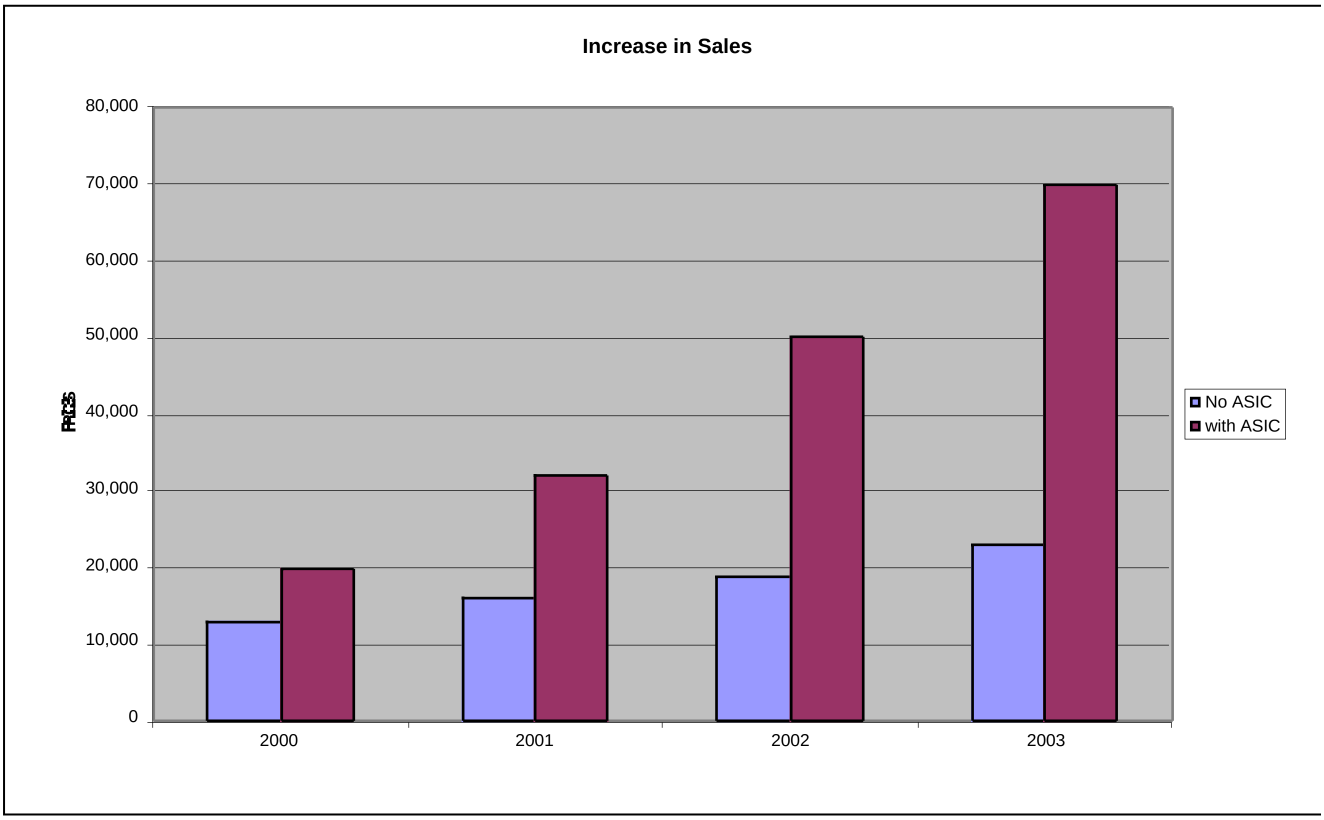
Denotes modem that new ASIC will be fit in

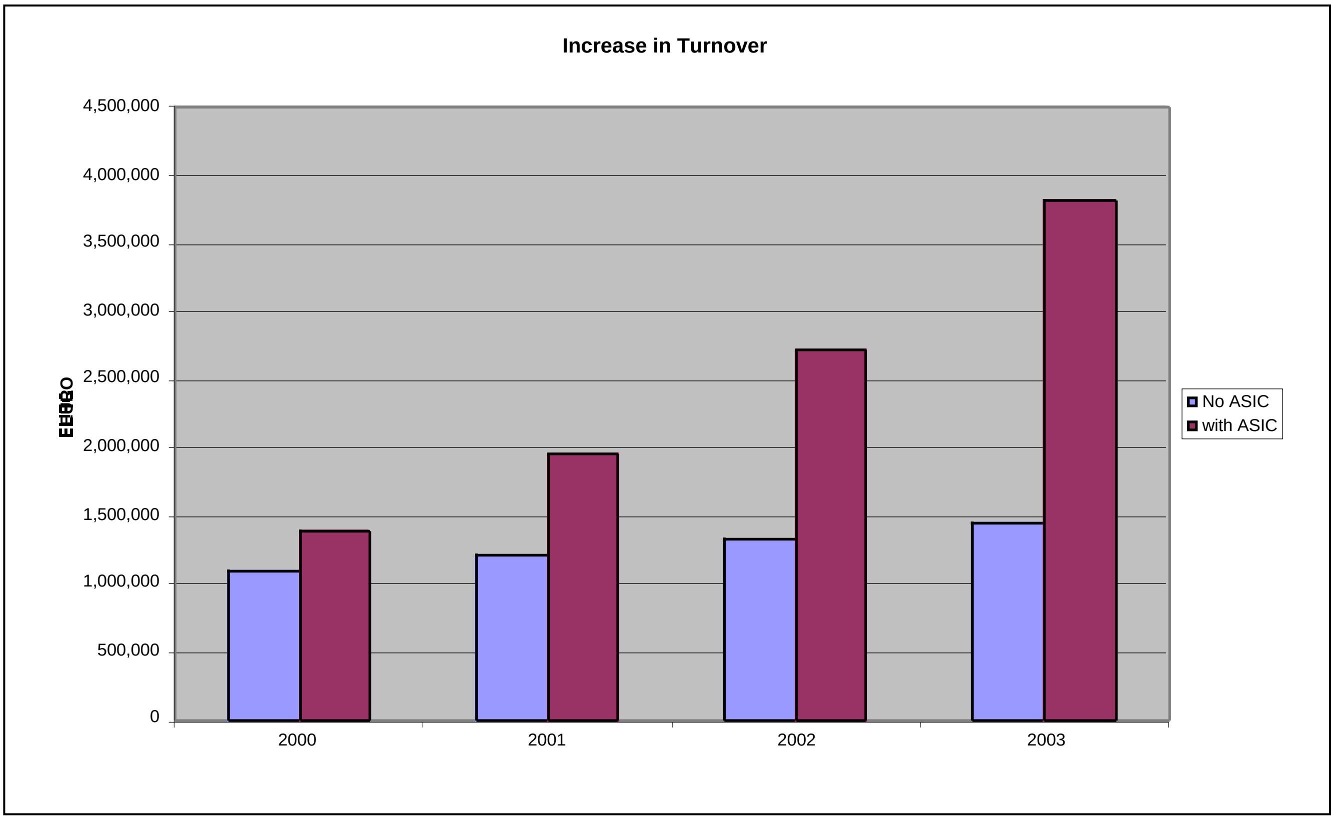
The cost of the ASICs, the cost of the improved products and the selling prices, as well as other companies that produce DAA chip-sets are given in the previous sections 4, 5,15.

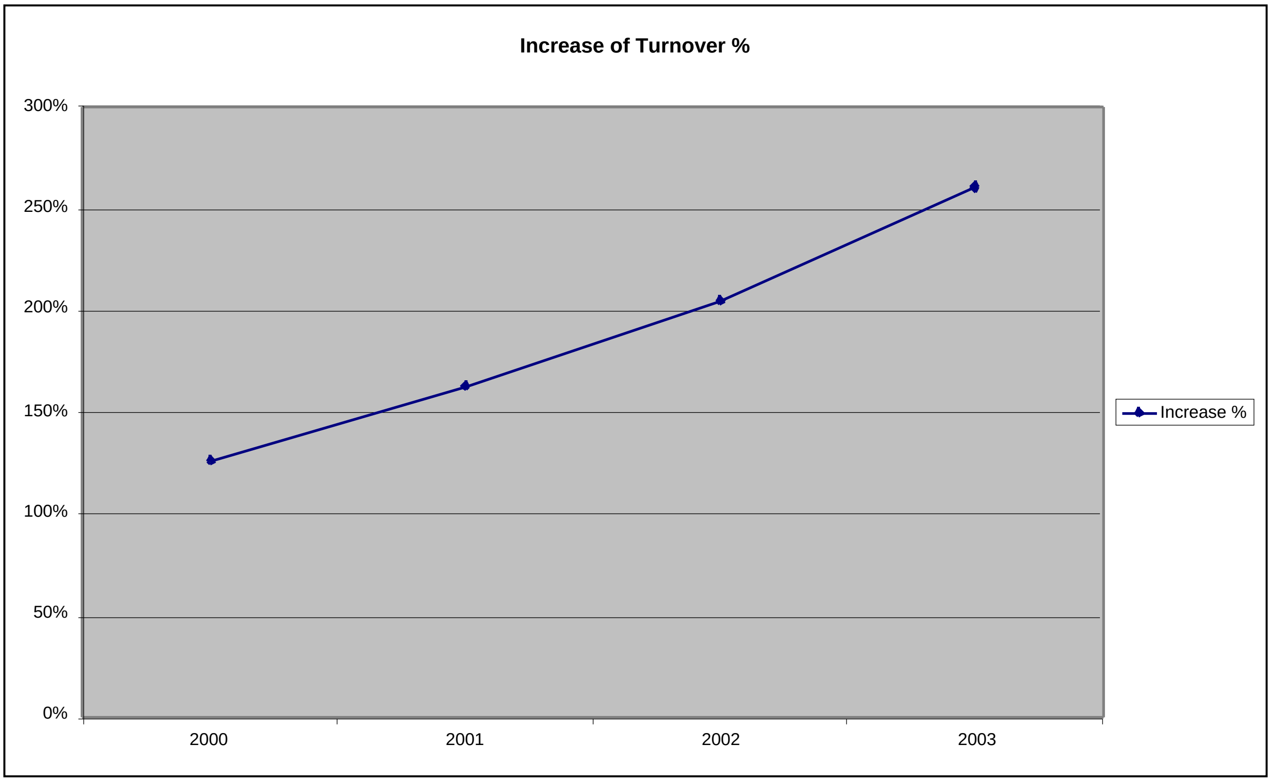




Also, increase in sales and turnover is shown, after introduction of the new technology.




Increase in Turnover
4,500,000
4,000,000
3,500,000
3,000,000
2,500,000
2,000,000
1,500,000
1,000,000
500,000
0
2000
2001
2002
2003
No ASIC
with ASIC


Increase of Turnover %
300%
250%
200%
150%
100%
50%
0%
2000
2001
2002
2003
Increase %

Payback period is calculated, based on actual AE costs (119 KEuro) and net profit increase (220 KEuro) resulting from AE introduction in a 4 year period and it is found to be 38 months.
Return on Investment (ROI), also based on above figures is calculated as 185%, 4 years after product launch to market.

It is worth noting, that it is our company intention to further improve the ASIC designed, as soon as a new high voltage technology is available, in order to include in a single ASIC all required circuity. This improvement will give a DAA consisted of one ASIC and some peripheral external circuitry.

It is also worth noting that this new solid state ASIC technology could be applicable not only to voice/fax/data modem devices, but also to regular fax machines. It is our company's intention to explore possibilities of cooperation with such fax machine manufacturers.

17. TARGET AUDIENCE FOR DISSEMINATION THROUGHOUT EUROPE

Crypto established a best practice design approach based on mixed analog/digital ASIC technology that was capable to reduce the overall product cost by 16%. The results of this AE will be interested to other companies mainly SMEs which follow the traditional bulky discrete components-based approach leading to high cost and limited competitive products. Specifically the managing directors of these companies as well as their technical directors (for small size companies maybe these will be the same persons) should be aware of the benefits of the introduction of the ASIC technology both to the business of the company (increase in market share, increased profits/sales) as well as to the improved performance of the device in terms of power consumption, minimised required adjustments, easy of maintenance etc. So the target SMEs may specialize in the areas of modems, telegraph and telecom apparatus and equipment, TV and radio receivers, computers/information processing equipment as well as toys and games. In terms of PRODCOM codes these SMEs are:

- 3220 (Telegraph and telephone apparatus and equipment and radio and electronic capital goods)
- 3230 (television and radio receivers)
- 3002 (computers and other information processing equipment)
- 3650 (games and toys).

available ASIC technology could not support in one chip the high isolation voltage in the range 1250 to 3750 VAC required by Telecom authorities. During the project's feasibility study stage we had been informed by leaflets that the specific technology would be enriched with a number of high-voltage features, but until the detailed ASIC technical specifications extraction phase none of these features had been added. So we had to find an alternative solution to this problem and we were forced to change the ASIC specifications and adapt accordingly the system design, so that system specifications remain the same. The workaround was to use 2 low voltage identical (to reduce cost) ASICs and achieve the high voltage isolation by the use of high voltage capacitors, to provide a connecting path between the ASICs. Note that the only other DAA solid state implementation that we are aware of, is given by KRYPTON Isolation Inc. of USA, which uses 3 different ASICs in order to achieve the high voltage isolation.

TASK 4: Design

4.1 ASIC Design

The ASIC was designed by CEM according to the methodology outlined in section 7 using VHDL, the AMS Design kit 2.50 provided by EUROPRACTICE and 0.8 um standard cells CMOS technology. CRYPTO actively participated in this process.

4.2 PCB design

The existing board was re-designed by CRYPTO to accommodate the new ASIC, the optocouplers and the required power supply circuit.

Duration: 10 months (m4 - m13)

Crypto's Effort: 177 persondays

ASIC design, was delayed by 2 months since system and ASIC specifications were delayed and due to complexity of the mixed analog/digital circuitry implementation and to some problems accounted by our subcontractor in the use of the development tools (they have switched from AUTOLOGIC II by Mentor Graphics to SYNOPSYS synthesis tool). Duration of 4.1 was extended from 8 to 9 months (m4-m12).
The PCB design was actually started at the end of the ASIC design period (end of the month m12) and finished in the next month (m13) since the full information about the exact pin-out of the ASIC was derived after the layout phase of the ASIC.
Total additional company's effort for TASK 4 was 51 persondays.

TASK 5: Fabrication

5.1 ASIC fabrication

The netlist produced during ASIC design was used for layout generation and subsequent fabrication-packaging using EUROPRACTICE MPW services.

5.2 PCB fabrication

The Gerber files produced as a result of PCB design were sent to a local manufacturer for producing the prototype boards.

Duration: 4 months (m13-m16)

Crypto's Effort: 0 persondays.

There was no occupation in fabrication procedures from company's engineering team. ASIC fabrication was delayed since the ASIC design was delayed. The actual duration was 3 months, since it was sent to foundry mid of 13th month and samples were received mid of 16th month. PCB fabrication started immediately when PCB design was finished and took one month to be delivered instead of the 2 months that were forecasted.

TASK 6: Testing/System Integration

6.1 ASIC testing

Testing of the ASIC prototypes was performed by INTRACOM's CEM using TOPAZ-V tester for the digital part and functional testing for the analogue part. Ten prototypes were tested and verified by INTRACOM ASIC center (CEM). Nine of them worked perfectly while the 10th was working only in receive mode.

6.2 System integration and testing

Integration of the whole system and functional testing were completed by CRYPTO.

Duration: 3 months (m16-m18)

Crypto's Effort: 72 persondays

System Integration and Test started as soon as we received the ASIC samples and the actual duration was 2.5 months (in m16-m18), i.e. 15 days more than projected. Total actual company's effort for TASK 6 was as planned.

TASK 7: Dissemination/Awareness

This task involved preparation of the appropriate information material (demo document, flyers etc.), and participation in TTN workshops, international fairs (Infosystems, October 98, Salonica and an exhibition in Austria).

Duration: 2 months (m17-m18)

Crypto's Effort: 18 persondays

Started at the mid period of System Integration and Test and the duration was 2 months as forecasted.

Risk Analysis

The development of the ASIC was based on a previous working product made of discrete components which was well understood and had been working in a large number of modems sold to satisfied customers. In addition the technological risk of the new development was low due to INTRACOM CEM's (subcontractor) expertise in ASIC design and CRYPTO's extensive knowledge of such modem system design. So, overall a successfully working new modem system had been foreseen since the start of this AE.

Tables 3 and 4 report the duration (forecasted and actual) of each Task detailed. Note that the actual time deviates from the forecasted one.

Month	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TASK1 Technical Management	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
TASK2 Training in ASIC Design		■	■	■	■	■	■	■	■	■	■	■	■		
TASK3.1 System Specifications	■														
TASK3.2 ASIC Specifications	■														
TASK4.1 ASIC Design		■	■	■	■	■	■	■	■						
TASK4.2 PCB Design			■												
TASK5.1 ASIC Fabrication										■	■	■			
TASK5.2 PCB Fabrication				■	■										
TASK6.1 ASIC Testing													■	■	
TASK6.2 System Integration/Test														■	■
TASK7 Dissemination/Awareness														■	■

Table 3: Time to be spent for each Task as originally planned

month	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
TASK1 Technical Management	■	■	■	■	■	■	■	■	■	■	■	■	■			■	■	■
TASK2 Training in ASIC Design	■	■	■	■	■	■	■	■	■	■	■							
TASK3.1 System Specifications	■	■	■	■														
TASK3.2 ASIC Specifications	■	■	■	■														
TASK4.1 ASIC Design				■	■	■	■	■	■	■	■	■						
TASK4.2 PCB Design												■	■					
TASK5.1 ASIC Fabrication													■	■	■	■		
TASK5.2 PCB Fabrication														■				
TASK6.1 ASIC Testing																■	■	
TASK6.2 System Integration/Test																■	■	■
TASK7 Dissemination/Awareness																	■	■

Table 4: Time actually spent for each Task

Task	**Crypto's Effort (persondays)**	**Crypto's labor cost (KECU)**	**Subcontractor's Effort (persondays)**	**Subcontractor's cost (KECU)**
Task 1	90	11.6	-	-
Task 2	83	10.7	6	2
Task 3	86	11	9	3
Task 4	177	22.8	90	30
Task 5	-	-	-	-
Task 6	72	9.3	9	3
Task 7	18	2.3	-	-
Total	**526**	**67.7**	**114**	**38**

Actual CRYPTO's and SC's effort and cost per task

10 SUBCONTRACTOR INFORMATION

Since the selection of an ASIC implementation (especially a mixed-signal ASIC) includes some possible risks concerning the ASIC development stages, we decided to select an experienced subcontractor located in close distance from us, for performing and consulting during the ASIC development phase, in order to reduce these risks and the time spent in communication. Especially since CRYPTO had no previous experience in the specific domain the final decision was much more difficult and critical. Our criteria for a successful consultant selection were:

Experience: Has the Subcontractor developed in the past mixed signal ASICs? Were these ASICs integrated successfully into systems?

People: How big is the ASIC department? Do the staff of this department have the attitude to comprehend our questionings and hesitations?

Tools: Do they have the proprietary software and hardware tools that are necessary for ASIC design simulation and verification? How long has this equipment been used by subcontractor?

Cost: What is the subcontracting cost?

The demands from our subcontractor were mainly two:

A. TRAINING

First of all we asked for an effective and full package of training in order to adopt this new technology and become able to repeat similar projects in the future. Our request was satisfied while the training consisted of the following six special topics:

- ✓ **Project management**: Project structuring, available tools for project analysis and monitoring, cost analysis, resource analysis, MIS introduction, special topics on information industry oriented projects.

- ✓ **ASIC specification extraction** Actually this session answers the questions: What does a well-specified ASIC project consist of and which are the most critical issues on an ASIC implementation?

- ✓ **CAD tools and CAD based procedures on ASIC design**: Introduction in VHDL, VHDL structures, design entry in VHDL, simulation on VHDL, Mentor graphics design environment, logical design entry in Mentor graphics, functional and timing simulation in Mentor graphics, using libraries for physical layout.

- ✓ **Special digital design techniques on ASIC**: Design for testability, modern techniques on synchronous design, special structures at algorithm and architectural levels, special structures at logic and layout levels, low power design, methods for functional and timing simulation.

- ✓ **Analogue design for an ASIC:** Special issues on mixed signal ASIC design, special analogue techniques, problems in analogue simulation, trends on BiCMOS technology, typical structures and implementations, examples

- ✓ **Evaluation of an ASIC based product:** Special evaluation and testing procedures.

The training policy that was followed included seminar sessions as well as on-the-job training. The topics of project management were conducted in seminars. A special training method was followed in CAD tools, Digital design techniques and Analogue design techniques included two steps: A preliminary seminar describing the most basic knowledge, and on-the-job training afterwards. Finally, the techniques of ASIC specification extraction and ASIC evaluation were conducted via on-the-job training.

B. ASIC DESIGN SIMULATION AND VERIFICATION

The second demand was a remarkable help in design phase for technical aspects that related with ASIC implementation. For this reason the preliminary digital part of the ASIC that was designed by CRYPTO was modified by INTRACOM in order to comply with the design methodology for an ASIC (in accordance to synchronous design techniques, etc.). During this specific activity our design became fully synchronous, (previously some modules had asynchronous timing) and also some modules were added to support chip testing procedures. The analogue part of the ASIC was also verified by INTRACOM and was mapped in the CYE 0.8 CMOS technology. The final design was simulated in a Mentor Graphics workstation by INTRACOM in cooperation with our Engineers.

INTRACOM also produced, through a EUROPRACTICE MPW run, the final artwork layout and actualize all the negotiations with the foundry (AMS) as well as the testing of the ASIC prototypes.

A brief profile of our subcontractor is presented below:

INTRACOM S.A. has established since 1993 the Centre of Microelectronics (CEM) within the framework of Special Action in Microelectronics in Greece. CEM is the national industrial VLSI design and Testing centre in Greece and also acted as TTN centre for Greece. It promotes R&D activities in the area of VLSI design for INTRACOM's needs and simultaneously provides similar services to Small-Medium-Enterprises (SMEs). CEM is equipped with state-of-the-art facilities including powerful SUN series workstations running MENTOR GRAPHICS CAD tools for schematic capture/VHDL design entry, digital and mixed mode simulation, logic synthesis, layout, automatic test pattern generation, Digital Signal Processing, ELDO analog simulation S/W by ANACAD, technology and vendor independent libraries, TOPAZ V digital tester running at 110 MHz for testing digital ICs up to 160 pins and FPGA development tools by XILINX and TEXAS INSTRUMENTS. CEM has currently designed over 70 ASICs for telecommunication applications, image processing and power control applications.

Considering the **contractual clauses**, no IPR-related issues were granted to the subcontractor after the finalisation of the ASIC design. The subcontractor had the responsibility to develop the ASIC according to the specifications, otherwise it was responsible to redesign the ASIC free of charge. The subcontractor kept the right of any specific publication with the prior approval of Crypto S.A.

The interfacing between company and subcontractor was performed basically by technical meetings and exchange of data using the electronic mail services.

11 BARRIERS

The barriers that prevented Crypto SA to adapt a new ASIC technology are presented below:

- **Knowledge barriers**
    - The main knowledge barrier was where to search for technology and cost information.
    - The second important barrier, since we have never dealt with ASIC design, was to understand the risks and contingency planning and it was also very hard to predict the investment, effort and time required to complete the development.
- **Technology barriers**
    - We had some bad experiences in the past with subcontractors who delivered out of schedule or never delivered at all. Also sometimes the specifications were not as agreed and we had no experience with contractual issues. Note that those barriers were not of the major importance.
- **Financial barriers**
    - We could not estimate to a good extend, the actual cost of transferring the new ASIC technology to our company and it was very difficult to bare expenses of high risk, while our position in the market was declining.

12 STEPS TAKEN TO OVERCOME THE BARRIERS AND ARRIVE AT AN IMPROVED PRODUCT

The barriers mentioned before were overcomed as follows:

- **Knowledge barriers**
    - The solution to the barrier was a suitable selection of a subcontractor, who had the required knowledge and who was willing to disseminate it to our company. INTRACOM seemed to be a very good choice, since it had an extensive ASIC design experience.
- **Technology barriers**

- The solution to this problem was to find a partner who was respectable and worth to trust and who had a good history of smooth cooperations in the past. Again INTRACOM seemed to be a suitable choice and from the first contacts with its personnel that would be involved in our project our expectations came true. No extra effort needed to impose time and cost targets as our collaboration was ideal at all segments.

- **Financial barriers**
  - This barrier was overcomed with the help of following parties:
    Our subcontractor helped us to estimate to a good extend the actual cost of transferring the new ASIC technology to our company.

    FUSE project gave the solution of financing a big part of the whole project, thus minimizing the overall risk a lot.

13 KNOWLEDGE AND EXPERIENCE AQUIRED

CRYPTO had an extensive experience in modem design using discrete components, but we lacked technical and managerial experience is ASIC design. The knowledge and experience acquired from this AE in combination with the initial targets, are in the following fields:

- We decided to introduce in our products a new technology that it would offer lower product cost and we learned how to investigate a new technology by the use of suitable subcontractors.
- Participating actively in the whole ASIC development procedure, we gained valuable knowledge and experience in all ASIC related issues, like specifications, design, testing and manufacturing process.
- We increased our knowledge in project planning and specification and formal report writing as from the start of the AE we had the project management.
- We increased our expertise in our company’s market position research and payback and ROI issues, afield that at past we had not given emphasis on.

CRYPTO achieved experience in mixed signal analogue/digital ASIC design methodology. The main objective for CRYPTO was the upgrading of already successful products, while at the same time a "new" design methodology was introduced in the company's environment. The new developed product will have better reliability with less cost, something that is vital for telecommunication field. Furthermore, the know-how transfer accomplished through the experiment will allow the development and the upgrading of other products using ASICs.

If in the future a project with similar difficulty will be undertaken by our company the only external supply will be on the ASIC CAD tools for design-entry, simulation and synthesis, as our company do not have such kind of tools.

14 LESSONS LEARNED

During this AE we gained valuable experience and we have learned some good lessons. I am sure that if we are engaged again in a new ASIC design, we could do much better, based in the experience of this first ASIC design, approach.

· The most important lesson that we have learned is to specify in the early stages what are the critical issues in a project. In those issues we must give particular attention and allow sufficient time for research, in order to find the most suitable solution. For our project a key issue proved to be the selection of the right ASIC technology and the technology capabilities as well. Since we underestimated the importance of this factor in the beginning and we based in future features that would be added in the selected technology, there was a significant delay in ASIC specifications and System specifications as well.

· Another very important lesson learned is that the selection of the appropriate subcontractor is an essential factor. In our case, in contrast with the past, we chose a subcontractor that corresponded to all stages that we needed its assistance. Although we had a delay in ASIC design phase, it was unavoidable as we had to move from Mentor Graphics AUTOLOGIC tool to SYNOPSYS synthesis tool. This transition had to be done as an incompatibility was observed between Mentor Graphics design libraries and silicon foundry (AMS) libraries. But on the other hand all this transaction with the synthesis tools and design libraries in which we participated, resulted to a better knowledge transfer about ASIC technology to our company. As it concerns timing delays, a whole 4-month delay in delivering the ASIC prototypes compared with the planned schedule, did not lead to any unpleasant implications for our project. It is better to have a more careful specification and design phase which will give you functional prototypes, than to go quickly to the fabrication stage, deliver the prototypes and then observe that many points would be better to be implemented in a different way and a new design and fabrication must be performed. The latter case will lead to much more extra effort, expenses and perhaps to bad results for the company market.

· The last but not least lesson learned, is that it is not difficult to achieve an improvement in a new technology, if you know the way. That means, even if you have no experience whatsoever in this new technology field, if you find the right partners, who have the right know-how, you can arrive in the desired result safely and in a time predictable manner.

15 RESULTING PRODUCT, ITS INDUSTRIALIZATION AND INTERNAL REPLICATION

In order to introduce this new technology to our existing modems we examined the industrialization costs. Based on quotation from AMS which was the silicon foundry that fabricated our ASIC prototypes via EUROPRACTICE services, we have calculated the new cost of the resulting DAA ASIC, which was found to be 30% more expensive than the previous discrete DAA. So we started to look for a vendor that would offer us more competitive prices. A ‘quotation cycle’ began and the desirable result came by THESYS and ATMEL silicon foundries. The NRE cost for the ASIC (i.e. the once-time cost to be paid by the user to the foundry for the development of dedicated masks for the production of the ASIC) is approximately 45 KECUs. An average cost reduction for the various Crypto’s modems is 16%. A detailed cost analysis for the company products that will be improved with the new DAA is given on the next tables.