FUSE Demonstrator Document
Application Experiment Number 23627
Wireless Image Transmission (WIT)
Company: DCT-Hellas
TTN: INTRACOM S.A.
January 1999

AE Abstract

DCT Hellas designs, produces and sells high speed telecommunication products, wireline modems and other wireless communication products. DCT Hellas also develops software for multimedia applications over ATM and non-guaranteed bandwidth LANs. The company has expertise in development of wireless and high speed baseband modems.

The objective of the application experiment was to design and prototype a JPEG codec ASIC and finally use it to speed the transfers of images with the VL-40 wireless modem. This device is capable of error-free wireless connections at 9600bps for a range of 10 to 20km, depending on the antenna type. It provides forward error detection and correction, Windows Plug and Play interface, standard AT commands, 800 programmable carrier frequencies and self-diagnostics.

The WIT-codec chip uses the baseline CCITT/ISO JPEG image compression algorithm, permitting high quality compression and decompression of YUV 4:2:2 color or 8-bit grayscale pictures. The chip is expected to be a low cost solution for a wide range of applications that require temporary storage or transmission of image data. Typical examples are digital cameras, color scanners, image processing, wireless or standard modems and teleconference applications.

The AE started in February 1997 and completed after 14 months, at the end of March 1998. The FUSE project provided 100 KECU of the AE’s cost and DCT Hellas contributed another 180 KECU for a total project cost of 280 KECU.

DCT Hellas plans to use the JPEG codec ASIC inside the VL40 modem and other future products, and expects an increase in sales due to that fact. The company already signed an agreement to sell the ASIC through Atmel, as a standard part and collect royalties by Atmel for the usage of the core. At the same time, DCT Hellas will also sell the core (as an IP building block) to its customers obtaining additional profits. Furthermore, the wireless modem with the JPEG chip will be marketed within 1Q99. It is estimated that the ROI is of the order of 12 for the three-year period of modem’s lifetime. The pay back period is estimated in 18 months maximum. DCT Hellas expects a minimum of 30% increase in the sales of the VL-40 wireless modem during the first year, due to the new feature of the JPEG compression module. Until the year 2001 we expect to receive around 1,8 MECUs for the ASIC as royalties by Atmel, around 225 KECUs from sales of the IP core and around 1,6 MECUs from sales of our modem.

Finally, another great benefit from this AE was that through the development of this ASIC, we got knowledge and experience that opens numerous possibilities for the company’s projects. The combination of cost and performance characteristics that ASIC technology gives, opens various replication possibilities for our future products. The experience we gained as a company and the successful outcome encourage us to continue. This AE can be a lesson for small companies like DCT-Hellas, which have expertise in conventional sectors of microelectronics and fear to move a step further.

1. Company name and address

DCT Hellas S.A.
Tel. (+30 1) 9409778
Fax: (+30 1) 9409778
2. Company size

DCT Hellas employs 25 people and 20 of them are engineers involved in microelectronics product development. The turnover for year 1997 was 400 KECUs, an increase 365% over FY96. The company has a research and development department, located in Patra, Greece, which is divided in two sectors:

- Hardware development sector, involved in designing, prototyping and testing new products and preparing them for volume production. This sector is specialized in high speed and density FPGA designs, mixed with discrete parts and hybrid modules, both in SMD and through-hole packages. The design team has developed skills in design using configurable logic, optical, low power and wireless technologies.
- Software development sector, specialized in the development of firmware, driver and application software for the company’s products. The same sector also develops generic communications and multimedia applications for Ethernet, ATM and IEEE 802.11 wireless networks.

The company also has a management sector and a market research department located in the company’s central offices, in Athens, Greece.

3. Company business description

DCT-Hellas is a small company founded by a group of engineers returned to Greece after long careers abroad, specifically in the US. The company has great experience in digital system design, data communication networks, and modem design. The hardware design, software development, system testing/packaging are performed in-house, while the PCB manufacturing and the assembly of board components are subcontracted.

The company’s line of products includes V34 and K56flex types of computer modems implemented either as ISA or PCI plug-in cards, independent external devices, or as compact PCMCIA type II cards. The company also expertise in 10/100Mbit Ethernet and ATM products and develops communication software for all the above. It should be mentioned that in less than a year of operation the company produced its first product which is the VL40 wireless modem. This long haul modem exhibits state of the art performance at an extremely competitive price. Also DCT-Hellas, is developing a wireless polling device for interactive meeting applications as well as applications concerned with the remote control of unattended coin-operated laundry mats and attended video-game arcades.

Finally the company offers consultant services (around 10% of turnover) related to modems installations /study for implementation of telecommunication networks/ user support.

Concerning company’s clients it should be mentioned that these are OEMs, service providers, and distributors of wireless modems (OEM agreements with Automatic Industries in Belgium and GMA International in U.S., negotiations currently done with distributors like Ingram for U.S. market). Specifically our VL40 modem is the modem of choice for Siemens-Greece (distributes in the Greek market) in applications requiring remote control of PLCs. DCT-Hellas has implemented a communication protocol in VL40 that allows direct interface of this modem with the PLCs sold by Siemens. Intracom S.A., is currently evaluating the radio module of the VL40 modem for a possible OEM agreement for this module with DCT-Hellas.
4. Company markets and competitive position at the start of the AE

DCT Hellas delivers products to the European and the International market. Although DCT Hellas is a new company in the wireless modems area, has strong market relations with other companies world wide, due to the low cost and the high quality of its products. As mentioned before our client list include OEMs, service providers, and distributors of wireless modems.

Given a fairly complete list of manufacturers with compatible product offering features, capabilities, and price, the DCT-Hellas modem compares extremely favorably with the list shown in the table below. The addition of the JPEG Chip of this project, will give the VL40 modem a capability that is unique for wireless image transmission and therefore will enhance the position of DCT-Hellas in the international market.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product</th>
<th>Range (m)</th>
<th>Data Rate (Kbps)</th>
<th>Freq. (MHz)</th>
<th>Number of Channels</th>
<th>Output Power (W)</th>
<th>Unit Price</th>
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<td>450-470</td>
<td>800</td>
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Table of competitive position of the VL40 wireless modem

Given the small size of the Greek market for wireless data communication products, DCT-Hellas targets most of its production for export primarily to the EC and the USA. It has signed an OEM agreement with Automatic Industries in Belgium for the Wireless Interactive Polling Device and will start producing the Coin Operated Laundry Remote Control system for this company. In the US, DCT-Hellas has signed an OEM agreement with GMA International to supply the VL40 modem to a number of hospitals and trauma centers, operating fleets of emergency response vehicles (ambulances). In this application VL40 is used in the ambulance to transmit patient data to the trauma center and there is demand for the capability to transmit images from auto-accident sites using portable VL40 units.

The total wireless market size is estimated to be 1 million narrow band units (non ISM like our modem) by 2001. DCT Hellas expects to enter dynamically the market of low cost wireless devices and gain by 2001 a share in the market of about 2% with around 20,000 units.

Currently, there is small interest both in the local and the international market for wireless communications products, due to pure quality and high prices of the relevant products. DCT Hellas has entered this market with a high performance, fully featured and well supported product, at a reasonable price and is willing to apply the same strategy to all its future products.

5. Product to be improved and its industrial sectors
The product to be modified is the VL-40 wireless modem (Prodcom code:3220), currently produced by DCT-Hellas. This high performance device is capable of performing half-duplex connections over a licensed UHF band, with speeds up to 14.4 Kbps at a distance of up to 10 km. The modem is built around the MC68HC11F1 microcontroller and contains on-board memory that allows user definition of various protocols for networking applications. The factory shipped units implement the q-persistent CSMA protocol and rely on forward error detection and correction capabilities to minimize the number of re-transmissions for error-free data communication.

The baseband modulation used is GMSK which allows the peak performance for the baseband unit to reach 40 Kbps. On board data memory is used for buffering and temporary storage. It supports Windows Plug and Play mechanisms and TAPI integration, AT command interface, error detection and automatic retransmission, programmable carrier frequencies, standard RS-232 port and self-diagnostics. It can also emulate a standard RS-232C serial connection and therefore it can be used with the unlimited assortment of software that has been written for the serial communication port, for practically every operating system.

The RF section of the modem contains a synthesized radio device that allows the user to select a transmission channel best suited for an application and compliant with local spectrum regulations. Eight hundred (800) channels are available to the user and the radio programming is performed using Windows based software shipped with the product.

The VL40 interfaces with any data processing device that features an RS232 interface. Its embedded firmware allows it to perform a point-to-point wireless connection or to emulate a wireline modem. In the latter case, VL40 operates with the standard AT commands used to control wireline modems. Windows based software (shipped with the unit) allows the user to easily operate VL40 in a number of modes and configure wireless wide area networks for a diverse range of applications. Possible utilization fields for this wireless modem include:

- Point to point and multi-point data connections
- Portable computer networks
- Remote measurements and control
- Voice plus data wireless links
6. Description of the technical product improvements

Although the prior product VL40 exhibits high performance for a long-range modem, its capability to transmit digital images is very limited by a number of issues characteristic to this specific application. The first issue of concern is simply data volume. Even for a small size color image the amount of data makes its real time transmission prohibitive, even with state-of-the-art wireless modems. For example, a 256 x 256 pixels color image (i.e., 8-bits/pixel) produces 524,288 bits, which will require over 40 seconds to be transmitted with VL40 (assuming that no retransmission is necessary). Given that most of the power dissipation occurs during data transmission, in this case VL40 will also have additional power requirements that make its use prohibitive for applications relying on a battery based power supply. Furthermore, VL40 has memory constraints and therefore requires bit-rate control for the image codec in order to treat each frame with a fixed size buffer, and also to deal with retransmission in case of errors detected in the received bit-stream.

So there was a need for powerful image compression to be used. The algorithm that was implemented into a chip was the CCITT/ISO Joint Photographic Experts Group (JPEG) digital image compression algorithm. Computations at very high rate during the encoding phase had to be performed by this chip. The quality of the compressed image under bit-rate control also depends on the dynamic update capability of the quantization tables.

The block mainly contains five functional modules, the Raster/Block Conversion Unit, the DCT/IDCT & Quantization Unit, the Huffman Unit, the Bit Stuffer/Unstuffer Unit and the High Level Controller. Apart from these units, the chip also has built-in Huffman and Quantization tables, which must be initialized before any compression/decompression operation can take place.

The high level controller has the overall control of the chip and it gives instructions for execution to each functional block in accordance to values set in internal registers. The controller makes sure that the various units are reading the right tables, and also controls the sequence in which the color components are processed by the implemented architecture.

The WIT IC design enables VL40 to transmit digital images in real time by providing a compression ratio of a minimal 20 to 1 (for perceptually lossless images) with bit-rate control and adaptive quantization table updates to achieve the best quality/transmission rate performance as selected by the user. The example image mentioned above can be transmitted in as low as 2 seconds. This is a major performance improvement with an additional impact on the power required to transmit the image.

In Fig. 6.2, the functional block diagram of the improved VL-40 design shows the connection scheme for the JPEG-chip. The specific architecture offers the desired set of functions and is compatible with the existing design.
Fig. 6.2 The JPEG-enhanced VL-40

However, this application alone was not flexible enough to serve for complete testing and measurements on the chip prototypes. In order to test the functionality of the JPEG codec under varying configurations and without having to pass through a costly redesign based on a VL-40 board, we designed a suitable evaluation PCB formed as a full-length ISA card.

Fig. 6.3 The JPEG evaluation board
This board utilizes a generic application of the new chip and transfers images between two host PCs, using wired or wireless connection. The wireless links we tested included the original VL-40 and several other products, both from in-house and OEM origin.

The test application software permits a selection of compression and decompression modules between the WIT-chip or a software implementation of the JPEG algorithm, in order to show the compliance of the hardware codec to the JPEG standard.

Similar IC’s available from other manufacturers already existed at the time we decided to develop this chip, but none of them satisfied the specifications we had set. Here are the available IC solutions that we examined before we actually decided to build the WIT-processor:

- CL550 or CL560 from C-Cube: JPEG-8-R2 compliant baseline codec, 350 stage pipeline, on-chip Huffman and quantizer tables, 44.1 MB/sec (for CL550-30), RGB, YUV, CMYK supported, real-time CCIR 601, 16/32-bit host interface, 144 pin PGA or QFP
- ZR36040 and ZR36050 from Zoran: bit-rate control, 7.4 MHz throughput, 20mW standby mode, 100-pin PQFP or 85-pin PGA
- L64745, L64765, L64735 from LSI Logic: 3 chip solution, dynamic Huffman table control, 27 MB/s on CCIR601 frames, 27 and 20 MHz versions

From the above cases, only C-Cube CL550 offered a one-chip solution with acceptable speed versus cost characteristics. The WIT processor delivers comparable compression throughput and our estimates for the cost of the chip when it reaches the market indicate a 25% lower price and a 40% smaller board space. We can see, for comparison purposes, that the WIT-codec has the following advantages over the competition:

- 30 MB/s throughput with 40 MHz clock
- Adaptable bit-rate control
- Low cost, single chip solution
- Low Voltage Operation; Both 5V and 3V is supported
- Small footprint; 100-pin QFP package, ideal for limited space designs

Due to a special agreement with Atmel, to produce and distribute the ASIC with its own brand, our NRE costs for the ASIC (complexity 42,000 gates) were minimized to 28 KECUs (the normal NRE was around 53 KECUs). This type of agreement, apart from giving an impulse early in the effort for producing the chip, also guarantees an extended lifetime for the product, since Atmel will automatically convert it to newer technologies whenever they become available.

The use of the WIT-chip makes possible a number of additional uses for the wireless modem, not possible to be achieved before, like:

- High speed image transmission modem systems
- Multimedia
- Color publishing and graphic arts
- Image storage, processing and retrieval
- Color printers, scanners and copiers
- Remote digital cameras (security monitoring, traffic control, Hospitals)

In particular, this new feature in our modem permits deployment in new market sectors involving multimedia presentations and remote monitoring, that the original VL-40 could never address. DCT-Hellas has developed the VL40 wireless modem primarily for the international market. It is the first developer in Greece that has produced a high performance modem that complies with international regulations for wireless data transmission and has obtained FCC approval for sale in the US. The sales of the original VL40 are 1,000 units/year and we anticipate an increase of about 20% in this volume with the added capability of efficient image transmission.
7. Choices and rationale for the selected technologies, tools and methodologies

The WIT-codec was designed to satisfy a frequent customer request; to improve the transmission times of image data through the VL40 narrow-band wireless modem. Before choosing the ASIC solution, several options were examined extensively. For example, modifications to the existing design had to be minimal and the incremental cost of the final product should be kept low, otherwise it would be better to design a new modem from the beginning. Also, the compression method had to be perceptionally lossless, a feature that only the JPEG image compression could offer. However, this algorithm required a lot of processing power, thus narrowing the variety of suitable choices to implement it.

The required characteristic for the wireless image transmission chip were:

- Use of standard CCITT/ISO JPEG compression
- Easy interfacing
- Low cost
- Small size and minimum external components
- Low power consumption
- High speed operation

Possible design solutions that met the above requirements are the following:

- A subsystem based around a standard, high speed microcontroller. This solution was not viable because the relevant cost would be very high, especially if we wanted the compression and decompression to occur in short time. Also, operation in near real time (e.g. 2 frames/sec or better) was not possible, even with the most powerful microcontrollers around.
- Using a specialized DSP processor. This should work, but the cost would go even higher and it was difficult to maintain the small area and low power requirements in this case.
- Use of an existing, specialized integrated circuit chipset from the few that were available in the market. This solution was rejected, because of the raised cost and the inability of the available solutions to completely match our specifications.
- Implementation of the algorithm using PLDs or FPGAs; This approach would require several high capacity and high speed parts and even then the expected throughput (in terms of time required to process an image) would not be acceptable. Also, the impact on the total cost was prohibitive for mass production and extra costs had to be added for programming the devices.
- Development of an ASIC. It was clearly the better solution for a JPEG processor, considering the complexity of the design and other requirements like clock speed, power consumption and cost for a large volume production.

Reaching to the decision to develop an ASIC, a choice had to be made also about the preferred ASIC technology, and the design methodology that we should follow. For the first part, we chose the ECLP07 digital CMOS process from Atmel/ES2. This is a 0.8 micron process and it delivers a good compromise between cost, speed and die area.

The Verilog Hardware Description Language (HDL) was used to develop the design. Verilog was chosen both for the ease of use and fast learning time and also because of our special relationship with Atmel/ES2 (business reasons as already mentioned in previous paragraphs), which provided us the latest standard cell libraries for this line of fabrication, royalty free. There are many advantages of designing using a hardware description language over the traditional schematic capture approach. Using HDL’s one can simulate the designs and can uncover functional errors that would otherwise be detected only when the actual hardware is implemented. In addition, the design is divided in steps in a straightforward manner, resulting in fast and efficient delivery of the results, even in the case of large and complex designs.
So in our case after the design was broken up into various modules and Verilog descriptions for all the modules were written, simulations were carried out on the behavioral Verilog models of each module to check for their functional correctness. When all modules were finished, a top level model consisting of all the individual submodules was constructed and simulated. After this stage was completed successfully, the next step of the design process was to convert the combined model of all modules into a gate level model. This conversion was carried out using the Autologic synthesis tools from the Mentor Graphics framework, which developed a gate level netlist using the available ASIC libraries. The synthesis and simulation steps were carried out at the subcontractor CEM/INTRACOM.

The synthesis tools optimized the design taking into consideration the area and speed requirements, the clock speed and the input/output delays. Both functional simulations and timing verifications were carried out on the back-annotated synthesized netlist of the design. The timing performance of the netlist was examined thoroughly to verify that the circuit meets its timing specifications. An extensive simulation with various setups and example files showed that the codec exhibits the expected behavior under all circumstances. Finally the chip design was sent for fabrication to Atmel as mentioned before and then the prototypes were tested in co-operation with our subcontractor using their digital ASIC tester.

8. Expertise and experience in microelectronics of the company and the staff allocated to the project

The engineering team in DCT-Hellas has a great experience in system design with off-the-shelf components, radio modem design and data communication firmware/software development. DCT-Hellas has also extensive expertise in data compression algorithms and architectures with particular emphasis on multimedia data compression. Although some of our employees had gained some experience in ASIC design earlier in their careers, this was not felt as a company know-how so as to be able to develop an ASIC as DCT-Hellas. Most of the experience of these individuals came from academic programs, which had nothing to do with real life applications, especially with items that concern management of the economic aspects. Also, the advances in this area are so fast and complicated that without a continuous involvement is impossible to keep up with them.

The specific project engaged a total of 10 of our engineers, most of them involved in a single or a couple of the individual tasks from the ones we describe in the following paragraph. The provision to divide the actual work in as many people as possible was aiming to distribute the transferred knowledge in a significant percentage of our employees and obtain the know-how at a company level.

The subcontractor, Intracom S.A. helped in replenishing our management skills with respect to the new technology and provided the training of our engineers in the various steps of the manufacturing process, especially during the synthesis and timing verification steps. Also the subcontractor’s CEM provided the necessary tools, development time and transport of know-how that was necessary for the completion of the design.

9. Workplan and rationale

The first step in carrying out this project was the construction of a phased workplan, which was based on the complexity of the design, the time to market restrictions and our experience with other similar projects. This workplan was followed exactly without any time delays as originally planned. The local TTN helped us in allocating the tasks in the areas that we hadn’t any experience, and we allowed some overhead as a safety precaution. A short description of each task along with the roles of DCT-Hellas and subcontractors (INTRACOM and ES2) is presented below:

<table>
<thead>
<tr>
<th>Task 1: Technical Management</th>
<th>Starting Date</th>
<th>Ending Date</th>
<th>Duration</th>
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9
The DCT-Hellas project leader worked closely with the local TTN to establish the technical management structure and the allocation of the necessary resources and subsequently managed the project according to its schedule and list of deliverables, assuring the smooth running of the project.

**Task 2: Training**

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The DCT-Hellas engineers received by the subcontractor (CEM/INTRACOM) seminars as well as hands-on training on ASIC design and testing methodologies and CAD tools used.

**Task 3: Design Specifications**

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DCT-Hellas defined the overall system’s functional, electrical and interface specifications and discussed these specifications with the subcontractor as link to task 3.2

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DCT-Hellas defined the functional, electrical, timing, and interface specification for the JPEG ASIC taking into account its system environment, availability of macrocells, and the targeted ES2 process. DCT-Hellas engineers were in close contacts and discussions with the subcontractor obtaining technical consulting wherever needed.

**Task 4: Design**

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The ASIC design was first performed by DCT-Hellas based on Verilog approach as discussed in previous sections and based on the macrocells available by ES2 for process ECLP07. The subcontractor CEM performed the synthesis and optimisation of the design and our engineers fully observed the whole procedure. Also a test vector set had been completed by the time of tape-out.

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The JPEG coprocessor board was designed by DCT-Hellas to incorporate the JPEG chip. Its Gerber files were send to a PCB manufacturer for producing prototype boards.

**Task 5: Fabrication**

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The JPEG ASIC was fabricated, parametrically tested, and packaged by ES2 using the targeted 0.8µm CMOS process.

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The PCB fabricated by a contract PCB manufacturer.

**Task 6: Testing**

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The ASIC packaged parts were tested by subcontractor (INTRACOM) with the test vector set produced during the design phase. All test results which were successfully documented and analyzed. The engineers of DCT-Hellas were fully observed the whole testing procedure under the guidance of subcontractor’s engineers.

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The coprocessor PCB including a fully functional JPEG chip were tested by DCT-Hellas.

**Task 7: System Integration and Demonstration**

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</tr>
</tbody>
</table>

The VL40 modem was integrated and demonstrated with benchmark images which were transmitted between two PCs using the JPEG coprocessor and a wireless connection. INTRACOM as subcontractor assisted the execution of that task by preparing the set-up for a real-life application for monitoring specific areas of buildings.

**Task 8: Dissemination/Awareness**

<table>
<thead>
<tr>
<th>Starting Date</th>
<th>Ending Date</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>13th month</td>
<td>14th month</td>
<td>2 months</td>
</tr>
</tbody>
</table>

DCT-Hellas prepared the appropriate information material for press releases, flyer, demonstrator document and workshops.
A comparison table with the planned and actual total costs (ECUs) for this project is presented below:

<table>
<thead>
<tr>
<th></th>
<th>Planned</th>
<th>Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Labour</td>
<td>41.000</td>
<td>45.993</td>
</tr>
<tr>
<td>Travel</td>
<td>3.000</td>
<td>892</td>
</tr>
<tr>
<td>Services</td>
<td>50.000</td>
<td>47.585</td>
</tr>
<tr>
<td>INTRACOM Subcontract</td>
<td>20.000</td>
<td>19.180</td>
</tr>
<tr>
<td>ASIC Fabrication cost</td>
<td>30.000</td>
<td>28.405</td>
</tr>
<tr>
<td>Consumables</td>
<td>3.000</td>
<td>2.092</td>
</tr>
<tr>
<td>Other</td>
<td>3.000</td>
<td>1.748</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100.000</strong></td>
<td><strong>98.310</strong></td>
</tr>
</tbody>
</table>

Furthermore a comparison table showing the company’s planned and actual effort and costs are presented below.

Table of effort and costs

<table>
<thead>
<tr>
<th>DCT-Hellas Effort and Costs</th>
<th>PLANNED</th>
<th>ACTUAL</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MAN DAYS</td>
<td>KECUs</td>
</tr>
<tr>
<td>Task1</td>
<td>50</td>
<td>4,98</td>
</tr>
<tr>
<td>Task2</td>
<td>40</td>
<td>4</td>
</tr>
<tr>
<td>Task3</td>
<td>42</td>
<td>4,2</td>
</tr>
<tr>
<td>Task4</td>
<td>170</td>
<td>17</td>
</tr>
<tr>
<td>Task6</td>
<td>50</td>
<td>5</td>
</tr>
<tr>
<td>Task7</td>
<td>30</td>
<td>3</td>
</tr>
<tr>
<td>Task8</td>
<td>30</td>
<td>3</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>412</td>
<td>41,2</td>
</tr>
</tbody>
</table>

Finally in the following chart we present the actual time duration (in months) per task which was exactly as the one which was initially planned.
DCT-Hellas signed a subcontracting agreement with INTRACOM within the framework of this FUSE project. Regarding IPR issues, it should be noticed that the whole system as well as ASIC design/specifications are owned by DCT-Hellas and no public announcement can be made by the subcontractor for technical issues without the written approval of the company. The choice of the particular subcontractor was done based on its technical expertise in the relevant field, excellent performance and time-scale accuracy in previous co-operations as well as close proximity from our premises.

INTRACOM S.A has established since 1993 the Centre of Microelectronics (CEM). Currently CEM is the national industrial VLSI design and Testing Centre in Greece with expertise in over 70 designs in various areas of applications like telecommunications, image processing, energy systems, medical applications, etc. It promotes R&D activities in the area of VLSI design for INTRACOM’s needs and simultaneously provides similar services to Small-Medium-Enterprises (SMEs). CEM’s main activities include System Design, VLSI Design, FPGA Design and migration to ASIC, Prototype Testing and System Production.

As described in the previous section, for the specific needs of this FUSE project, CEM provided us training on ASIC design and testing methodologies as well as on CAD tools that were used. It also contributed during the synthesis phase of the design, the ASIC prototype testing and the system evaluation setting up a real life application for monitoring specific areas of buildings.

Apart from learning the terms and guidelines that matched our requirements for this project we’ve been able to take a look, at the CEM, for other interesting possibilities of ASICs implementations. Furthermore, CEM’s training and consulting also helped us to obtain some knowledge about the various categories of design tools and methodologies, so that the task of selecting one in the future will be easier.

Another elevating action for the completion of this project was our preliminary agreement with Atmel/ES2, which provided us both lower manufacturing costs and technical assistance, i.e. with the latest edition of their standard cell libraries. Our agreement with Atmel/ES2 stated that we will have the Intellectual Property and the right to sell the JPEG core to future clients, regardless the fact that the chip will be sold as an Atmel part. We find this type of agreement as the most beneficial for us.

11. Barriers perceived by the company in the first use of the AE technology

Many small companies like DCT Hellas have skilled engineers and are willing to transfer some of their designs in custom integrated circuits, but afraid to make the appropriate steps to try out this
technology. The reasons are possibly similar to those in our case, detailed as the barriers that follow, listed by importance:

**Psychological Barriers**
- Fear to use a new, unknown technology
- The belief that there isn’t place for a small company in a field that traditionally ‘big’ companies operate.
- Bad experiences with other new technologies
- Fear of high risk, especially when there is a strict time-schedule and no other alternative solution in case of failure.

**Financial Barriers**
- High cost of development of ASIC prototypes
- Delayed return of investment (ROI) period, compared to of-the-self solutions

**Knowledge Barriers**
- No prior experience in conducting a feasibility study
- There is a wide range of ASIC manufacturing technologies and we didn’t know which to choose

**Technology Barriers**
- High complexity of the design that we want to transfer in ASIC
- No previous experience in choosing a physical package and defining its specifications

12. Steps taken to overcome the barriers and arrive at an improved product

Considering all the possible options for the JPEG codec, we examined the possibility of an ASIC development. The local TTN gave us useful information about this technology and we applied a feasibility study about the project in question, which showed that it was in our experience level and the financial margins were acceptable.

We continued to examine several aspects of this technology and we came to the decision that this is the best suited solution of our product. So we submitted a proposal to the EU to initiate a First User Application Experiment. By that time, our confidence in our ability to carry out this project was continuously being developed. The difficulty to overcome psychological and financial barriers we had earlier became insignificant after we realized that many of the successful cases we had seen started at a much lower technology level than the one we were at that time.

The interest given by Atmel/ES2 for the chip and the subsequent reduction in manufacturing costs for the prototypes composed an easy way to overcome the financial barriers and helped us to believe in the viability of our goal. Since DCT-Hellas signed an agreement with Atmel to sell the ASIC through them as a standard part, and collect royalties by Atmel for the usage of the core, financial barriers were completely collapsed.

We also realized that the risks involved were not greater than the ones we had to face with conventional design methods, especially if we expected to produce a high volume per year. In some respect, there is a lower risk approach in designing with ASICs, since the completion of a project can rely on the correctness of a single component, opposed to discrete designs with hundreds of parts from various sources. Many times in the past we had problems with devices that failed to work within their specifications, something that is difficult to happen when the chip is designed by us and we know exactly what we want it to do.

After approval of the application experiment, the company engineers that were assigned to the project completed an introductory course in the subcontractor’s CEM on Verilog HDL and ASIC development tools and methodologies. At the same time, a detailed study of all available options gave the preferred specifications for the chip. Based on these specifications, a software model of the JPEG codec was developed in C-language effectively, giving us a first look in the final hardware. This model was based in an almost already existing proprietary algorithm developed by
our engineers, that delivered fast operation and it was easier and efficient to implement. After successful testing of this model using a large number of image files was completed, we proceeded to the hardware design phase.

The end of the hardware design phase and the start of fabrication of the prototypes was the point where we overcame all the fears and barriers we had before, except perhaps from the fear of an unpredictable chip failure. Luckily, the first prototypes worked without any problems and the final testing on the demonstration board performed as expected. This produced greater confidence in the validity of these new skills we developed, and rewarded us in the best way. We are confident that we have developed a solid background in ASIC design methodology and we will continue to use this technology in the future.

13. Knowledge and experience acquired

The company gained better understanding of the advantages in using ASIC technology, such as cost effectiveness via increased levels of integration and development time-scales which allow faster entry into the market for the end product. The designed ASIC transitioned software models to silicon and provided a real application experiment with a core product for DCT-Hellas. Key benefits from applying this technology are:

- Compatibility with our existing tools and methodologies
- Lower cost and other savings (space, power consumption, etc.)
- The reusability of design blocks and processes
- Additional profits by distributing the chip to the market

The know-how transfer has been carried out to the company with various ways:

a) First, through our participation to our subcontractor’s (INTRACOM) theoretical as well as hands-on training we had the opportunity to fully observe, participate and contribute to the process of defining the specifications, designing, prototyping and testing an ASIC. Indeed the company’s engineers feel that they have obtained sufficient know-how, with the courses they received at the CEM, to continue and develop future products without further assistance.

b) Second, through our contacts with the local TTN we acquired valuable experience in project management related issues and specially in conducting and choosing sub-contractors and manufacturers, choosing technology options and preparing a time-schedule to develop a new design.

c) Third, through our collaboration with Atmel we were introduced to their specific technology library’s items and also got in contacts with foundries representatives and start talking about further business opportunities.

14. Lessons learned

This project introduced ASIC design capability, a new and exciting alternative to conventional PCB design with off-the-shelf components. It opened new possibilities for current and future products, considering the cost and space reductions, flexibility, short development time and performance enhancements of the new technology.

We found that developing an ASIC is very similar as designing with programmable logic, a practice that the company engineers had exercised many times in the past. The main difference is in the added task of choosing between different options of the technology, voltage rating, packaging and pinout of the chip. These parameters can’t change easily afterwards and usually they are constrained by various dependencies between them. As an example, a change to a different package (PQFP-100 instead of PLCC-96) was necessary, in order to add some more power supply pins.
Total 19% was subcontracted for training, consulting/support in ASIC design, evaluation and system integration/demonstration. Specifically the subcontractor percentage participation per task was: training 33%, design 18%, testing 27%, demonstrator 40%. Subcontractor selection is another point that have to be considered. Choosing a subcontractor with experience in the field of the technology gives a lot of solutions in the critical points of the design and offers assistance and guidance where they are required.

There are many advantages of designing using a hardware description language over the traditional schematic capture approach. A designer that uses HDL can simulate his designs and can uncover functional errors that would otherwise be detected only when the actual hardware is implemented. In addition, the design is divided in steps in a straightforward manner, resulting in fast and efficient delivery of the results, even in the case of large and complex designs.

Also, we saw that partnership with another firm, like Atmel in our case, can minimize both the costs and the risks for a project of this type, without affecting severally the expected profits. Specifically in our case we found that with a royalty for every chip sold by Atmel and with the IP for the core available for other possible clients, we will have greater profits, compared to our first thought, to produce the chip ourselves, due to the increased distribution possibilities.

15. Resulting product, its industrialization and internal replication

As a result of this AE, the company succeeded in both its technical and economic targets. Specifically DCT-Hellas obtained an improved competitive and international standards compatible modem (by developing the current digital ASIC as mentioned in the previous sections and obtaining the FCC approval for sale in the US) and also through the agreement we signed with Atmel, the chip will be sold by Atmel paying royalties to DCT-Hellas. Furthermore, it should be noted that Atmel has already printed a brochure with the AT76C101 and distributes it through international resellers. DCT Hellas also has the right to sell the evaluation board and the IP core through the same distribution channels. However the evaluation board will be offered free of charge to customers who are interested for the chips or systems. The total investment necessary for the new product is 280 KECUs taking into account our agreement with Atmel.

As a result of the successful completion of this experiment, DCT Hellas plans now to obtain the necessary tools and continue to develop ASICs independently. We expect to cover the initial cost for the new tools within the first 2-3 integrated circuits, which is much shorter than the normal payback period of every other design tool we used in the past. Specifically the company now examines all of its new designs under the ‘possible ASIC solution’ magnifying lens. Most immediate plans include the design for a wireless communication processor for PCMCIA-based applications, according to the newly released IEEE 802.11 standard wireless networking protocol and a low cost DSP processor. Based on the obtained results and the execution of this project, DCT has on-going discussions with Atmel/ES2 for an expanded relationship that will be mutually beneficial for the two companies.

Also, the core of the WIT-design is available as a megacell and it will provide for an easy enhancement for image transmission in many future ASICs, either ours or other’s under license. This core forms the basis of our library of customized solutions and we believe that we will continue to expand this library with new interesting modules and obtain another steady source of yearly earnings from it, from license rights only. Interest for the JPEG core was given by Fuji (Japan) and Motorola (Germany) and as a result the migration in the 0.35 micron technology is on the way.

16. Economic impact and improvement in competitive position

DCT-Hellas has developed the VL40 wireless modem targeting primarily to the international market. The same rule applies also to the majority of the company’s range of products, due to the small size of the local market. As a result of this, DCT-Hellas is the first developer in Greece that has produced a high performance modem that complies with international regulations for wireless data transmission and has obtained FCC approval for sale in the US.
Our business approach for the WIT design is twofold. On one hand, the JPEG chip, when added to the VL40 device will satisfy the emergency vehicle market needs as was requested by our distributor in the US. Using this new capability, the existing price can be increased by 28% and the minimum distribution volume in that market will be 500 units/year as agreed upon with one distributor so far, addressing this particular market. Our second approach to capitalizing on the WIT design is the agreement with Atmel, a well known semiconductor manufacturer to distribute it as a catalog part, namely AT76C101. DCT-Hellas will receive a royalty for every part sold by Atmel/ES2. Based on worldwide market projections for the JPEG Chip an initial production volume of 200,000 units is anticipated by Atmel/ES2.

A major strategic business outcome from this project however, is the development of the capability within DCT-Hellas for chip design. This capability will allow us to transit our data compression and data communications expertise to high value-added ICs which can be sold as parts through a business agreement with a manufacturer and also be used to enhance the performance of our modems. DCT-Hellas is positioning itself to be one of the most competitive suppliers in the wireless data modem market.

The redesign of VL-40 with the new JPEG processor was scheduled to start shortly after the end of the application experiment, with the anticipated product to be released at the 1st quarter of 1999.

![Fig. 16.1 Sales (units) for the VL40](image_url)

DCT Hellas expects a minimum of 30% increase in the sales of the VL-40 wireless modem for the first year, due to the new feature of the JPEG compression module. Until the year 2001 (forecasted production of 20,000 units of VL40) we expect to receive around 1,8 MECUs for the ASIC as royalties by Atmel, around 225 KECUs from sales of the IP core and around 1,6 MECUs from sales of our modem.

DCT-Hellas augmented the FUSE support program with its own investment to bring the improved VL40 modem to the marketplace. The total investment is presented in the following table:

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DCT-Hellas Participation</th>
<th>FUSE Participation</th>
<th>Total Investment</th>
</tr>
</thead>
<tbody>
<tr>
<td>JPEG ASIC Development and System Integration</td>
<td>100</td>
<td>100</td>
<td>200</td>
</tr>
<tr>
<td>Software Development of JPEG Codec</td>
<td>36</td>
<td></td>
<td></td>
</tr>
<tr>
<td>User Software for the Modem Interface</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>User Manuals</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Marketing Activities for Product Launch</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>TOTALS (kECUs)</strong></td>
<td><strong>180</strong></td>
<td><strong>100</strong></td>
<td><strong>280</strong></td>
</tr>
</tbody>
</table>

![Fig. 16.2 Total investment costs](image_url)

The FUSE contribution in this project was essential, because without it we would have a very difficult task in raising that amount of money, starting from ground zero.

DCT expects to recover the costs in about 18months, after the end of the FUSE project. This period may become shorter, as sales will probably grow to higher levels and new projects are to be
scheduled and carried on, based on the JPEG core. The ROI is of the order of 12 over the expected 3-year life time period of the product. The following table shows an estimation for the company’s revenue from this design.

<table>
<thead>
<tr>
<th>Year</th>
<th>1998</th>
<th>1999</th>
<th>2000</th>
<th>2001</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue (KECU)</td>
<td>35</td>
<td>120</td>
<td>700</td>
<td>1600</td>
</tr>
</tbody>
</table>

*Fig. 16.3 Company’s revenue*

These figures are based mainly on the forecast sales for the IP core, VL-40 modems and royalties from the chip sold by Atmel. Also, possible variations of the same design, based on the JPEG core, which we cannot predict now, will add to this revenue.

To conclude, the addition of the JPEG chip will give to the VL40 device a capability that is unique for wireless modems and will enhance the position of DCT-Hellas in the international market. The ability to develop custom integrated circuits will also provide a strong advantage for the company when negotiate with clients for developing new products.

**17. Target audience for dissemination throughout Europe**

The distributed informational material is designed in a way to provide a comprehensive guide for everyone interested about the benefits of introducing ASIC technology, especially for small companies who, like DCT-Hellas expertise in conventional sectors of microelectronics and fear to move a step further. In particular, we find that the results of this AE will provide a useful guide for companies with similar management style, i.e. run mainly by engineers and specializing in the following sectors (listed with the corresponding PRODCOM codes at the right)

- Computers and Other Information Processing Equipment (3002)
- Television and Radio Receivers, Sound or Video Recording (3230)
- Medical & Surgical Equipment and Orthopedic Appliances (3310)
- Instruments & Appliances for measuring, checking, testing etc (3320)
- Games and Toys (3650)

The technical and marketing literature distributed will acknowledge the EC contribution to this project. The key points that we want more specifically to outline are:

- Information about the First Users Action
- Reports on the technical benefits from this application experiment in terms of overall system performance, reduction in size/volume/power dissipation, speed response, etc.
- Economic benefits in terms of high added value for the system, product competitiveness market share (domestic and international), and sales volume.
- Guidelines for transferring designs to ASICs.