



Title:	Applying FPGA Technology to improve a range of Data Acquisition and Control Products
Business Description:	BEDE Technology Ltd is an electronics design and manufacturing company which has three main product ranges: <ul style="list-style-type: none">- Data Acquisition and Control Cards for PCs- Customised Test Equipment- Bespoke Factory Automation Systems
Industry Sector:	Industrial Process Control Systems, Telecoms and Instrumentation
Electronic Technology:	New: FPGA Previous: Analogue and Digital PCBs

ABSTRACT

BEDE Technology Ltd is a small U.K. manufacturer of Data Acquisition & Control Cards for PC compatible computers. These products are printed circuit boards which plug into the ISA bus of PC compatibles and are used to interface computers with external devices such as sensors and actuators. The current range of PC cards is widely used in process control and monitoring systems.

This experiment, with a budget of 40kECUs and seven months duration (September 1996-March 1997), was to apply FPGA technology and VHDL design techniques to improve the current range of PC based data acquisition cards. A prototype multifunction card was successfully designed, manufactured and tested. This prototype consisted of an ISA bus PCB with a FPGA to implement the digital logic and an add-on daughter board to perform the analogue interface.

A top-down VHDL design methodology was adopted throughout as this gave the greatest design flexibility, provided vendor independence and the ability to migrate to ASIC technology if required at a later date. It also reduced the development time and costs with a payback secured within 10 months of the project completion and ROI expected to be minimum of 5-fold.

Benefits

- Training of two design engineers in the use of VHDL and CAD tools for FPGA design, allowed BEDE to acquire sufficient in-house expertise to apply FPGA technology and VHDL techniques to develop new products.
- A complete design-flow manual was produced as a reference manual for new product designs. This manual can be purchased from the Satellite TTN Centre at the University of Northumbria at Newcastle, England.
- The prototype demonstrated the following improvements:
 - Reduced development cycle for new designs
 - Increased functionality
 - Cost-effective custom designs for small volume and reduced manufacturing costs.
- Following the experiment, BEDE Technology has manufactured two additional FPGA based products during autumn/winter 1997/98. As a result of this, a new niche market for customised PC cards has been established and additional customer based products emerging.
- Increased sales are now helping BEDE Technology to expand their business.

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Company Information

1. Name and Address

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2. Company Size

The company has 12 employees of which 2 are electronic engineers. Mr. R. M. Gott and Mr. J. W. Mulholland were the two electronic engineers involved in the Application Experiment. They are both qualified to University standard and have analogue and digital system level design, and PCB design and test experience. However, they did not have experience in electronic design at the component level.

Mr. J.W. Mulholland, the Senior Electronic Engineer has over 10 years experience designing analogue and microcontroller products. Dr. P. J. Mulholland, the Managing Director of BEDE Technology Ltd supervised the project. His expertise is in microprocessor/microcontroller based control systems and industrial processors.

3. Company Business Description

BEDE Technology Ltd was established in 1989 as a design and manufacturing electronic company. The company has experience of designing and manufacturing data acquisition and control equipment, amounting to 70 different PC card designs, using conventional Digital and Analogue ICs with turnover of 800KECU/annum. The company products addressed typical applications such as:

- Machine control
- Instrument interfacing
- Industrial Process Control
- Automated Test Equipment (ATE)
- Data Logging

These applications are marketed under three main product ranges:

- Data Acquisition and Control Cards for PCs
- Customised Test Equipment
- Bespoke Factory Automation Systems

Before the FUSE experiment the company did not have any experience or expertise in using FPGA devices or the VHDL design Language. The staff had a limited knowledge of advanced digital design techniques and no exposure to sophisticated CAD tools.

4. Company Markets and Competitive Position at the Start of FUSE

4.1 Company Markets

The market for BEDE Technology's products is currently 95% UK based with the remaining 5% sales to Ireland, Germany and the U.S.A. This represented a 1-1.7% of the 1997/98 UK market share. The UK data-acquisition cards market is approximately a quarter of the European market.

The company's customers include GEC, EDS, Rolls Royce, DRA, BNFL, IBM, Philips, Samsung and a wide range of SMEs. BEDE PC data acquisition cards is marketed and sold for the following applications:

Applications	Percentage of Bede Cards Sold
Industrial Process Control Systems	25%
Office Machinery and Computers	6%
Telecom & Networking Products	17%
Machinery, electrical and Optical Equipment	12%
Medical, Precision and Optical Instrument	12%
Automotive and Aerospace	13%
Test & Measurement	15%

The market for the company's product is expected to grow annually by at least 10% due to the increased applications for desktop and industrial PCs.

4.2 Competitive Position

The main customers for BEDE cards are OEMs and military users who have specific requirements which are not currently available on a single PC card. Prior to the Application Experiment BEDE's market for the existing technology increased from 0.7% in 1995/96 to 1.7% in 1996/97. This trend reversed during 1997 due to the company's technology limitation, market demands, and competition. BEDE's catalogue of more than 70 PC cards still did not cover market demands and therefore more new cards were required. The Company's business, with the available limited technology, was restricted, as the development cycle of new cards was around 3-4 months, this was unacceptable to clients, and resulted in loss of orders. BEDE's overheads grew to a level that started to affect the company's profits and its economic feasibility.

Figure 1 shows 1995/98 actual and forecasted sales to 1999 of BEDE's existing products.

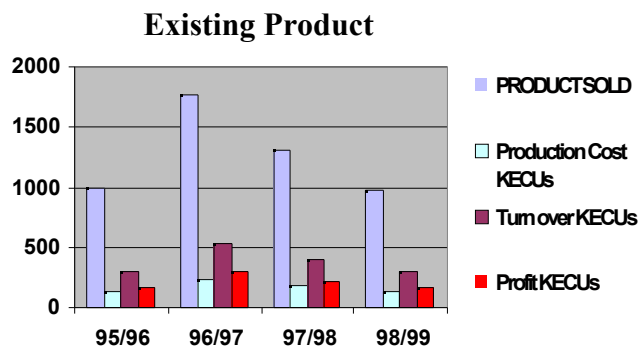


Figure 1

The Product to be Improved

5. Existing Product

5.1 Product Code & Signature

PRODCOM Code 3002
Signature 3 1420 500 0440 2 3002 1 30 UK

5.2 Description of Existing Product

All BEDE cards use the Industry Standard Architecture (ISA) Bus for PCs. The existing product is a range of data acquisition and control cards which plug into the ISA bus slots in PC compatible computers. These cards are used to interface the computer with sensors & actuators and are typically used in process control & monitoring systems. Some of the functions are:

- Measure analogue inputs (thermocouples, strain-gauges etc.)
- Detect digital inputs (micro-switches, proximity switches etc.)
- Control analogue outputs (motor control, signal generation etc.)
- Control digital outputs (alarms, indicators etc.)
- Counting/timing input or output events

A typical card design is shown in Figure 3. All BEDE cards were designed using off-the-shelf analogue and digital components and each of the cards is tailored to client or market demands. The need for added functionality requires more components and hence more card space. Most of BEDE's cards are already densely populated with no possible room for expansion. This is seen by BEDE as a barrier and affects their dynamic response to the needs of the PC control cards market.

The other disadvantages of the current products are:

- Lengthy development cycle (typically 3/4 months for a new PC card)
- Limited functionality (only a limited number of discrete ICs can be squeezed onto a PC card)
- Fixed designs (cannot be easily customised)
- High manufacturing costs (large number of ICs and large PCB makes manufacturing and assembly more costly)



Figure 4

A feasibility study was carried out to resolve the design and production problems and to help BEDE to improve their productivity. The results identified programmable microchip technologies as the best alternative to BEDE's existing technology. It also recommended the change of the design methodology to reduce the design time, cost and the number of required boards. This led to BEDE's application for funding under the FUSE programme.

6. Description of Product Improvements

The objective of the application experiment was to apply FPGA technology and VHDL design techniques to improve the existing range of PC based data acquisition cards. The designed card was a multifunction data card suitable for a number of applications such as:

- Industrial process and control
- Medical applications
- Underwater remotely controlled vehicles
- Environmental research for the National River Authority water sampling and data collection
- Environmental chambers control of dangerous gases
- Military applications

The experiment objective was met with a total funding of 40KECU and within a seven months period. A prototype multifunction PC card (Figure 4) was successfully designed, manufactured and tested. This prototype consisted of a PCB, which plugged into the ISA bus using an FPGA to implement the digital logic and an add-on daughter board to perform the analogue interface. The successful completion of the prototype product demonstrated to BEDE how FPGA technology and VHDL techniques could be used to improve the current range of PC cards.

6.1 New Product Specification

A functional block diagram of the prototype multifunction PC card is shown in Figure 5. The prototype card has the following functional specifications:

- Eight differential 12-bit analogue inputs
- Two 12-bit analogue outputs
- Four methods of sampled data transfer: software controlled, interrupts, DMA and FIFO
- FIFO sampled data memory (size limited by FPGA)
- Sampled data throughput > 100khz
- Software programmable input and output analogue voltage ranges
- On-board Counter/timer for pacer clock and general use
- 16-bit programmable digital input
- 16-bit programmable digital output

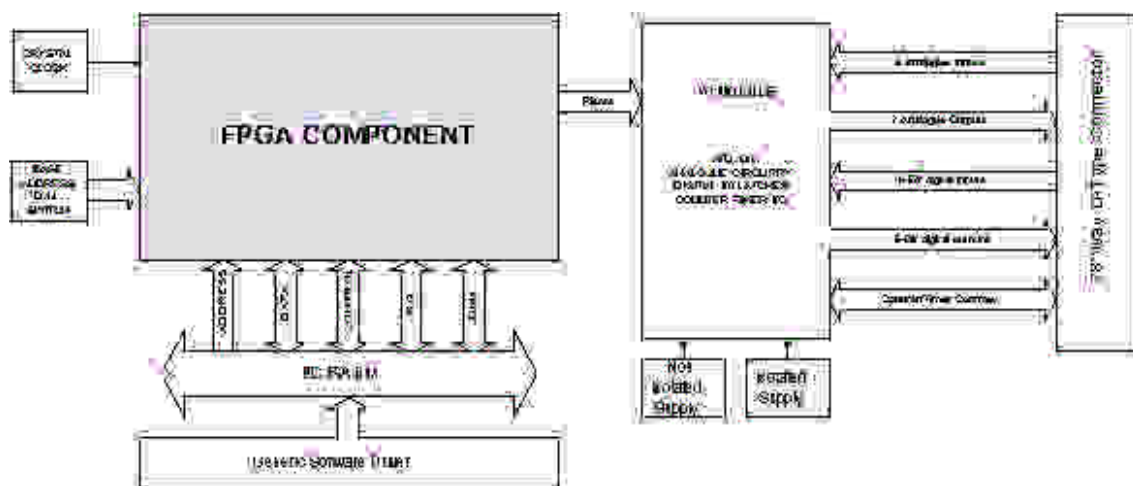
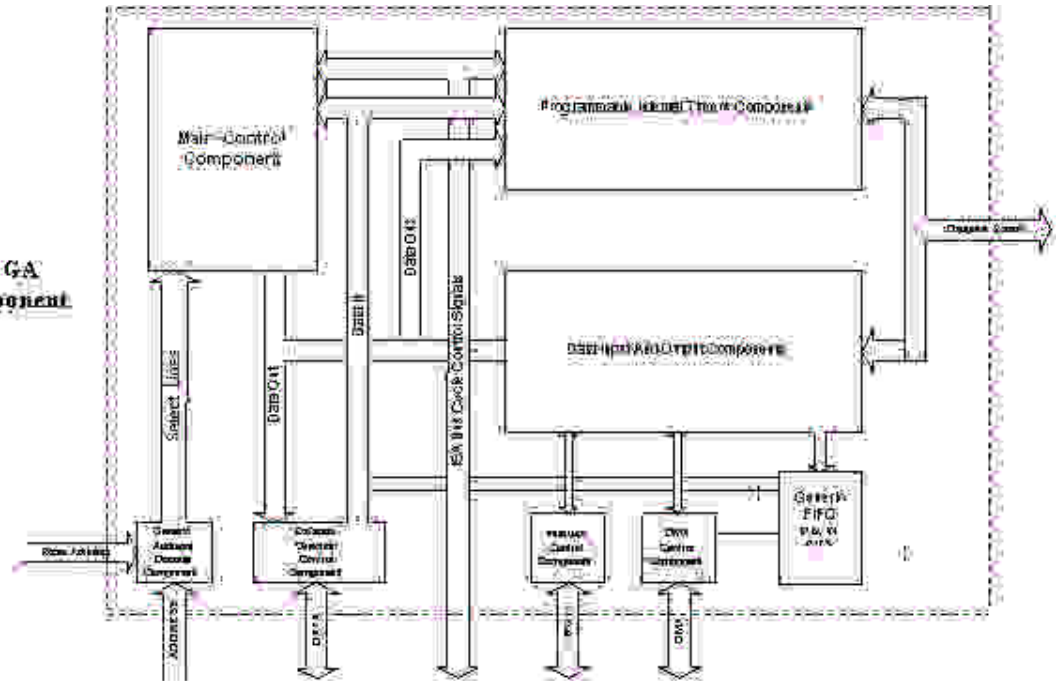


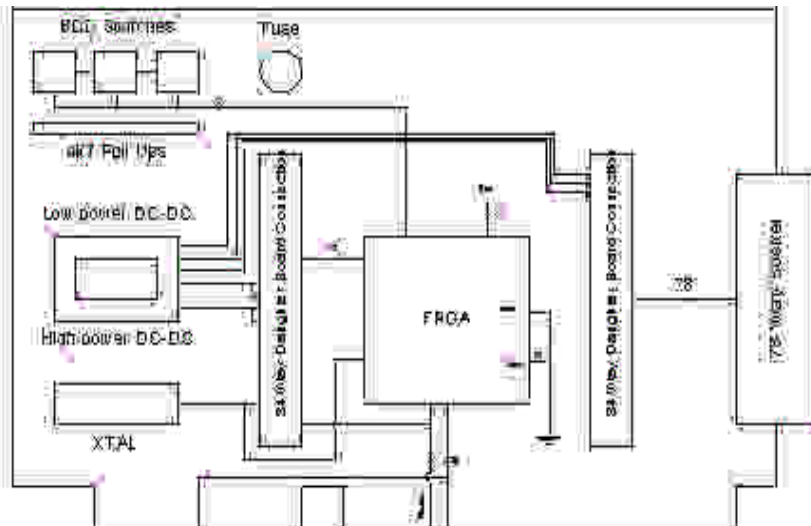
Figure 5: PROTOTYPE CARD BLOCK DIAGRAM

Figure 6: FPGA Component



All of the digital blocks (Figure 6) were implemented inside the FPGA using VHDL modelling and synthesis techniques, whilst the analogue components were mounted on an add-on daughter board. The final prototype board and circuit layout are shown in Figures 4 and 7, respectively.

Figure 7: Prototype PC Card Layout



6.2 Product Improvements

The use of FPGA technology allowed the encapsulation of all of the digital circuits of the existing product on to a single IC. The selected Actel device allowed the expansion and successful implementation of the specification listed in the previous section. The enhancement of the PC card capability is a fully efficient ISA bus architecture capable of handling a wide range of data acquisition. Using a single solution card enabled BEDE to have a dynamic response to the demands of the PC control card consumer market.

The prototype multifunction card demonstrated the following improvements over the existing product range;

- reduced development cycle for new designs
- increased functionality
- cost-effective custom designs for small volumes
- reduced component count (compare Figures 3 and 4) and manufacturing costs

Choices and Experiment Decisions

7. Technology, Design Methodology and CAD Choices

7.1 Technology Choices

Prior to the application phase, BEDE engineers considered the following technology options:

- **Discrete technology (including microprocessor/microcontroller):** This technology is commonly used by BEDE engineers and therefore does not represent any risk. The implementation of a universal Data Acquisition PC card with increased functionality is seen to be the only solution. The discrete technology is an easy option, however it requires a larger PCB due to the expected increase in component count. BEDE management rejected this option due to the expected increase in the design and test time, reduced product reliability, MTBF (Mean Time Between Failure), and an exponential increase in cost.
- **ASIC technology:** This technology would allow the incorporation of both the digital and analogue circuits into a single component and hence would allow an increase in functionality with a reduction in PCB size. Programmability is essential to meet users' change of specifications and would allow BEDE a flexible and low cost future upgrade of the product. This is possible using ASIC with an embedded microcontroller though at a substantial increase of cost and complexity and at a reduced yield. This represented a high risk to BEDE, whose production volumes, at less than 10k units per annum, did not justify the ASICs costs, and therefore the technology was rejected.
- **FPGA Technology:** The reduction of the product's PCB size and manufacturing costs were the main project concern. An FPGA implementation was chosen because of the current relatively low production volumes and the fact that the digital hardware needs to be programmable to produce new PC cards and customised designs with fast turn around of new products.

After considering the available FPGA technologies it was decided that Actel antifuse devices would be most suitable for this particular application. The reasons for choosing Actel were as follows:

- **Highly predictable time delays-**
Actel's segmented routing and low impedance antifuses produce highly predictable, short routing delays (90% of all routes use only 2 antifuses with a maximum of 4 antifuses for any interconnect path). These predictable time delays produce very accurate simulations which is extremely important when using top-down VHDL techniques and one-time programmable devices from Actel.
- **Cost Effective Solution**
The antifuse requires much less space than SRAM based FPGA cells, therefore the chip die size is smaller and the devices are cheaper to produce. Also, unlike SRAM devices, there is no need for configuration devices (e.g. EEPROM etc.) to initialise the FPGA. These extra chips increase costs and waste valuable PCB space. For the same number of gates Actel FPGAs were found to be significantly cheaper overall compared to their competitors.
- **Reliable antifuse technology -**
The antifuse is a programmed hard contact between layers inside the chip and is therefore extremely reliable. Actel FPGAs do not require any configuration procedure, are fully functional at power-up and are more resilient to power fluctuations and radiation effects than SRAM based FPGAs. These factors are extremely important for many of the critical control and monitoring applications of PC products.
- **Flexible pin-out definition -**
Due to the small antifuse size, Actel FPGAs provide more routing resources on the chip than the equivalent SRAM device. Therefore, Actel FPGAs are more efficient at routing and are typically able to use 90-100% of all logic modules on the chip. Another extremely important effect of the efficient routing is that it allows more flexible pin-out definitions. Therefore, the PCB and FPGA can be designed at the same time and any changes in PCB layout can usually be accommodated by the FPGA. This is the approach adopted by BEDE to speed up product time-to-market.

- **High quality, easy-to-use Actel Software tools -**
Actel's Designer Series software tools were used to take in the EDIF Netlist file from the synthesis tool and place, route and program the FPGA. These tools are efficient, easy-to-use and integrated well with synthesis and simulation tools.
- **PCI support and Core HDL models available -**
Actel have chips which support the PCI bus standard and have PCI bus models and other VHDL models available in their Core HDL libraries.

The foreseen limitations of antifuse technologies, which can be resolved by closely following the design rules and guidelines of the technology suppliers, are:

- They are one time programmable (OTP) devices, therefore the design must be correct first time. New products must go through a number of iterations and hence wastage of devices can increase development cost. Designers iteration between design and simulation to satisfy the design correctness before programming would reduce the cost of production.
- The programming time for antifuse device is 5-10 minutes. This will allow programming of a small number of devices per working day. In-system programming (ISP) of a number of systems in parallel would however increase the throughput.
- Antifuse suffers from parasitic effects which could affect the production performance. This could be resolved by keeping the number of the antifuse connections blown in series to a minimum and also by using well structured routing techniques.
- Long term reliability is an important issue in antifuse technology since they tend to suffer from many failure mechanisms, such as electromigration and change of properties, with time. This can be resolved by complying with suppliers' recommended procedures and design rules.
- It is a purely digital solution and it can not currently deal with analogue circuits.

7.2 Design Methodology and CAD Choice

A top-down VHDL design methodology was adopted throughout as this gave the greatest design flexibility, provided vendor independence and the ability to migrate to ASIC technology if required at a later date.

After evaluating a number of VHDL CAD tools, the Synplify synthesis tool, V-System simulator and Actel's DESIGNER SERIES placement, routing & programming tools were chosen.

Synplify was chosen because of its speed of synthesis and its compatibility with other CAD tools. In tests it proved to be at least 10 times faster than its main competitor and produced more efficient netlists. The package was also cheaper and supported all the popular FPGA vendors.

The V-System simulator is an industrial standard package, which has been available for many years and supports the IEEE 87 & standards for VHDL. It was chosen because of its reputation, reliability, compatibility and the fact that it is the most flexible standalone VHDL simulator available for the price. The simulator is the most important CAD tool used in a top-down VHDL design because it is the tool which verifies whether the design will work or not.

Actel's DESIGNER SERIES software was used to place, route & program the Actel FPGAs. The software is efficient, easy-to-use and integrated well with Synplify and V-System.

Using these software tools, a design-flow procedure was established for BEDE's FPGA designs as shown in Figure 8 and a detailed design-flow manual was written as a reference document for future designs. Copies of the design-flow manual can be purchased from the University of Northumbria at Newcastle (North-East Satellite Centre to Bolton TTN).

The prototype multifunction card PCB was designed using ORCAD schematic capture and layout CAD tools. These were chosen because of their technical specifications, widespread popularity throughout industry and compatibility with VHDL CAD tools. The PCB was actually designed at the same time as the FPGA and the final pin-outs from ORCAD were input to the Actel Designer series software for placement, routing and programming of the FPGA.

The FPGA and entire multifunction PC card were simulated using V-System. A library of behavioural models were written for all of the component parts of the FPGA (counter/timers, I/O ports, address decode, DMA control etc.) and these models were combined into a single structural model of the FPGA. A functional description was also written to model the ISA bus,

input stimulus expected results and daughter board. A testbench was then written to combine the FPGA component and ISA bus functional model and simulate the behaviour of the entire multifunction PC card.

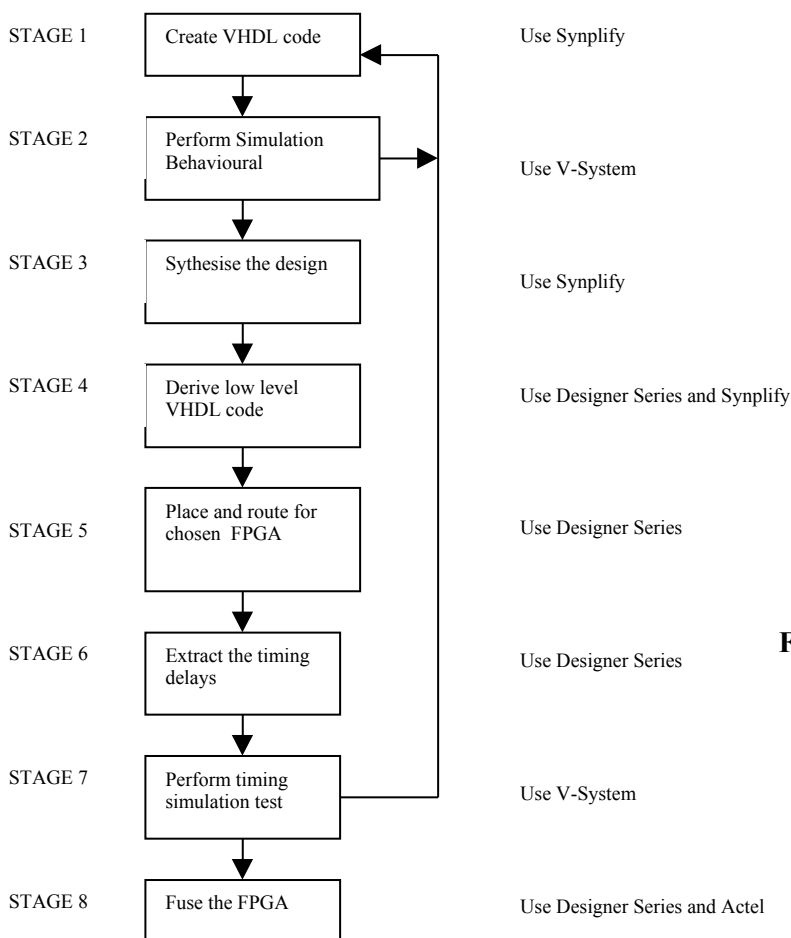


Figure 8: Design Flow Diagram

7.2.1 VHDL model and simulation hierarchy of the testbench card

The testbench model is partitioned into two main sections: the multifunction VHDL structural model and the ISA bus functional model.

⇒ The Multifunction VHDL Structural Model consists of:

- Data Direction VHDL Behavioural Model
- FIFO Behavioural VHDL Model
- Data In & Out Behavioural Model
- PIT Behavioural VHDL Model
- DMA Controller VHDL Behavioural Model
- IRQ Controller VHDL Behavioural Model
- Address Decoder VHDL Behavioural Model
- "GLUE" VHDL Behavioural Model

⇒ The ISA Bus Functional Model consists of:

- XTAL behaviour
- ISA Bus VHDL Structural Model
 - ISA Read VHDL Behavioural Model
 - ISA Write VHDL Behavioural Model
 - ISA DMA VHDL Behavioural Model
 - ISA IRQ VHDL Behavioural Model
- Stimulus Control
 - VHDL File Handler and Parser
 - File of Test Instructions
- Auto Correlation

- VHDL File Handler and Parser
 - Expected Results
- Daughter Board VHDL Model
 - A/D Behavioural Model
 - D/A Behavioural Model
 - 78 Way Socket Structural Model
 - VHDL File Handler and Parser
 - Input Stimulus File
 - Expected Results
 - "GLUE" Behavioural VHDL Model

BEDE staff successfully implemented out all of the above tasks.

7.2.2 Simulation and CAD

Simulation was performed before place & route and after place & route using the VITAL timing libraries. In practice the simulation is performed at the highest level as a set of instructions written into a text file using a word-processor. This text file consists of simple instructions which simulate the operation of the PC when talking to any type of plug-in card on the ISA bus (e.g. READ, WRITE, DMA, IRQ, RESET, etc.). These instructions are executed sequentially under V-System and the results are displayed in any type of V-System window. This high-level simulation approach allows hardware test engineers who have no knowledge of VHDL, to evaluate and verify a new PC card design before even a prototype has been manufactured. Therefore, a number of BEDE engineers will be able to use this simulation system to increase productivity, reduce the need for repeated prototyping, speed-up the time to market and ultimately reduce development time and cost per card.

The VHDL behavioural models of the ISA bus and component parts (counter/timers, I/O chips etc.) will be of particular interest to many other companies developing ISA bus products. BEDE are therefore considering expanding these models to include serial communications and networking components for ISA and PCI bus and licensing them to other companies via the Internet. This is an unexpected spin-off from the FUSE experiment, which may be of financial benefit in the future.

8. Expertise and Experience

BEDE's staff are experts in designing and testing analogue and digital discrete circuits and programming microprocessor/microcontroller using assembler and C. All of BEDE's PC cards were designed in-house including PCB layout design and full testing of the PC cards.

Prior to the FUSE experiment BEDE did not have any knowledge of high level digital design or modelling using VHDL. The company was aware of the FPGA technology but was unaware of its suitability to its products.

Work Programme

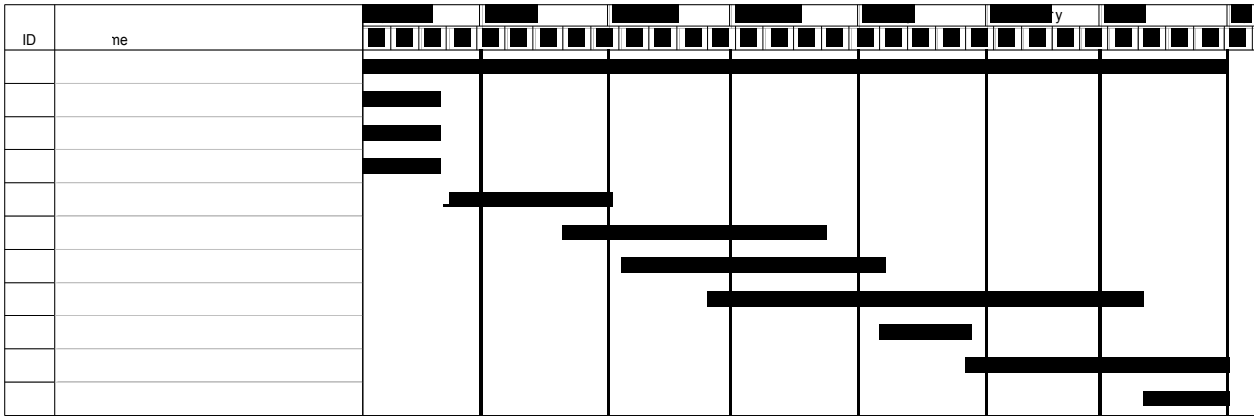
9. Workplan

9.1 Comparison of Planned and Actual Person-days

The following workload indicates the schedule planned (with the help of the TTN) in the original Technical Annex and Approved by the FUSE Consortium before the start of the Application Experiment.

		Planned	PERSON DAYS	
			BEDE	Actual Subcontractor
Management	Project Management	3	3	
	Reporting	14	18	
	Dissemination	3	3	
	Total	20 DAYS	<u>24 days</u>	<u>0 days</u>
Specification	Functional	5	5	
	System	4	4	
	Technical	5	5	
	Test	4	4	
	Total	<u>18 days</u>	<u>18 days</u>	<u>0 days</u>
Training	Management	0.5	0.5	0.5
	Specification	0.5	0.5	0.5
	CAD	6	6	3
	Design	4	4	2
	Evaluation	2	2	1
	Total	<u>13 days</u>	<u>13 days</u>	<u>7 days</u>
Design	PC Card	15	12	
	PCB	10	10	
	FPGA tools	5	5	0.5
	VHDL model	50	60	7.5
	VHDL Test bench	15	20	1
	Place and Route	5	5	
	Test set up	10	10	
	Total	<u>110 days</u>	<u>122 days</u>	<u>9 days</u>
Evaluation	Prototype production	15	15	10
	Test set-up	15	15	
	Test FPGA	10	12	
	Test PC Card	15	15	
	Environmental test	5	5	
	Total	<u>60 days</u>	<u>62 days</u>	<u>10 days</u>
TOTAL EFFORT		<u>Planned</u>	<u>Actual</u>	
		221 days	265 days	
			239 days	
			26 days	

The above workplan is shown in the following Gantt-Chart.



Deviation from the original planned schedule was in the reporting and the preparation of the demonstrator document, which consumed an additional 4 days. The design phase, especially the VHDL modelling, consumed an extra 10 days and the test and redesign consumed an extra 5 days.

Since the project was so important to company development, BEDE decided to fund the extra person-days from their own budget.

The project was divided into a number of work-packages in order to apportion the correct person-days to each task. The details of each work-package are highlighted below: -

Management

A detailed plan for the experiment was drawn up in order to manage BEDE's technological staff, write reports and organise dissemination of the experiences acquired to benefit the company and other organisation. During the course of the application experiment from September 1996 to April 1997, seven monthly technical and costs reports were completed and approved by the company Managing Director and the TTN Officer. The TTN kept regular visits and telephone contacts with BEDE during the experiment period and beyond. This allowed BEDE to meet the set deliverables on time. Regular monitoring meetings helped BEDE to focus on the experiment and achieve more than what was originally planned. A TTN dissemination seminar was delivered in July 1997 at a venue in Sunderland, England.

Specification

The objective was to generate a functional, system, technical, and test specification for the prototype. The basic functional specifications of the multifunction PC card are given in section 6.1 of this document. The specification of the experiment was developed by the project manager and two engineers and required 18 person days of work during month 1. The company discussed the specifications with the TTN Officer before their final approval.

Training

The University of Northumbria at Newcastle (UNN) provided training in FPGA project management, FPGA design, and the use of VHDL CAD tools. This included how to select the appropriate vendor technology and design methodology for the application. The training required 13-person days work during months 1 - 3 and was accomplished by 3 days formal training followed by 4 days practical hands-on training. BEDE staff gained more knowledge through the assistance given by staff from the UNN during the design phase of the experiment.

Design

The aims were twofold; firstly, to design the multifunction PC Card, PCB and the associated analogue circuitry and secondly, to select the FPGA technology and vendor. This FPGA component was then modelled in VHDL, synthesised, simulated and from this a test bench was produced. Finally, the FPGA design was placed routed and programmed. The total allotted time was half the total experiment duration due to the complexity of the modelling and required interfaces. Seven tasks were carried out in producing the experimental prototype.

- A system level design of the multifunction PC card took 12 days in month 2.
- Purchase of V-System, ACTEL FPGA tool and Synplify. ORCAD was also purchased for schematic capture and to design the layout of the PC card. The tool is compatible with the ACTEL FPGA software and it allowed the integration of the FPGA component and the external multifunction card components on the same PCB. The integration of the ORCAD tool into the FPGA CAD suite was achieved. The evaluation and selection of the CAD tools took 5 BEDE person days and 0.5 UNN during month 2.
- To design, synthesise and simulate the VHDL model for the FPGA component took 60 person days during months 3 and 4 with 7.5 design assistance days from the UNN. VHDL Libraries were developed and tested and an FPGA design flow was adopted.
- The PCB track layout took 10 person days in month 5.
- The VHDL FPGA test bench design took 20 person days and 1 day from UNN in month 4.
- The FPGA programming of ACTEL devices took 5 person days in month 5.

- The test set-up design for the multifunction PC card took 10 days in month 5.

The fully functional ISA bus was developed by BEDE engineers using VHDL modelling techniques and was synthesised and simulated successfully. This was achieved with minimum assistance from the subcontractor.

In addition, BEDE developed a high level interface to allow testing the FPGA components using the functional behaviour, such as DMA, IRQ, Reset etc. This is to allow operators to test the components and PC cards without prior VHDL knowledge. This modelling is at a high level of abstraction in the hierarchy tree which allows BEDE the flexibility of modelling new PC card ideas and to simulate the design concept before the actual subsystems conception. This resulted in a reduction of the design time and helped BEDE to be a market leader, meeting client's demands in a very short time. This high level of modelling was used in the development of two new cards which were available for sale within one month of completion of the application experiment.

Evaluation

This consisted of the performance evaluation of the prototype multifunction PC Card with the prototype FPGA fitted. A test set-up was designed and manufactured in tandem with the test software to fully verify the complete system's integrity. The evaluation process was extremely detailed in order to verify that the design-flow, modelling and simulation processes were correct and repeatable for future designs. Functional, behavioural, timing and environmental tests of the FPGA component and the multifunction PC card were carried out successfully, and the card has been tested in a number of computers under all possible conditions. The evaluation process required 62 person days during months 6 and 7.

9.2 Actual Project Costs Claimed

The approved budget for this Application Experiment was 40KECUs. Cost statements were made and submitted monthly and quarterly to the TTN. The monthly expenditure and claims, shown below, were in line with the experiment workplan of section 4.1 above. During the lifetime of the project, it was tightly monitored with set tasks and deliverables. Both the AE manager and the TTN officer have worked together and BEDE have managed to deliver all tasks on time. Monthly claims were submitted to the TTN and are detailed below; these claims exclude subcontractors costs.

	Claim £	Persondays				
		Management WP1	Specification WP2	Training WP3	Design WP4	Evaluation WP5
Month 1	6,029.19	5	18	6	0	0
Month 2	4,862.57	2	0	5	20	0
Month 3	3,667.57	3	0	2	20	0
Month 4	4,593.06	2.5	0	0	30	0
Month 5	4,610.86	2	0	0	40	0
Month 6	4,307.38	2	0	0	0	35
Month 7	3,942.04	3.5	0	0	0	25
	----- £ 32,012.67 =====	----- 20 =====	----- 18 =====	----- 13 =====	----- 110 =====	----- 60 =====

BEDE subsidised travel expenses to allow the flexibility of purchasing ORCAD at no extra cost to the approved budget. This also compensates the loss of some of the FUSE funding due to the fluctuation of the rate of exchange from ECUs to pounds sterling which affected cash flow. The extra cost borne by BEDE, not shown above, was recovered during the first month of the product sales. Eliminating the effect of the rate of exchange on the experiment budget there was no deviation from the original budget planning. The company funded the extra 18 person days taken to complete the experiment and this cost was recovered in the first sale of the new PC cards.

The design work package (WP4) consumed 50% of the total experiment person-days. This is considered moderate for a first user due to the complexity of the tasks delivered. The design of the following two new FPGA products consumed much shorter time. This was due to the reusability of a large proportion of the VHDL code from the component library generated under FUSE experiment.

Evaluation phase is essential and BEDE carried out a comprehensive test to insure that the FPGA component and the PC card complies with the set specification. This helped BEDE staff to reconsider other issues such as the card performance, clock rates and initial conditions which was of less importance when designing a PCB circuit using discrete components.

BEDE documented the design lifecycle and the procedures used for each CAD tool (model, simulate, synthesis) and also for programming ACTEL devices. This is a work through manual and other BEDE staff can use it to independently learn how to design and test a FPGA product. It proved useful as a step-by-step check list to guarantee correct design first time.

10. Subcontractor Information

The two sub-contractors used by BEDE Technology Ltd were:

Subcontractor 1 University of Northumbria at Newcastle (UNN)
School of Engineering
Dept. of Electronic Engineering & Physics
Ellison Building
Ellison Place
Newcastle upon Tyne NE1 8ST

The Microelectronics Design Centre is based within the School of Engineering at the University of Northumbria at Newcastle. The Centre was set up by the UK Department of Trade and Industry as a centre of excellence to introduce microelectronics to SMEs within the North East of England and to help develop and support this technology transfer. The aim is to provide independent and impartial advice and solutions to companies on a cost-effective basis by providing access to a highly qualified, innovative team of experts. The Centre is equipped to provide the training and design assistance service needed for this experiment. The centre is easily accessible.

The UNN provided the following services to the First User:

- ❑ Training:
 - For FPGA project management
 - VHDL modelling and synthesis CAD tools,
- ❑ Design assistance during FPGA technology selection, design, and evaluation.

The training courses included full documentation packs and practical sessions. They were invaluable to the Project Manager and two Engineers and allowed them to develop a design-flow using the Synplify, V-System and Designer Series CAD tools for Actel FPGAs. UNN provided management and technical advice throughout the project and assistance with design flow and software problems.

Subcontractor 2 Interconnection Systems Ltd
South Shields
Tyne & Wear
NE33 5BU

Interconnection Systems Ltd (ISL) is a local manufacturer of Printed Circuit Boards. They employ 1400 people and are the largest manufacturer of PCBs in Europe.

The role of ISL in this project was to provide the prototype PCBs from CAD files. BEDE have worked with ISL for many years and they provide an extremely fast, cost effective and efficient service

Results

11. Barriers Perceived

The following are the perceived barriers which delayed BEDE from adopting FPGA technology prior to the FUSE experiment.

11.1 Knowledge barrier

The main barrier, perceived before and at the start of the project, was the lack of knowledge of FPGAs and VHDL design methods. The technical staff were aware of the technology however its applicability to BEDE products were unknown. The new orders and the short market windows as well as the economic climate left BEDE with no time to investigate this technology option. Prior to the experiment, the VHDL modelling was seen as an additional design task which could result in extra time and cost. FPGA case studies were unavailable to the company management until autumn 1996's North East FUSE seminar, which triggered BEDE's interest in experimenting the technology.

11.2 Psychological

The top-down VHDL design route adopted represents a large risk for an SME but offers huge benefits for future product development and sales. The company has seen this as a psychological barrier (too risky) and probably would have opted for the safer schematic capture solution.

11.3 Technological

The major technological barriers in this project were as follows:

- **Integration of VHDL CAD tools from different suppliers.**
Currently, there is no cost effective, fully integrated CAD tool for FPGA design and VHDL modelling. BEDE had to select and evaluate a number of packages from a number of suppliers. The selection of the appropriate CAD tools and then interfacing these as part of the design, test and production procedures were seen as a major technological barrier to a First User. This was partially due to skills and knowledge shortage at the beginning of the experiment and also due to the difficulties dealing with biased suppliers.
- **Requirement for more I/O lines on the FPGA.**
Device selection represents a barrier due to lack of knowledge of its size and I/O requirement at the start of the experiment. The first developed prototype PCB was a simple I/O card used to test the BEDE Technology design-flow (e.g. VHDL coding, synthesis tool, simulations, and place & route tools). This used an Actel 4000 gate A1225XL FPGA in an 84-pin PLCC package. It had been assumed at this stage that an 8000 gate A1280XL device in an 84-pin PLCC package would be suitable for the final prototype multifunction PC card. However, it soon became obvious that to meet the specifications more I/O lines would be required for the ISA bus and the card I/O connector.

LAYOUT AND ROUTING OF PCBs

BEDE's existing PCB layout tool was completely manual and not suitable for such high density PCBs. This represented BEDE with a barrier designing PCB cards to accommodate the 8000 gate A1280XL FPGA devices.

11.4 Financial

Technology upgrade is always expensive and risky and the financial barrier was high for such a small company. The management were reluctant to invest because the market for the existing cards using discrete components was still active though the orders were decreasing.

12. Steps taken to overcome barriers

12.1 Knowledge barrier

This was overcome with the help of the University of Northumbria (UNN) who provided an excellent training programme, documentation and design assistance throughout the project. FPGA case studies helped BEDE management to realise the capabilities of both the technology and the benefits of modelling at a higher level of abstract.

12.2 Psychological barrier

The technical support of the FUSE programme and the UNN subcontractor helped BEDE engineers to overcome this barrier through efficient design assistance and practical hands-on developing VHDL models. Modelling has saved the company design and test time and cost. It allows the company to investigate alternative solutions and build a fully tested model library that is applicable for future products.

12.3 Technological

All technological barriers were successfully overcome during the experiment with the effective technical help from the TTN staff and the design assistance provided by the University of Northumbria (UNN).

- **Integration of VHDL CAD tools from different suppliers.**

The VHDL CAD tools chosen for the FUSE project were the Synplify synthesis tool, V-System simulator, and Actel's Designer Series place & route tools. The three versions of CAD tools which integrated fully and were used to perform the application experiment were Synplify V2.6c1, V-System 4.6 and Actels Designer 3.1.1

The Synplify synthesis tool worked extremely quickly and efficiently. The only minor limitation of this product was the relatively poor text editing facilities, which will be upgraded in the next release. There were no problems integrating Synplify with the other CAD tools.

The V-System simulator was the most important CAD tool for top-down VHDL designs because it was used to simulate the operation of VHDL code before synthesis, after synthesis and after place & route with the VITAL timing libraries. V-System was the tool which determined if the designs would work or not. The CAD tool was found to be extremely good value for money and had no problems integrating V-System with the other two tools.

The ACTEL Designer Series software was extremely good as a stand-alone product but there were problems integrating it with the other chosen CAD tools. The major problem was with bi-directional data busses. The original version had a software bug that caused busses which were synthesised by Synplify to be reversed. The designer worked around this for most simulations by using extra VHDL code to reverse these busses for display by V-System. As three different suppliers were used for VHDL CAD tools the cause of this problem was initially very difficult to track down. However, a new version of Designer was received, which addressed this problem.

TTN technical support during the consultation with the CAD vendors helped BEDE to overcome this barrier

- **Requirement for more I/O lines on the FPGA.**

This problem was overcome by choosing the same 8000 gate A1280XL device but in a PQ160 package with 125 I/O lines. The chip was mounted in a socket on the PCB for test purposes. BEDE engineer identified the correct device after consultation with the ACTEL device supplier.

LAYOUT AND ROUTING OF PCBs

This problem was overcome by purchasing the ORCAD schematic and layout CAD tools, which were also compatible with the ACTEL FPGA Designer Series software. This additional purchase had not been planned for and slightly exceeded the budget for durable equipment, but after discussions with the TTN it was agreed that BEDE Technology Ltd would subsidise the travel and subsistence costs to keep the total project costs the same.

12.4 Financial

The FUSE financial assistance has helped to reduce the inherent financial risk involved in introducing new FPGA technology and VHDL design techniques at BEDE Technology Ltd. Without this assistance BEDE management would have adopted the cheaper and less flexible schematic capture approach and introduced it over a longer period. The response from customers to the first three products in the new range and the new niche market for custom designed cards, has clearly demonstrated the benefits of the FUSE programme to BEDE Technology Ltd.

13. Knowledge and Experience Acquired

As a result of the FUSE project BEDE Technology Ltd have gained in-house expertise in FPGA design and VHDL software techniques. This expertise has been used to develop a BEDE design-flow manual and high-level simulation and modelling system for future PC card designs. The company has also gained knowledge in:

- Microelectronics management skills
- Experience of different FPGA technologies, their advantages and limitations
- CAD tools, their capabilities, limitations and cost
- Design hierarchy and the importance of following a well defined methodology to reduce design time and to improve performance productivity

14. Lessons Learned

CAD Selection

Without the impartial advice, training and design assistance BEDE would find the selection of the CAD tools a difficult task especially at the start of the experiment. Error of judgement would cause the loss of First User's confidence on the technology as well as financial risk which is too high for SMEs. BEDE consulted with the TTN and the UNN technical staff, and used all of the FPGA available CAD packages at the University of Northumbria before selection. This proved useful to try the CAD before purchasing because it allowed BEDE to select a cost effective CAD tools with minimum interface problems, which currently constitute a fully integrated design system. This system was used and it will be used to replicate the technology in BEDE's future products.

Reduced Time to Market

The use of best practice, modelling, and synthesis tools have helped the company to improve their productivity. The development time for a new PC card within a new system has been reduced from 3-4 months to 3-4 weeks. This is achieved by incorporating a well structure design method in company product's design and manufacturing process. This is based around the top-down design methodology. As a result of the experiment, the VHDL modelling is employed for new systems, subsystems, and individual devices. This has given BEDE the flexibility to move to other FPGA or ASIC technologies with a much-reduced risk factor.

The initial acceptance of the new methodology was slow, however, during the last quarter of the experiment BEDE management with the help of the subcontractor realised the benefits of high level and structured design methods, and now the company is gaining the benefits of the technology.

Increased Functionality

The FPGA technology allows more functions for each PC card for the same PCB area. Customers see this increased functionality as a major benefit and it has boosted sales. The FPGA holds the enhanced digital functions for use in a universal PC card with enough space for future expansion. This replaced a number of existing cards. Now BEDE can meet orders, which was not possible in the past due to the shortage of the PCB area.

Reduced Costs

The use of Actel FPGA devices has significantly reduced the production costs. A single FPGA device has replaced all of the card's digital components. The cost/gate of these devices is far smaller than discrete ICs and the required PCB area has been reduced by 50%. Labour costs in the assembly of the new PC cards has reduced by 50% and the use of a generic main PCB for all new cards has further reduced costs. As a result of the FUSE project the overall production costs have been reduced by 40%.

BEDE with the design methodology implemented during the experiment are now able to move from one FPGA family or supplier to the other, this allow flexibility to manage the production costs and therefore the profit margins.

High Level PC Card Simulation

BEDE have developed and documented a high-level PC Card simulation system for new product designs. This system can be used by test engineers who have no previous experience of VHDL to test and evaluate the performance of new designs without prototyping. This system was implemented to successfully produce two new additional products.

New Niche Market

A new niche market for BEDE is the supply of customised PC cards that have design functions ordinarily only available on several PC cards. A large military customer and an OEM have evaluated and ordered the first custom PC card designs. BEDE has also entered the VHDL modelling market, licensing their VHDL models to other companies through the Internet.

A new service has emerged following the successful completion of the FUSE experiment in the area of consultancy. BEDE is currently offering a consultancy service and design assistance to a number of clients in the North East and Scotland, similar to that of FUSE. This is a new venture which has proved profitable during 1998.

Enhanced Sales

The knowledge and experience, which has been gained by BEDE through FUSE, is currently being used to produce a new range of PC cards. Two of these cards are already being sold and BEDE has received orders from existing and new customers. The customised PC cards are also producing a great deal of interest among large customers and orders were received following the introduction of the FPGA cards. As a result of the FUSE project, sales of the new products have outstripped those of the older products during the last quarter of 1998.

15. Industrialisation and Internal Replication

The production of the new PC card and a further two new cards (internal replication) were advertised for sale in the company catalogue of summer 1997. A new range of FPGA based cards have been manufactured and are now advertised in the company catalogue, as a result of this programme. The knowledge gained has resulted in a niche market supplying custom designed PC cards, which can now be supplied within 3/4 weeks. Additional new products are currently being developed using the expertise and the new technology acquired.

A large number of FPGA PC cards are being sold through OEMs and directly to clients. Currently, the cards' main clients are Marconi Avionics and the National River Authority.

To enhance the sales of the first three FPGA products, BEDE have:

- Participated in a seminar at Sheffield, organised by the TTN in October 1997. This generated a number of enquires and industrial contacts.
- Published a new catalogue with all of the new PC card applications.
- Carried-out a mail-shot targeting 400 customers during November/December 1997 to advertise the services now available.

BEDE now offer the following, as part of their service, which has started to generate interest and additional business:

- Full design assistance on VHDL and FPGA design and evaluation.
- Licensing of BEDE's VHDL models to other companies which is a FUSE experiment spin-off.

A step-by step design flow manual was produced during the experiment to help BEDE engineers to model using VHDL, and to synthesis, simulate and test FPGA products. This manual is currently used internally for training new staff or as a reference to help existing design staff to follow a well structured and proven design steps. This manual is available for purchase from the North East Satellite Centre at University of Northumbria at Newcastle.

The company has invested in a new building to house a new manufacturing and production facilities for FPGA based PC cards. This venture is now ready and production was started during autumn 1997. The company is now replacing its outdated technologies in their PC range and also developing new products using FPGA technology.

During Spring 1998, BEDE invested more than 1m Euros in a new production facility, of which 360k Euros was dedicated to the FPGA production. This is a substantial capital investment by a small company due to the increase in orders since the completion of the AE.

16. Economic impact and improvement in competitive position

The FUSE programme has been a great success and BEDE have gained valuable experience and in-house expertise that has been applied to produce new products and open up a new niche market for customised PC cards. The sales revenue from the new range of PC cards has increased and is expected to continue over the next two years. It has currently exceeded that of the old products since December 1998.

As a result of the FUSE experiment a new improved range of data acquisition cards were phased-in over a nine months period and a new niche market for customised PC cards has been established.

The new range of PC cards provides increased functionality and covers a wider range of applications than competitors' products. Since this range uses a generic main PCB and common FPGA component, only the daughter boards need to be

upgraded and FPGA programmed to keep the product range up to date. This will ensure that new products are available to customers ahead of competitors. The first three new products in this range are being sold in the company's summer 97 catalogue.

New FUSE Product

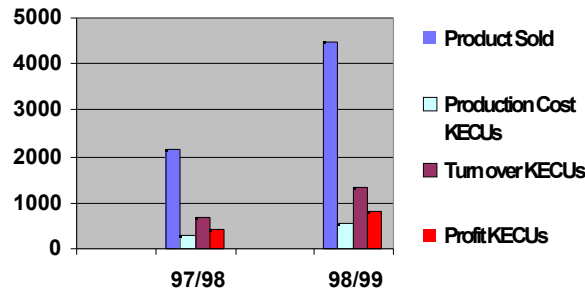


Figure 2

A new niche market for customised PC cards has been established as a result of the application experiment. This customisation service is not available from any of the competitors and therefore this is an ideal opportunity to exploit a new market. The established market research and actual first quarter orders indicate a 3-4% increase of BEDE market share during 1998/99 (see figure 2). This information is based on data acquired from BEDE's existing military and OEM customers for the new PC Card developed under the FUSE experiment. This is expected to grow during 1999 as a result of the company's marketing decision to address a number of new OEMs in UK and Europe.

16.1 Profits

The company is extremely satisfied with the new products which are currently in production. This new range of products will provide a basis for further expansion at BEDE Technology Ltd with more capital investment and further job creation.

The new range of PC cards will range in price from as little as £95 up to £900 depending upon

- complexity,
- volume, and
- whether a customised solution is required

The manufacturing costs of the new cards have fallen by 40%, significantly increasing profit margins. The PC card yield has risen due to the use of a single FPGA device to replace all of the digital components. This improves the card's MTBF. The repair of cards, when faulty, is faster, simpler and lower labour cost with less fault finding required.

BEDE market share of PC data acquisition cards has increased from 0.7-1% to 2-2.5% during 1998. By 1999 BEDE's market share is estimated to reach 3-4%.

The revenue from PC cards sales by the end of 1999 is expected to be in excess of 1.5m ECU. The FUSE program has been beneficial to BEDE Technology Ltd and should promote business expansion and considerable revenue increases in future years. For example, the forecasted sales at the beginning of the experiment from Figures 2 is in excess of 4,000 units per annum, but the actual is in excess of 6500 units.

It was estimated in January 1998 that an increase of 360% in sales of the improved product would be achieved over the existing one during 1998/99. This would result in an increase of 400% in company profits, see Figures 1 and 2. 1998's sales indicate that these figures will be met during the first quarter of 1999.

The payback of the FUSE experiment funding of 40kECU was secured during January 1998. The return on investment is expected to be 5-fold.

16.2 Product

Two new PC cards (PC-MF12 and PC-DIO48CT) have been produced as a result of the FUSE project. These new cards are advertised in the company catalogues and have generated a great deal of interest from customers. Using the new PC card

simulation system, BEDE expect to complete a further 10 new PC card designs during 1998. This amount of new product development in such a short time would not have been possible without the FUSE project.

16.3 Company Personnel

The Technical Manager and two Design Engineers have benefited from the FUSE program as a result of the training, design assistance and experience. The training and design assistance were an essential part of the FUSE project which helped underpin the necessary knowledge required for future self-sustained development.

The high-level PC Card simulation system for new product designs is being used by test engineers with no previous experience of VHDL, to test and evaluate the performance of new designs before prototyping. Test engineers not involved in VHDL design now benefit from the FUSE project.

The skills developed by BEDE personnel will be applied to projects in other branches of the company, e.g. custom test equipment design and automation systems. This will further exploit the benefits of the FUSE project.

17. Target Audience

The target audience for FUSE information contained in this demonstrator document are SMEs in the industrial control, automation, data acquisition, telecom, and IT sectors which currently use discrete ICs in the design of their products. For instance, companies with the following prodcom codes:

3002 Computers and other information equipment
3210 Printed Circuit Boards and other electronic components
3320 Instruments and applications for measuring checking and testing, etc

These companies operate in a wide range of sectors including Industrial process control, telecoms & networking, automotive, aerospace, test & measurement etc.

- Small companies with electronic design expertise.
- Companies with PCB design capability and experience and who have not yet ventured beyond the use and application of conventional discrete components in their designs.
- Companies using or developing (assembling or designing) computer automation and control products

The demonstrator highlights the choice of selecting ACTEL devices (which is still applicable to most of the other antifuse devices) and the importance of following a best practice procedure to reduce product design time.