

FUSE DEMONSTRATOR DOCUMENT

AE194

Improved Blood Flow Monitor

ASIC technology improves performance at lower cost.

Company: Huntleigh Diagnostics Ltd

TTN: University of Glamorgan Commercial Services (UGCS) Ltd

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Version 2

Abstract

Huntleigh Diagnostics Ltd. is an established company that designs, develops, manufactures and distributes electronic medical diagnostic equipment in the healthcare market sector (Prodcom code 3310). These products are aimed at the healthcare market, including primary care suppliers. Company turnover is approximately 9 MECU and the company employs 130 people.

Huntleigh Diagnostic's product range includes a range of ultrasound handheld instruments ("Dopplex"), for cardio-vascular and foetal assessments, and a range of foetal monitors. These products combine technologies ranging from discrete analogue electronic devices to micro-controller devices and digital signal processors. No higher order device technologies are currently applied in Huntleigh's product range.

The objective of this experiment is to improve the Huntleigh Diagnostics' current range of Dopplex products. These are hand-held medical diagnostic monitors for use in measuring blood flow and monitoring foetal heartbeats. Each product consists of two parts, an ultrasonic probe and a main diagnostic unit. The proposed ASIC is intended to replace much of the circuitry in the main unit.

The application experiment resulted in the development of a mixed signal ASIC to extend product functionality and broaden market applications in the vascular field within the constraints of battery powered handheld devices at a low cost. This will lead to greater market share.

The application experiment used ASIC technology to allow:

- Reduced manufacturing costs
- Enhanced functionality of the product by performing fast Fourier Transform (FFT) and the extraction of the maximum frequency envelope.
- Improvements in the diagnostic capabilities of the instrument.
- Greater interchangeability of sensors.

The AE cost was 174 kECU. The payback period when implemented in a new product range will be approximately 1 year, and the ROI is anticipated to be 340%.

The duration of the application experiment was 21 months. The application experiment was delayed from the original 14 month time scale by the departure of the company's design engineer and the retraining of a new engineer during a critical phase of the programme of work.

The company has developed a sustainable capability in ASIC development, including the technical management of the design process and assessing its economic benefits.

The dissemination information included in this demonstrator document will be of interest to the managing directors, technical managers and decision makers in small to medium sized companies operating where pressures towards producing small, lightweight, complex Digital Signal Processing instrumentation is present. The target industry sector includes companies operating in the medical (Prodcom code 331), instrumentation (Prodcom Code 3320) or computing (Prodcom code 3002) industrial sectors.

Keywords and AE Signature

Medical Equipment; Blood Flow Monitoring; Health Care Instrumentation; ASIC Development

AE Signature: 5 0161 550 0200 2 3310 2 33 UK

1. Company name and address

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2. Company size

The number of personnel employed by Huntleigh Diagnostics is 130. Of this number, 12 have expertise in microelectronics. The site also houses a design support team for the Huntleigh Technology plc group of companies, which comprises 8 persons.

Company sales per annum are 9 MECU per annum.

3. Company business description

The Huntleigh Technology group of companies, of which Huntleigh Diagnostics is a wholly owned subsidiary, manufactures a wide range of products in the UK for the healthcare industry. These products range from hospital furniture through to electronic monitoring devices. A number of manufacturing sites are located throughout the UK and are supported by sales, distribution and service subsidiaries, located in key sites throughout the world including Germany, France, Holland, Australia and the United States of America.

Huntleigh Diagnostics is the only member of the group with electronic system design and manufacture capabilities. It acts as the design resource of electronic systems for the whole group and manufactures sub assemblies for other plants to assemble into their products. Particular areas of manufacturing expertise include surface mount technology, automatic test equipment and modern assembly techniques in medium volume manufacture.

In addition to the above, this division has its own product range of Doppler products which includes hand held pocket Doppler equipment for vascular examinations and foetal heart rate monitoring and a recently launched foetal monitor.

The company's industrial sector is therefore, defined by Prodcom Code 3310 (Medical equipment)

4. Company markets and competitive position at the start of the AE

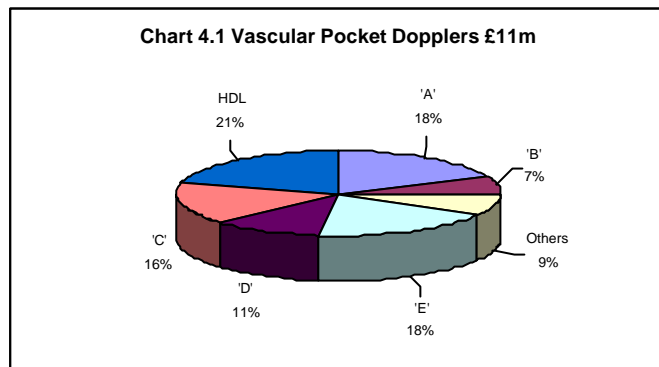
The company's clients for these equipment are a wide range of primary and secondary healthcare providers throughout the world, including doctor's surgeries, private and public hospitals. The company has a sales, distribution and servicing, network located in key sites throughout the world, including several counties in mainland Europe, Australia and the USA.

In the Healthcare industry, more and more emphasis is being placed on primary care and in care in the community, both of which require a high degree of portability for the equipment used. This has resulted in a distributed approach for healthcare devices and a need for increased functionality at a reduced size. Many of Huntleigh's current range of products are already designed to be portable.

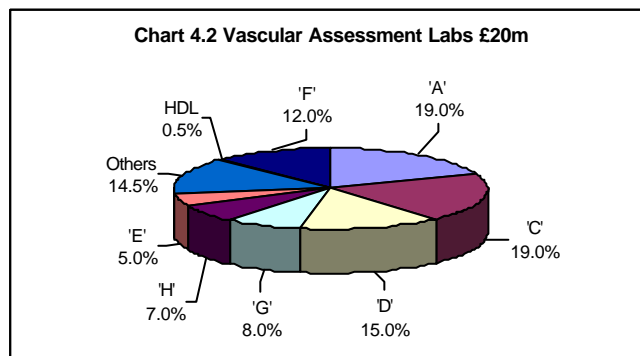
However, to protect and to improve current market share against other non-European manufacturers, further functionality improvements are required in these portable equipment. ASIC technology affords an opportunity to provide this enhanced functionality.

4.1 Competitive Market Position

The charts 4.1 and 4.2 below best illustrate Huntleigh Diagnostic’s position in the marketplace for both handheld and desktop vascular assessment devices. Currently higher cost equipment using advanced digital processing of the signals is used in vascular assessment laboratories. This is an area in which the company does not have a strong market position.



The company’s Vascular Pocket Doppler products were the first of type product used in the medical area. The current competition faced by the company has adopted similar technology solutions in their products to provide similar end user functions. The technologies adopted by these competitors are invariably based on the use of microcontrollers or DSP processor devices to provide the functionality included in these products. Our vascular pocket Dopplers offer a range and performance that continues to lead our competition.



However, because of the similarity in terms of product implementation technology, the price of the competing products is similar to those of the company’s. Little competitive price differential therefore exists.

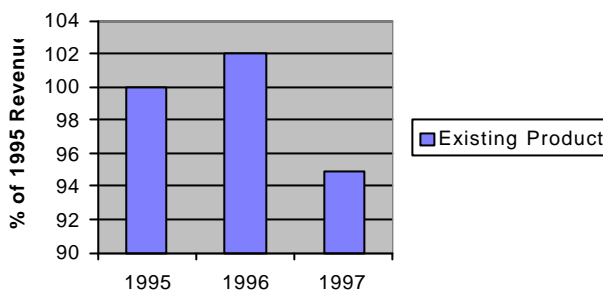


Chart 3.3 Sales Trend for the Existing Equipment

Company sales indicate a slight decrease in sales revenue as a result of increased competition, and reductions in sales price margins resulting from this competition.

Competitive advantage is therefore related to technical performance and to the advantages that this offers to the clinician using the equipment. The objective of this application experiment is to include a higher level of functionality into the hand held device thereby enabling tasks that could only be previously performed by the laboratory equipment to be conducted using portable equipment.

5. Product to be improved and its industrial sectors

The Dopplex range of products manufactured by Huntleigh Diagnostics principally comprises of an ultrasonic probe connected to a hand-held main unit. These units utilise standard discrete analogue and digital devices and components, and microcontroller devices.

The ultrasound probe, illustrated in Figure 1, is used to non-invasively examine the body by emitting harmless signals that are reflected at boundary changes in physical matter, or reflected by movement. The latter causes changes in pitch and in frequency due to the Doppler effect. In vascular applications of this technique, blood flow in the vascular system can be observed, and a range of clinical diseases detected. It is also possible to produce waveforms that indicate the rate and the direction of flow such that its velocity profile can be estimated, and changes during the cardiac cycle monitored.

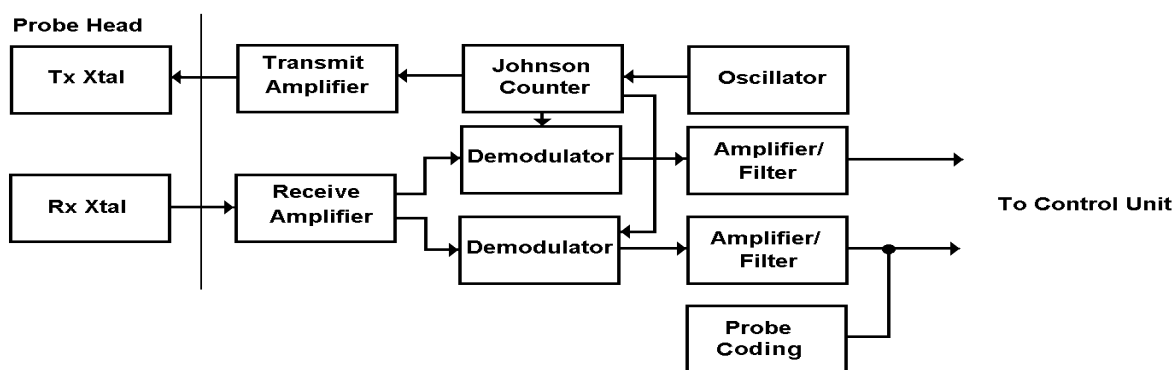


Figure 1: Probe Assembly Block Diagram

The probe assembly is a compact unit, and is therefore limited in its functionality. The main function performed in this unit is the quadrature demodulation of the amplified receive signal from the ultrasonic receiver amplifier and filtering of the resulting 2 channel signals before these signals are communicated to the hand held unit via a standard cable. The probe coding is used to enable the unit to enable several different probes to interface to the hand held units.

The functional block diagram of Figure 2 describes the hand held unit. This unit is centred on the use of a microcontroller device, which provides the control and data outputs to display information on a small LCD display mounted in the hand held unit. The display information includes information relating to the pulse rate of the signal, and the levels of return. The microcontroller also recognises the probe unit connected to the hand held unit, and processes the received information accordingly.

The hand held unit also processes the modulated receive information from the probe unit to provide an audible output of the returning ultrasonic signals from the test body. The hand held unit incorporates a small loudspeaker. The unit does not provide any processing of the information, beyond the translation to basic display information.

The increasing competition and reduced margins achieved from existing products require the company to provide additional product features to discriminate the company's product from competitor offerings. The next logical advance in providing additional user benefits is for a portable vascular device offering a colour sonogram display, a 3D plot of time and signal power against Doppler shift frequency. This would put the power of a vascular workstation in the clinician's pocket, and offers a major market opportunity.



Photo 5.1 Photograph of the Existing Product

This enhancement of the product’s functionality is the objective of Application Experiment. The functional parameters of the existing product remain functionally unchanged but significant additional, primary functional improvements will be incorporated, and these include:

1. performing a 256 point fast Fourier Transform (FFT) processing,
2. the extraction of the maximum frequency envelope at a rate of 3ms per frame, and
3. improvements in the diagnostic capabilities of the instrument by the visual presentation of the sonogram information on a LCD display.

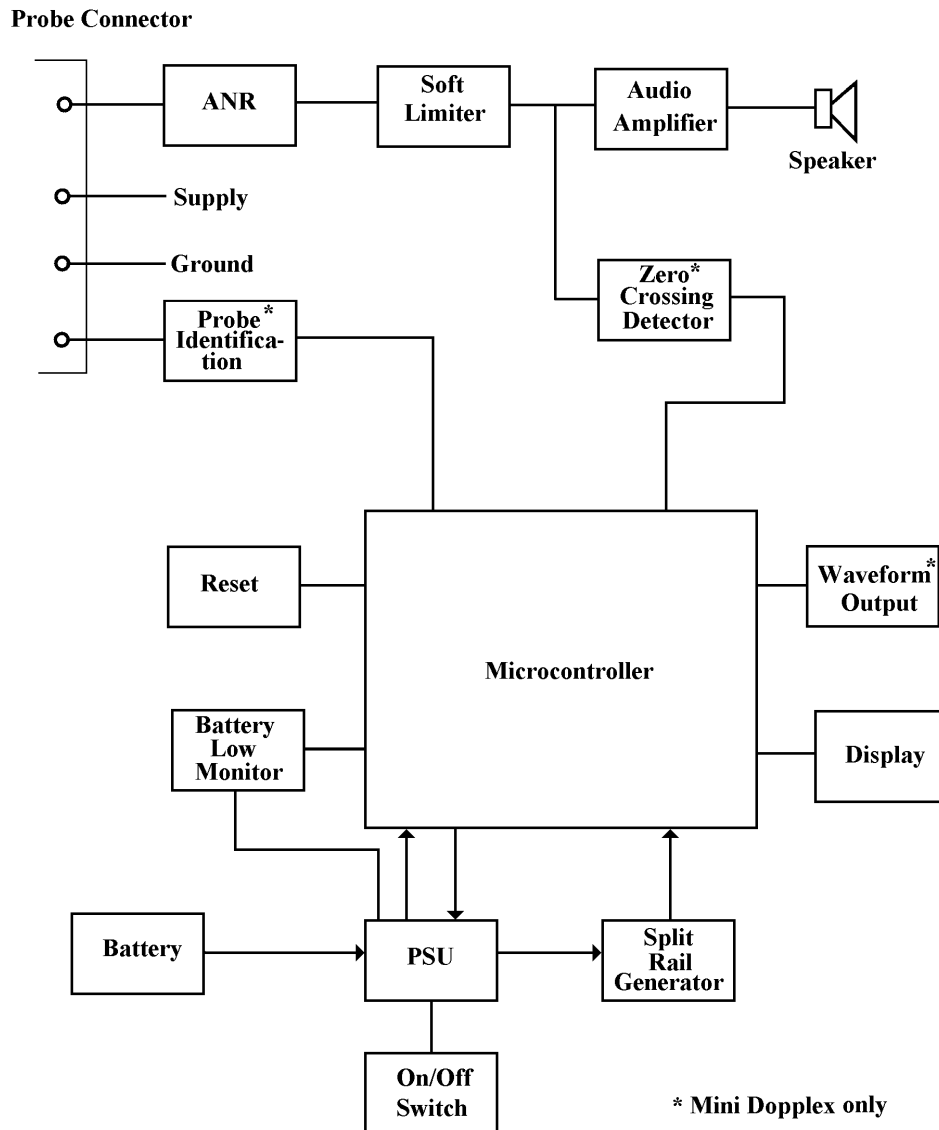


Figure 2: Hand Held Unit Block Diagram

6. Description of the technical product improvements

The improved ‘Dopplex’ unit contains a mixed signal ASIC, which provides the following enhancements:

- Simpler to manufacture and test – lower cost.
- Improved applications and functionality, based on the introduction of a display of the sonogram information to allow the clinician to improve his / her diagnosis of vascular ailments.

The product of this Application Experiment is a mixed signal ASIC that augments the signal processing in the existing Doppler range. The component:

- Enhances the functionality of the product by performing fast Fourier Transform (FFT) sonogram generation and enables extraction of the maximum frequency envelope within 3ms.
- Improves the diagnostic capabilities of the instrument by the provision of an integral LCD display facility.
- Enables replacement of expensive vascular workstation with a lower cost portable equipment.

The ASIC functional description is shown in Figure 6.1. Figure 6.3 is a Functional Block Diagram which shows more detail (see the end of this section).

The ASIC receives the two signals in analogue form. To generate a sonogram that displays forward and reverse flow, one signal must be in phase quadrature with the other (i.e. 90° out of phase). In vascular applications this phase lag or lead (dependent upon forward or reverse flow) is produced from the reflected blood by the ultrasound probe.

The frequency analysis of ASIC is performed in the digital domain. Since the signal sources to the ASIC are analogue in nature, dual analogue to digital converters (ADCs) are required. Once the information has been converted to digital format, it is passed to the FFT processor (frequency analyser). The processor then performs an FFT.

The maximum sampling rate of the on-chip dual, 10bit analogue-to-digital converters is 64samples per second with a master clock of 16MHz, though this is scaleable. With reduced master clock speeds the maximum clock speed is also reduced (e.g. 32samples/sec at 8MHz).

The benefit of this is the ability to dynamically adjust the power requirement for each application or to send the device to sleep by reducing the clock speed. The maximum sampling rate of the on-chip dual, 10bit analogue-to-digital converters is 64samples per second with a master clock of 16MHz, though this is scaleable. With reduced master clock speeds the maximum clock speed is also reduced (e.g. 32samples/sec at 8MHz). The benefit of this is the ability to dynamically adjust the power requirement for each application or to send the device to sleep by reducing the clock speed.

The sampling rate at each master clock speed is divisible in 8 steps from 64kHz down to 500Hz. Decreasing the sampling rate means an increased frequency resolution, but this is at the cost of an increase in the length of time that is required to acquire the necessary data to perform the FFT. This acquisition time, known as the *window period* is the reciprocal of the resolution.

At a rate of 64 samples/sec the window period of the ASIC is less than 4ms. In this time the chip must be capable of calculating a 256 point, real-time FFT and allowing it to be read by a bus-based microprocessor or other device. With an overlap of up to 50% at 64kHz sampling frequency, this processing time is reduced to 2ms. (Increasing the percentage overlap allows the window period to

be reduced without degrading the frequency resolution. This is achieved by using less new data. At 25% overlap, only 192 new points would be required).

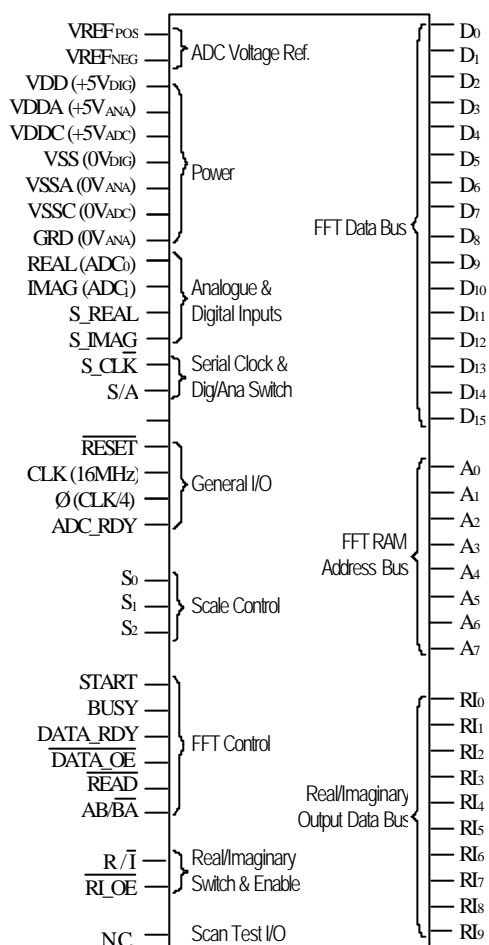


Figure 6.1. Functional Diagram of the ASIC device

The technical requirements of the ASIC consists of:

- A/D Conversion and data sequencing.
- Production of a 256 point FFT in the digital domain.
- A sonogram output stored in 256 RAM locations via an addressable 16 bit data bus.
- Complete, standard microprocessor interface and control.

The detailed specifications of the ASIC were confirmed using high level DSP tools. These included parameters such as the operating frequency required to perform Fast Fourier Transform functions on the incoming data. The required storage space for the results of the spectral analysis, the requirement for scratch pad memory and increased error resolution were benefits derived from the design-synthesis cycle.

Additional features were developed as by products of the design process:

- Serial digital data can be input as an alternative to analogue data, bypassing the ADCs.
- The 10-bit output of the dual ADC's is available as a switched tri-state data bus, addressable as standard RAM.

- The FFT data output can be switched to produce either a standard sonogram (minimum frequency in bin zero, and maximum frequency in bin 255) or a double-sided sonogram (minimum frequency in bin 128, forward frequencies in bins 128 to 255 and reverse frequencies in bin 127 to bin zero).

One key design requirement was for the ASIC was for it to be as low powered as possible, ideally less than 200mW. This is because the application is a battery powered handheld product.

A concept device has been developed to further investigate the lucrative marketing opportunities already identified (see Figure 6.2).

It is estimated that for the most complex of the products in the Doppler range a reduction of 63% of the component costs could be achieved.

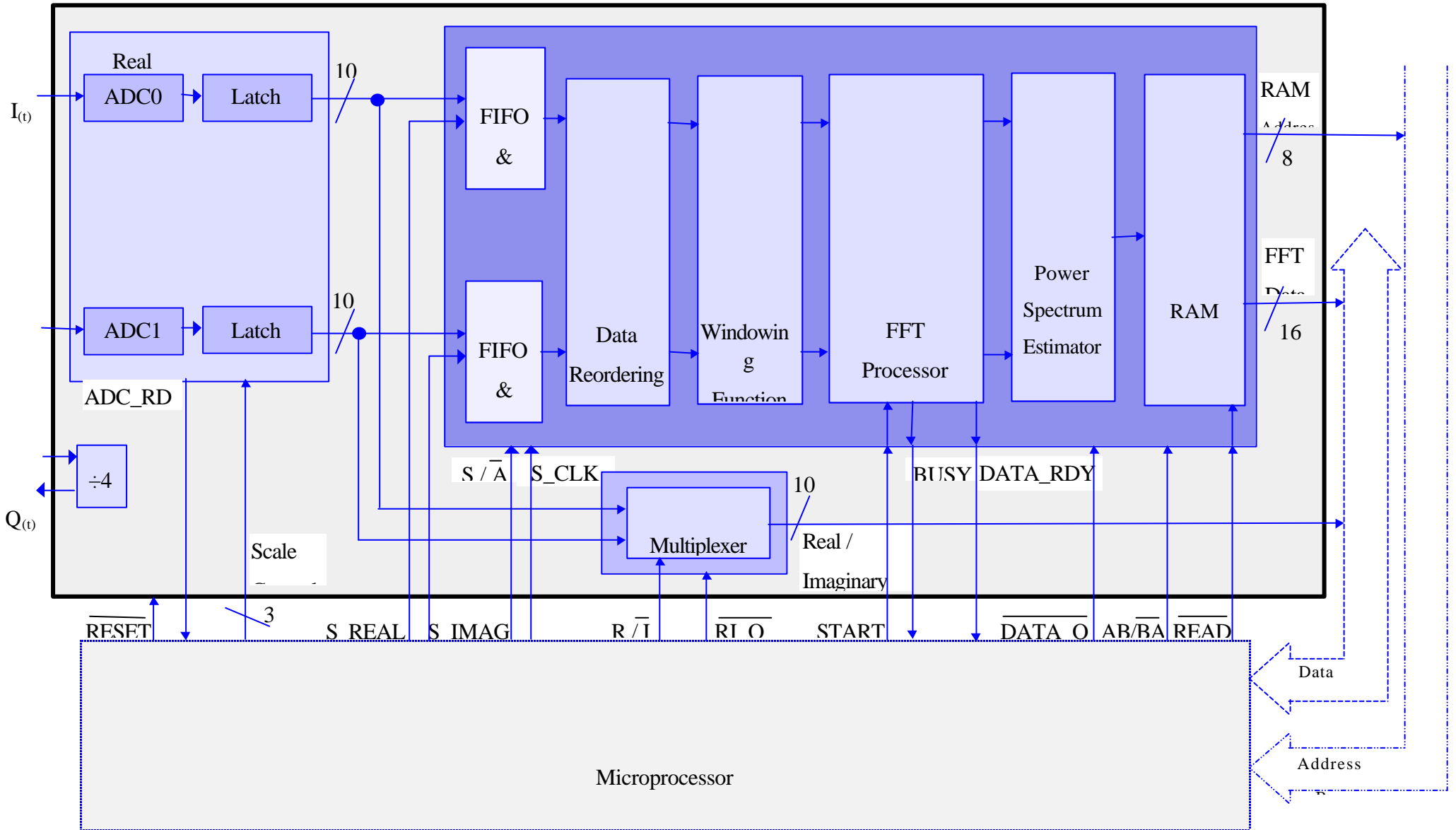


Figure 6.2 Doppler Concept Device Displaying a Sonogram

7. Choices and rationale for the selected technologies, tools and methodologies

The selection of ASIC device technology was identified as offering the best solution for the following reasons:

- High levels of integration – low component count.
- Analogue and digital circuitry can be placed on the same chip.
- Good design and simulation tools available.
- Standard cell technology offers a wide range of building blocks.
- Low cost prototype manufacture using the Multi-Project-Wafer route.
- Difficult for competitors to copy.



The current product utilises microcontroller device technology. However, the application of microcontroller technology to perform the complex real time processing of the received ultrasound signals was not possible using reasonably small pin count, and hence low cost, microcontroller devices. The company investigates the use of DSP (digital signal processing) devices, but again the specification of a device required to perform the processing tasks identified for the improved product resulted in too high an unit cost for the device.

Digital hardware technologies were therefore considered. The application of FPGA devices was technically feasible, but required the use of two or more FPGA devices, and therefore added additional complexity and cost. The only cost effective solution was that of a single ASIC device.

One concern in identifying ASIC device technology as the preferred route was the relatively low annual production volume anticipated by the company (a few thousand units per annum). Initial feasibility study contacts undertaken with the TTN identified a supplier of ASIC devices that was willing to supply units in the quantities identified, and at a unit price that was competitive to alternative technologies. After obtaining these reassurances the ASIC device route was then adopted.

7.1 Fabrication technologies

There were several technologies available that would have achieved the target of component size and cost reduction, including gate and standard cells, and full custom design. The choices that were considered in detail are outlined below.

Gate Arrays & Standard Cells

The final selection between these two technologies could be left until the final behavioural design had been assessed. Both options were viable for the AE in terms of performance and cost.

The gate array option was originally preferred, being the more cost effective. Later it became clear that implementing using this technology would have resulted in a product that consumed too much power. Also the memory requirements of the design were inefficient using gate arrays. Additionally, changing to standard cell technology enabled a mixed signal solution, allowing the use of on-chip standard cell ADCs. The final NRE cost of the technology was unchanged. The final production costs were improved significantly. Listed below are some of the reasons for finalising on standard cell technology:

- The technology allowed the replacement of the external, proprietary ADC (~£8.00) with a cheaper on-chip ADC (~£1.00 ea.).
- It reduced the chip footprint.
- A reduced overall pin count.
- Reduced overall power requirements.
- The NRE costs were unaffected.
- It allowed the replacement of the dual PWM outputs with DACs (digital-to-analogue converters).

This would have reduced the noise and produced better audio output. These were subsequently removed from the design altogether.

The ASIC device was implemented using a 0.8µ AMS mixed signal CMOS technology. The size of the ASIC implementation was approximately 36mm².

The ASIC prototype device was implemented using the Europractice MPW (multiple project wafer) route. This allowed the company to obtain prototype devices at low cost (< 5KECU production costs), and thereby avoid the risk of design problems occurring after commitment to a full set of expensive production masks for the ASIC device. The MPW route offered the opportunity of resolving design problems by the inclusion of several test pin outs for the prototype (which could be eliminated for the final production ASIC device), and a second MPW fabrication at low cost if required. In the event, the ASIC worked first time, but the elimination of commercial risk by adopting the MPW route is still considered worthwhile.

7.2 Design Methodologies

The design phase of the project was achieved using a combination of both behavioural level design and more conventional schematic capture. The complexity of the design required and the design time required for conventional methods dictated the use of high level tools such as DFL (data flow language) and VHDL. The DFL architectural synthesis methodology allowed the use of specialised DSP design capture techniques. The design methodology used the Mentor Graphics suite of design tools, including DSP station.

The architectural design produced by the DFL process, was implemented using high level VHDL and schematic capture methods to realise a design solution which was fully simulated. The simulation process utilised dedicated workbenches developed to test identified functional blocks, and the use of captured and digitised real world vascular signal inputs for system level simulation.

Due to the complexity of the design the use of effective simulation methods and tools was crucial. A mixed mode simulator was required to test the final design simulation with external analogue circuitry.

Test vectors were developed to enable device testing to be achieved. The CAE tools required to automatically generate the test vectors to fully test the completed device are expensive. Consequently, one of the criteria for choosing the silicon vendor was the ability to provide this service.

The final ASIC device incorporated full scan test, which simplified the test procedure. Using conventional functional and in-circuit test procedures would have been inefficient. It would have proved difficult to achieve the high level of fault coverage using alternative methods.

8. Expertise and experience in microelectronics

The engineering department at Huntleigh Diagnostics consists of 18 personnel split between mechanical design, electronic design, software design, printed circuit board design, production engineering, industrial design and project management.

Electronic design includes the capability of digital and analogue electronic design including the use of microprocessors and digital signal processing devices. The company's software design capability is focussed on generating code for embedded microprocessors and PC based systems. CAD tools are also used for PCB design which are mostly designed in house.

Prior to the start of this project Huntleigh Diagnostics had no experience of either the ASIC development process or the CAD tools required to design an ASIC device.

The following were allocated to the project:

- Design Engineer - Specification, testing and development of the ASIC. Development of software for the System Evaluation.
- Development Engineer - Development and prototype testing of the ASIC.
- Project engineer - Project management and specification

Additionally, a PCB designer was used to layout and produce boards for the Prototype Evaluation and the System Evaluation.

The Project engineer allocated to the programme was qualified to MSc. Level in Electronics, and had 18 years experience. The design engineer originally allocated to the ASIC design was also qualified to MSc. Level and had 1 years experience, but had some knowledge of VHDL methods. Upon his departure, a new design engineer was allocated with MSc. level qualifications and 6 years experience.

9. Work-plan and rationale

The following information describes the major work packages in the original and adopted work-plan and the rationale behind it.

Work-package 1: Technical Management

The task involved the technical and project management of all phases of the application experiment, including the development of subcontracts and their management, and the selection and purchase of the required design tools. The technical management task delivered an effective communication between all the subcontractors involved, and has resulted in a sustained ASIC technical management capability for the company. The time required from the task was 81 person days compared to the planned level of 78 person days

The company manager was supported by the TTN in undertaking the Technical Management role, especially in developing the understanding of the relationships and impact of the technology on work programme and costs.

Work-package 2: System Design and Specification

The system design phase consisted of the modelling of the proposed system architecture to confirm that the specification achieved the desired performance level. The modelling was performed using the DFL (Data Flow Language) on a Mentor Graphics DSP station. The use of simulation used the model to be proven, and optimal FFT, windowing, Only after this initial modelling was the detailed specification sampling rate, the frequency resolution, the FFT complexity and the filter orders.

Only after this initial modelling was the precise ASIC design specification generated to encompass all aspects of the ASIC device including functional and environmental parameters. A test specification based on the current product's test specification was also produced.

The modelling task was underestimated in that the apparently simplest design aspect (the audio channel) required extensive modelling effort to attempt to produce a cost-effective digital solution, and by time required to capture, digitise and convert the real world signals into a format suitable for

modelling inputs. The audio part of the design was evaluated using FPGA prototypes. The time taken was 80 person days as opposed to the planned 70 person days.

The role of the subcontractor in this task was to undertake the modelling task. The company engineers involvement included the capture of the real time input signal data, training on the DFL tools to be able to set this information up as test files, perform the simulations thereafter and feedback to the subcontractor on the adequacy of the model's performance.

The company's Technical Manager's involvement included reviewing the system design vs. cost trade-offs, and the preparation of the final system specification. The subcontractor reviewed the document, and provided suggestions for final amendments.

Work-package 3: Training

The training undertaken included a short introductory course on the Technical management of ASIC projects, and dedicated one to one tutorial based training on DSP Station, VHDL, Architectural and Logic Synthesis and Digital Simulation for the company engineer. The hands on experience gained during the application experiment also included training in design for testability and ASIC Evaluation methods.

The company anticipated 50 person days effort for the training activities, but because of staff changes during the application experiment 71 person days were required.

Work-package 4: Design

The ASIC design was developed using a combination of high level DSP tools and VHDL. The task included the following activities:

- High level system description using DFL (Data Flow Language), and the architectural synthesis to the specified processor architecture to produce a VHDL description.
- Logic simulation performed on the architectural VHDL simulation to verify correct functionality.
- Translation of the VHDL architectural description to the RTL VHDL description the Viewlogic Office system in-house.
- Gate level VHDL descriptions were then generated using logic synthesis and the whole design simulated. From the results a net-list was generated using the target technology library.
- The net-list was passed to Delta for physical layout and routing.
- The post layout simulation to ensure correct timing performance.

The company's engineers were actively involved in the design phase, especially in the interpretation and analysis of the simulation results at each development stage. The company's engineers were also involved in the design of the prototype circuit boards to receive the ASIC device, and the test set up required to fully evaluate the component. The company anticipated 196 person days effort for the training activities, but staff changes meant that 239 person days were required.

The role of the subcontractor was to undertake the ASIC design process, using company engineering support as described, and to provide on the job training to the company's engineer, for example in providing VHDL test benches. This generation of VHDL and other descriptions, and layout information was the responsibility of the subcontractors.

Work-package 5: Evaluation

The prototype devices were evaluated, both independently and as part of the complete system, to determine their functionality and performance. Device testing included the use of the test vectors conducted by the silicon vendor, and using the dedicated fixture and system test designed to exercise the ASIC device. The final test process involved the testing of the prototype ASIC in the final system configuration.

The task required 83 person days effort, and was undertaken with minimal design subcontractor support. The resources required were greater than planned because of the under estimation of the time required to test all modes of device operation fully.

An indication of the actual work-plan is shown in Chart 1. The shaded vertical line indicates the time at which the company engineer left, and the restart of the training activity.

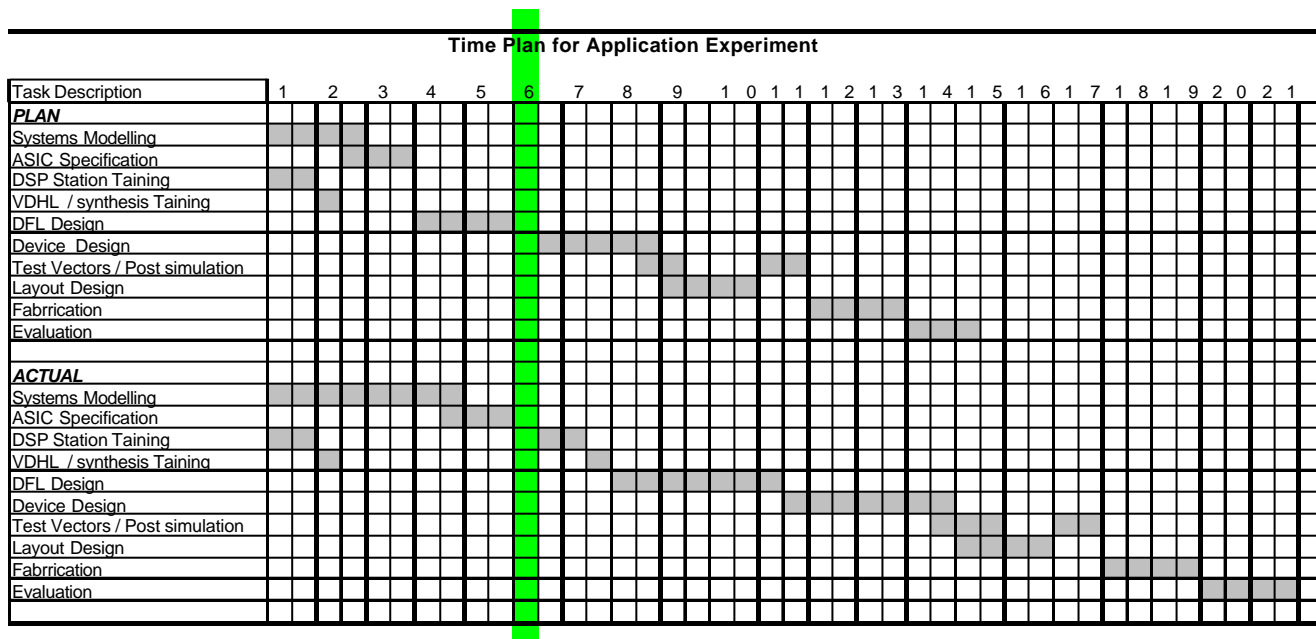


Chart 6.1 Actual and Planned work Schedule for the Application Experiment

The factors that lead to the overrun in the time schedule included:

- The largest affect was the loss of the design engineer halfway through the project. Not only did the training have to be repeated, but the lack of accumulated knowledge led to a slowing of the subsequent design tasks as the results of simulations were unfamiliar. This caused over 50% of the delay encountered.
- Additional time taken in the design modelling process, including analysing the audio processing system and the production of FPGA device prototypes for this function, led to a delay in this task completion. This stage required twice as long as required for the reasons previously described.
- The decision to incorporate the ADC and DAC functions into the ASIC yielded a significant product cost saving but required approximately 2 weeks additional effort to incorporate these functions during the design process.

- An additional design translation stage necessitated by design tool compatibility problems required two weeks delay prior to the layout stage.

The resources required to complete the application experiment are defined in Table 1.

The company identified several technical risks in undertaking the ASIC development. These included:

- Design specification errors and system design inaccuracies – this source of risk was addressed by the extensive system level modelling undertaken at the beginning of the AE, and the use of FPGA modelling of critical sections (such as the audio signal processing).
- ASIC design errors – These were minimised by the extensive use of simulation, and the use of real world data samples to prove functionality before committing to layout.
- ASIC fabrication or layout errors- This source of risk was addressed by using a MPW (multi-project wafer) fabrication facility. This minimised the cost exposure for this risk, and allowed recovery with a time delay of typically 3-4 months.

Task	Planned Effort of HNE (person days)	Actual Effort of HNE (person days)	Subcontractor costs (kECU)
Management	78	81	1.7
Training	50	71	8.2
Specification	70	80	12.0
Design	196	239	33.4
Fabrication	-	-	25.0
Evaluation	77	83	2.2
Total	471 days	554 days	82.5 kECU

Table 1. Actual and Planned Resources to Complete the Application Experiment.

10. Subcontractor information

Huntleigh Diagnostics considered a number of potential subcontracting options for the application experiment. The selection criteria required by the company for their subcontractor support included the following:

A local design house was preferred, not only to manage the technology transfer, but so that the company could liaise adequately with the subcontractor during the initial modelling and specification phase.

1. Expertise in the development of DSP solutions, and developing dedicated hardware solutions to implement these.
2. Flexibility in terms of technological solutions, including the ability to produce mixed signal IC's, in small volumes and with a fast turnaround of place & route and fabrication.
3. Access to a range of fabrication foundries, rather than being tied to just one.

4. The anticipation that a good working relationship between the various sub-contractors could exist.

Eight manufacturers were approached for prices and other details. Non-disclosure agreements were entered into before detailed block diagrams and provisional specifications were forwarded for tendering. The technologies, estimated gate counts, packaging options for the ASIC, the NRE and various other costs and parts costs were used to assist in the final selection.

Two subcontractors were selected; together the chosen vendors met all of the identified criteria. The parties selected also proved to have a good working relationship with each other.

The selected design subcontractor, CEPE, at the University of Glamorgan, were selected because of its previous experience in DSP algorithm development, proximity to the company, and their experiences in ASIC design. This design route allowed an optimum involvement by in the design process. It balanced the expertise of the company's product knowledge and of the requirement to gain experience, with the skills of the ASIC designer and the advice of the consultant on design tools and processes. It also allowed the use of the subcontractor's specialised design tools in order to reduce the investment costs required for the ASIC design.

The role of the design subcontractor was to be responsible for developing the ASIC from the Technical Specification through to producing working devices. Huntleigh Diagnostics' role was to perform the specification task, and to be involved in all of the design and simulation phases of the project, to develop the company's knowledge of the design process.

The ASIC supply subcontractor was selected after a lengthy evaluation, because the company offered the option of several final implementation technologies after the initial MPW run, and the ability to supply reasonably small volumes of ASIC devices (<10,000 units) in the initial periods of the product launch. The selected ASIC supplier subcontractor was Delta Electronics Testing.

Design Subcontractor Details:

Centre for Electronic Product Engineering
University of Glamorgan,
Llantwit Rd,
Treforest, Mid Glamorgan,
UK, CF37 1DL
Phone: +44 (0) 1443 482542

ASIC supply contractor:

Delta Electronics Testing
Venlighedsvej 4,
DK-2970,
Hoersholm,
Denmark.
Email : GJ@Delta.dk

Formal subcontracts were developed with both of the selected subcontractors. The subcontracts defined identified deliverables and values for these items. A development schedule was established in the design subcontracts and payment aligned to these. The IPR of the selected ASIC design implementation was allocated to the company free of charge under the contract terms and conditions.

The detailed role of the subcontractors for each work package is discussed in the previous section. There were no contractual disputes during the application experiment, and a good working relationship was maintained throughout the application experiment.

11. Barriers perceived by the company in the first use of the AE technology

Prior to the commencement of the AE there was a reasonably clear understanding within the company of the potential benefits that ASIC technologies could bring to bear on current and future product designs. These included the opportunity for increased functionality in reduced size, lower cost, reduced power consumption and inherently greater security from designs being copied by competitors.

Cultural barriers

Although the company had been used to investing capital sums in designs for plastic moulding tools it had no experience of similar levels of investment into electronic tooling of this type. This lack of experience together with the levels of complexity involved led to a significant resistance to investing in such technologies, because of the perceived risks involved. These led to a conservative approach and a reluctance to invest.

In preparing proposals for investment in ASICS there was a wealth of information available from a variety of vendors some of which were conflicting and led to greater confusion on our part.

In addition to the above there was no significant levels of 'in house' knowledge on the details of implementing an ASIC except that some of the engineers had previous experience from earlier career experiences. Their knowledge was significantly out of date .

Knowledge and Technology barriers

As stated above there was no directly relevant expertise within the company and this lack of knowledge led to a belief that the skills required would present a significant barrier in both requiring new personnel and management of such personnel. Additionally the tools required were not available in house and these presented further barriers in both investment and learning the new skills. These combined barriers highlighted the risks to be resolved in acquiring the technology.

Financial Risk Barriers

From the above there can be seen to be significant financial risk barriers. These can be summarised as cost of investment in tools, cost of personnel with relevant skills if sourced from outside the company and the investment costs of tooling and layout design.

12. Steps taken to overcome the barriers and arrive at an improved product

In order that the cultural and knowledge barriers could be more precisely understood, the initial step in considering ASIC technology was adopted. A final year MSc student at a local university was sponsored to carry out the initial research work as the basis for his project. This led to detailed investigations into our current product range and a clear identification of the potential benefits and costs associated with investing in ASIC technologies. This project concluded with a presentation to senior management and allowed in depth discussions of the potential benefits and pitfalls of the areas researched. In this way senior management was made more familiar with the whole area and they then felt more comfortable with authorising additional expenditure. This lowered the cultural barriers to considering the technology.

The student who had carried out the project was eventually employed by the company on a full time basis, and therefore some of the skills required were brought in house without having to support the salary levels of an experienced designer. As part of the student's project there also grew a working relationship with the university and a familiarity with their skills base and approach to a commercial organisation. This was invaluable in helping deal with the barriers outlined above. In particular it reduced the level of risk perceived to overcome the cultural barrier, and highlighted the economic benefits to help overcome the economic barriers faced by the company.

The financial risk barrier was quantified through these actions, and the quantified benefits and FUSE subcontractor and TTN support mechanisms meant that the company considered the financial risk barrier to have been lowered to an acceptable level.

The knowledge barrier was addressed by start up training, and on the job training provided at the local subcontractor's site by the design sub-contractor. This knowledge barrier was largely eliminated when new barriers occurred during the implementation phase of the AE. These barriers were related to the fact that this key development engineer left the company approximately half way through the project. This led to significant delays and the need to re-assign the tasks to another engineer. This in turn led to difficulties in that the training phases of the project had already been undertaken by the departing engineer and there remained very limited opportunities to re-train the new engineer.

As previously explained the original engineer allocated to the project had some exposure to ASIC technology and economic evaluation before undertaking the AE, extensive training in ASIC design methodologies, and more importantly, an extensive knowledge of the vocabulary and technology that had removed any fear of the technology. The new engineer had none of this experience and therefore was faced with a new set of barriers. These included:

1. A lack of familiarisation with the technical specification for the ASIC. The previous engineer had been responsible for acquiring realistic test data, performing high level design implementation simulations using this data, and was partially responsible for the specification of the device. This experience had to be re-acquired from a lower starting base and required additional time and subcontractor training for the knowledge to be re-established.
2. No previous exposure to the CAD systems used for the design process. There was a significant barrier in coming into a project where several designs using the HDL design method, synthesis and simulation tools were productively being applied and yet the engineer had no knowledge of these. Training was required to overcome these. This also required additional time.
3. A higher level of in-experience led to higher psychological barriers in attempting the technology familiarisation process. Additional sub-contractor guidance was required to overcome the start up process for the new engineer.

In addition, the company faced a high level of effort in defining the detail and investigation put into design compromises for the technical specification. These knowledge barriers were overcome during the implementation phase. For example, there was much effort put into trying to absorb some complex analogue processing onto the device. This was modelled using FPGAs and realised that the performance level required would significantly add to the complexity and gate count of the ASIC.

13. 12 Knowledge and experience acquired

The project allowed the company to build on its already detailed understanding of microcontrollers and DSP devices in the programmable and semi-custom device arena, which previously it had never used. During the course of the experiment PGA and PLD technologies were used to simulate parts of the device and this experience was directly put to use in other product development.

The company established as goals for its knowledge development at the end of the application experiment the following capabilities:

- Detailed specification for a complex ASIC device
- Project planning and management for this type of technology
- Capabilities and limitations of the various consultancy/sub-contractors and the elements of expertise they could bring to bear on such a project
- A thorough understanding of the processes that have to be undertaken in developing an ASIC
- An ability to use relevant CAD tools for circuit simulation and testing, programming PLD and similar devices
- Testing of ASICS and setting up appropriate test environments

All of these objectives were achieved, even allowing for the departure of the original design engineer.

At the end of the application experiment the company is capable of managing further digital ASIC designs, and implementing high-level digital design solutions for FPGA devices. A future ASIC project would still require design support from a specialist ASIC supplier, but the company could provide a much higher design contribution, possibly to an FPGA prototype. The abilities and experience gained will continue to influence key decisions on technology opportunities as they arise in new product developments, and now that we have successfully completed a complex ASIC implementation we will be less reluctant to follow this path again.

14. Lessons learned

There were many lessons learned during the course of this experiment. Advice to other first users of ASIC technology may be summarised as followed:

- Try and duplicate the skill base in personnel when learning new technologies so that key knowledge is not embodied in one person. Whilst in a small company this will be very difficult to achieve the impact of losing acquired knowledge in a new technology area can have a significant impact on the time scale required to complete the ASIC design.
- The original system design phase considered the implementation of a phase processing algorithm in the digital ASIC device. The design and performance evaluations using FPGA device technology resulted in a highly complex digital algorithm to emulate the performance obtained using a two operational amplifier solution over the required bandwidth. In this case it was cost effective and more efficient to implement the design using discrete analogue components external to the ASIC. This has therefore led to the important lesson that one should not always assume that a digital custom silicon design implementation is more optimal than a discrete analogue solution.

- Devote as much effort as possible in specifying requirements at the outset. This led to our achieving a better understanding of the current products and helped in both minimising changes and managing those that became necessary. Specification of the functional requirements was the key to the right first time implementation.
- The pace of technology changes often outstrips original expectations and this can have great benefits on a project in our case allowing more functions to be incorporated for the same costs and timescales. In undertaking ASIC designs, the trends of device / process minimisation is significant, and if a lengthy period of time occurs before internal project sign off and the design, then the technology implementation should be reviewed to ensure new design options are available.
- A detailed plan is essential especially when working with multiple sub-contractors split by diverse geographical area so that all concerned can easily recognise the importance of their input and its interaction with others
- The less well known a sub-contractor is then the more detailed a contractual basis of working is required, especially when they are based in a far away location when resolution of differences becomes more difficult. The company had not previously undertaken an ASIC design, so the process of developing the sub-contract required a lengthy period of consideration, and the development of a common understanding over this period with the selected sub-contractor.
- When entering detailed contracts with a sub-contractor make sure all the elements are covered and the wording is correct. It took several attempts for us to get the contract correct, in the first versions we would have given away all our intellectual property rights. Detailed review of the terms and conditions should be undertaken, and if necessary advice sought from other experienced parties sought to provide the guidance required.

15. Resulting product, its industrialisation and internal replication

The prototype ASIC device has been fully evaluated, and is operational. The prototype system developed to enable evaluation of the ASIC, will be further developed into a fully portable handheld device for user evaluation. To realise the portable instrument the following tasks will be conducted (with timings from the end of the application experiment in parentheses):

1. Microcontroller software development (months 2-9) for improved display and ASIC interfacing.
2. The integration of higher performance transducers (months 1-3)
3. New Circuit board design (month 4-5)
4. New moulding designs for the unit's case (month 6-8)
5. Regulatory approvals procedures - EMC, safety and related Technical File creation (months 10-11)
6. User Evaluations and design amendments for the system (months 10-12).

As indicated the total elapsed time for industrialisation is approximately one year. The costs of industrialisation were approximately 5 person years (150 KECU).

Additionally the facilities the ASIC provides means that the FU has the opportunity to market the ASIC and its IPR for non-competing applications. The IPR for the ASIC design lays completely with the company and allows the company to freely market the device as a product in its own right.

The signal processing algorithms embedded in the ASIC can be applied in several vascular application products, and other product developments have already been identified. The development of CPLD designs for integration into other new products that have already been launched is one such example.

16. Economic impact and improvement in competitive position

The increased sophistication resulting from the improved ASIC based product has not previously been seen in portable battery powered devices for the vascular monitoring market. The potential opportunities therefore, lead to the possibilities of blurring the distinction between portable and desktop devices in this section of the marketplace.

The improved product, incorporating a graphics display, will open up more clinically accepted measurement practises only available using current products in the high cost instrument sector. This will allow performance levels to be achieved in a portable unit previously only available to the market in expensive large, desktop systems. This will allow us to aggressively market the product providing the user with the advantages of significant cost / performance improvements and portability. It is also anticipated that this will, in turn, lead to an increase in market size in terms of number of units.

Further economic benefits will be derived from the reduction in the number of components required to realise such systems. This simplifies part procurement, and the availability of the ASIC has already by-passed at least one obsolete component. In the most complex product component costs will be cut to approximately 65% of the current component costs.

Without improvement the company anticipates a gradual decrease in the market value of the products sold in the forthcoming years. This is illustrated in Figure 16.1. In addition, the margins obtained on the products will decrease to approximately 60% of 1995 levels by 2000 because of the increasing levels of competition faced by the product from similar designs produced by the followers in the company's market.

Not only will the ASIC development result in a reversal of the sales decline by the additional functionality provided and the new market opportunities offered, but the margins obtained on the product will be improved as a result of cost benefits previously identified.

The total FUSE application experiment cost figures totalled 174kECU. The projected payback period is approximately one year from date of product launch. The ROI (return on investment) is estimated to be 340% over the product life of 4 years before further enhancements will be required.

The final inherent advantage of the ASIC technology is that it makes it difficult to copy the company's design. This has reduced the threat of 'reverse engineering' and will allow the company to maintain its leading edge over its main competitors, based in the United States and Far East.

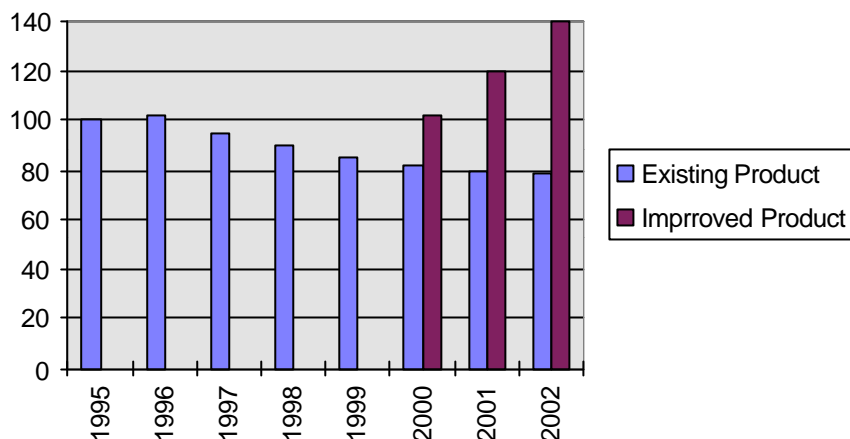


Figure 16.1 Sales Revenue for Existing and Improved Product (normalised to 1995 figures).

17. Target audience for dissemination throughout Europe

The trend towards small, lightweight, complex but simple to use instrumentation affects many sectors of industry. This demonstrator document is therefore considered to be of value to companies considering methods to produce lower cost, but more complex and smaller portable products. The application experiment also demonstrates the application of complex Digital Signal Processing algorithms in this scenario.

The target audience therefore, includes the managing directors, technical managers and decision makers in small to medium sized companies operating where these trends exist. The target industry sector includes companies operating in the following industrial sectors:

Medical and Surgical Equipment – Prodcom code 3310

Instrumentation Equipment - Prodcom Code 3320

Computing applications, involving DSP methods - Prodcom code 3002

Typical companies would include those involved in portable analysis equipment, for example companies involved in water analysis equipment manufacture, or companies producing portable health monitoring equipment such as monitors for heart functions.

Best practice information includes (i) the utilisation of higher level DFL design methods to produce a behavioural model of the device and the benefits this provided in delivering a ‘right first time’ design, (ii) the use of real world data to validate the design solution, and (ii) the role of continuous design evaluations to ensure cost effective design solutions.