

FUSE DEMONSTRATOR DOCUMENT

AE25907

A Shooting Target Control System

FPGA technology reduces product costs and increases flexibility

Company: Militec Ltd

TTN: University of Glamorgan Commercial Services (UGCS) Ltd

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Abstract

Militec Ltd designs and manufactures target equipment for rifle and pistol ranges for both national and international customers such as the police, Special Forces, military, recreation and sports users. Militec's turnover is about 350 KECU, and the company employs 4 people, including one electronics engineer and one electronics technician.

The existing system's electronic circuitry utilised discrete components, resulting in three circuit boards inter-linked in order to fit within the size constraints of the enclosure, thus making the unit expensive to manufacture and to modify to individual customers requirements.

The aim of the experiment was to improve the existing Turning Target and Pop-up target products by introducing FPGA technology to replace the bulk of the existing electronics and enhance its capabilities. Both of the products utilise the same circuitry, except for a few small logic modifications. The objectives of this experiment were to improve the existing products, and to ensure that knowledge was transferred to the company in the following areas; technical management, top-down design methodologies (including VHDL, digital simulation and synthesis), selection of FPGAs, test techniques, and modern CAD tools for digital design.

Meeting these objectives has enabled the company to utilise this flexible technology not only for the products involved in the AE, but also for future products, providing a means of competing more strongly in the market place. In fact work has already started on other products utilising the knowledge gained through the application experiment. Improvements achieved include:

- Large reductions in the component count, number of PCBs, PCB area and power consumption.
- Cost savings in labour, manufacturing and test of up to 31%.
- More reliable and versatile products.
- Economic benefits allowing larger sales to be achieved and new markets to be exploited.
- Feature improvements
 - ◆ Improved display, making the unit more user friendly.
 - ◆ Adding more programmable target reactions.
 - ◆ Flexibility to use various data formats.
 - ◆ Generation of a 'trigger out' signal after programmed target action and present number of hits sensed.
 - ◆ Self-checking diagnostics
- Single board stocked for most products.
- Increased commercial security.

The prototype development costs of 48 KECU which were entirely funded by the FUSE programme will improve company sales, resulting in a payback period of 8 months and a ROI of 882% over the 6 year design life of the product.

The duration of the application experiment was 7 months. The application experiment took approximately 1 month longer than envisaged to complete because of RF interference effects in the RF communications system. Fortunately the re-programmable nature of the FPGA device allowed improved digital protocols to be implemented to solve the problem. This flexibility demonstrated the significant technical benefits achieved by adopting FPGA device technology.

Keywords and Signature:

Target control; Remote control; Shooting; FPGA; Military Equipment

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1. Company name and address

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2. Company size

The company employs 4 people. Sales turn-over is approximately 350 KECU.

3. Company business description

Militec Ltd designs, manufactures and markets Target Systems for the target shooting market. The main customer base consists of supplying equipment to the police, Special Forces and military users, normally selling directly to the end user. User sites vary a great deal and on-site commissioning and servicing are also a part of the business. For this reason it was considered important that the FPGA development should be able to be applied retrospectively to existing products in the field.

Manufacturing is partly in-house and partly by outsourcing sub-assemblies or buying sub-systems.

The company only manufactures target-shooting systems. The product range includes moving, pop up, multiple target, and air rifle target controllers.

4. Company markets and competitive position at the start of the AE

The major activity of Militec is the design and supply of Shooting Range Target equipment for customers such as the police, Special Forces and military users. The company's major market is in the UK, but the company has developed sales to customers in the Middle East, Europe, and the USA.

The shooting target market can be categorised into 3 main application areas:

1. Electronic Firing Ranges, including in turn
 - Tank Target Systems
 - Scoring Systems
 - Shooting Ranges
2. Mechanically operated firing ranges.
3. Laser Firing Ranges

Militec supply equipment for the electronic shooting range market sector only.

Electronically operated firing ranges are slowly growing in number. The ratio of electronic to mechanically operated shooting ranges is approximately 1.5: 1. However, the number of

electronically controlled ranges in the USA generally exceeds that for mechanically operated systems by 4:1.

The UK market for shooting targets is segmented into the following major categories; Militec's market share for each is also indicated:

- Police Forces 70%
- Civilian & Air Weapons 40%
- Military 10%

With most major military countries reducing their military spending, the market has become increasingly more competitive between equipment manufacturers. The sales of shooting targets in the UK market have become static.

Competition in the target shooting system market is provided by small divisions of a few multi-national companies such as Saab and Lockheed Martin, and many smaller companies such as ADI, Tyson, Caswell, Shield and Polytronic. It is not possible to estimate the exact market share of these competitors in the shooting target market because:

- Many of the sales are highly confidential in nature, and the value and supplier for some contracts are not disclosed.
- All companies compete on a world wide basis, providing a highly complex market position that rapidly changes with the awards of military or police contracts in these regions.
- The structure of the competitors, including small divisions in multinational organisations, means that sales levels cannot be directly estimated.

Most competing products use discrete device technology in their products (although in some cases the handsets supplied with the products may include a microcontroller device). Many of these competing products are mature products based on old designs. The product features offered by competitors are generally related to the provision of common features, and there is little functionality differentiation.

Market advantage is in some cases related to the company's reputation or linkages to other products supplied by that company, and to a lesser extent cost. The larger multi-national companies therefore, enjoy a marketing advantage because of the perceived reputation of these companies.

The product price range for a typical target controller varies considerably depending upon the purchase methods, routes to market (intermediaries etc.), and specifications required. The general price range is 1 KECU to 4 KECU.

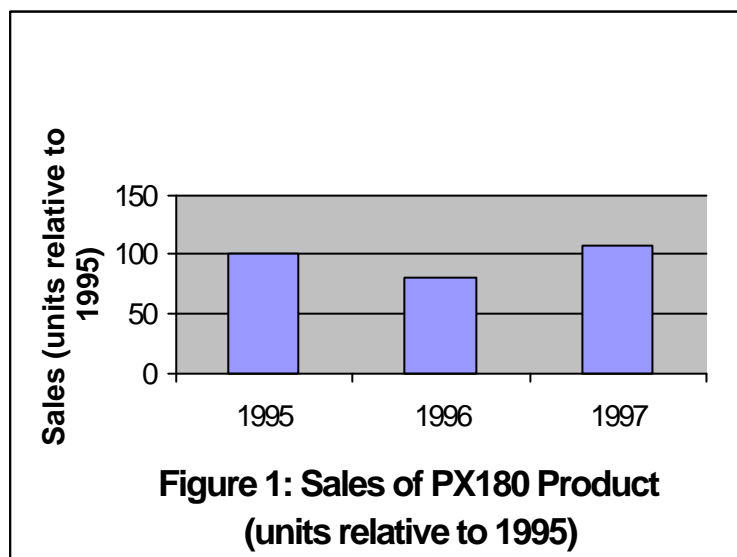
Militec's assessment of its product's cost competitiveness is that the company's products are not the lowest cost available but that the product's cost is towards the low end of the market competitors. Feedback from overseas customers and agents indicate that Militec Ltd equipment performs very well and is in advance of most of its competitors.

The major competitive advantage offered by the company is its responsiveness to customer enquiries, and the ability to supply products at relatively short notice.

Analysis of the export markets for the company indicates that there is a growing world-wide demand for the training of armed personnel involved in the security business. The company has also

identified the USA market as a growth area. A number of Target Systems have been sold by the company to the US Marines and the FBI, who have given favourable reports on the performance of the system, but the unit cost has restricted further penetration into the US market. The US market is vast, including; Special Forces, Marines, FBI, National Guard, Railway Security, Forest Rangers, various Police Forces who all having firearms and requiring training. Therefore, for the company to increase its world-wide share, the company has determined that it should increase its cost competitiveness and further improve its responsiveness to customer enquiries.

The aim of the experiment was to achieve cost savings by the introduction of new technology into it's the PX 180 product, and thence into all of the current product range, and to achieve the decrease in time to market required to enable improved delivery schedules. The substantial reduction in the manufacturing cost achievable through the adoption of FPGA technology will enable the company to offer target equipment at very competitive prices, not only in the USA, but also on a world-wide basis. The reduction in lead-time for design modifications and the ability to implement changes in the field will therefore, improve the competitive position of the company. The sales of the PX180 product over the past 3 years are indicated in relative terms in Figure 1.



5. Product to be improved and the reasons to innovate

The PX180 Turning Target system is a shooting target controller produced by Militec Ltd. The system consists of two units: a radio handset transmitter unit from which the user issues commands and the main unit that receives and decodes them. The main unit has a motor that turns or flips up the target mechanism to present one of the two faces of the target to the user.

The radio transmitter unit issues the following commands: present A face, present B face, hide target, set target display time, set target hide time and activate external device. Fig. 2 shows the functional blocks of the radio handset. The keypad commands are read and then encoded before being transmitted to the main unit. The encoder unit is a proprietary unit and to interface successfully to this unit the system uses analogue, discrete components to convert the keypad entries into appropriate analogue signals to the encoder.

The block diagram for the main unit to be improved by the use of FPGA devices is shown in Fig. 3,. The unit is currently implemented using standard discrete logic devices where possible, although the

decoder unit is implemented using analogue devices to interface to the proprietary radio receiver unit. The main unit requires 3 PCBs, of which there are variants for individual customers' requirements.

The main unit has detects target hits using external vibration sensors. This input is used to trigger a hit reaction event in the product. This event is programmable, and the reaction is pre-set within the unit, e.g. hide target, or using an external adapter unit, illuminate a lamp.

The radio receiver and modem interface includes a decoding facility for the 6 possible key presses that are transmitted by the handset. The unit operates in the following sequence: the target is set (i.e. presented to the user) by either a key press of the handset or by an external trigger signal. The trigger input is typically provided by the use of a pressure mat to detect that the user is in the firing position. Thereafter, the system operates a motor to either flip a target up, or turn a target through 90°. When the target is subsequently hit, the motor is activated to return the target to its original position. The actual motor position is fed back to the control logic via a sensor.

The line control input allows the system to be operated manually via mechanical means, and this input disables the radio control system.

The motor control logic latches the relays to supply the motor current. The motor is switched on until the position sensor input is detected, and reversed to return the target back to its initial position. A low battery cut-out circuit is also provided in this functional block.

The product is based on the use of discrete devices only. The digital functions were implemented using standard 4000 series CMOS devices, including flip flops, gates and shift registers.

6. The disadvantages of the current implementation are:

- Large number of discrete components which require 3 PCB boards and interconnections.
- Expensive to manufacture, requiring a high level of pcb assembly and interconnection wiring effort. The reduction in assembly effort by 50% is anticipated by moving to a single board solution.
- Hardware modifications are required for different variants of the unit, these are expensive to implement and the sub-assembly of each unit has had to be separately held in stock. Variants of the unit have included the following features; mains/battery powered, internal/external batteries, lamp output, external triggering, integral hit functions and different radio codes.
- Difficult to change data formats in radio system.
- Lack of flexibility to add extra features.

The discrete device implementation therefore, impeded the ability of the company to improve its cost competitiveness in the market and causes time to market response problems when special requirements are placed on an order. The objective of the application experiment is therefore to improve the competitiveness of the product by reducing its cost and producing a more flexible design implementation.

No specific functional or parameter performance enhancements were identified for the existing product design as essential for the product, although as is identified in the next section some additional product features were included.

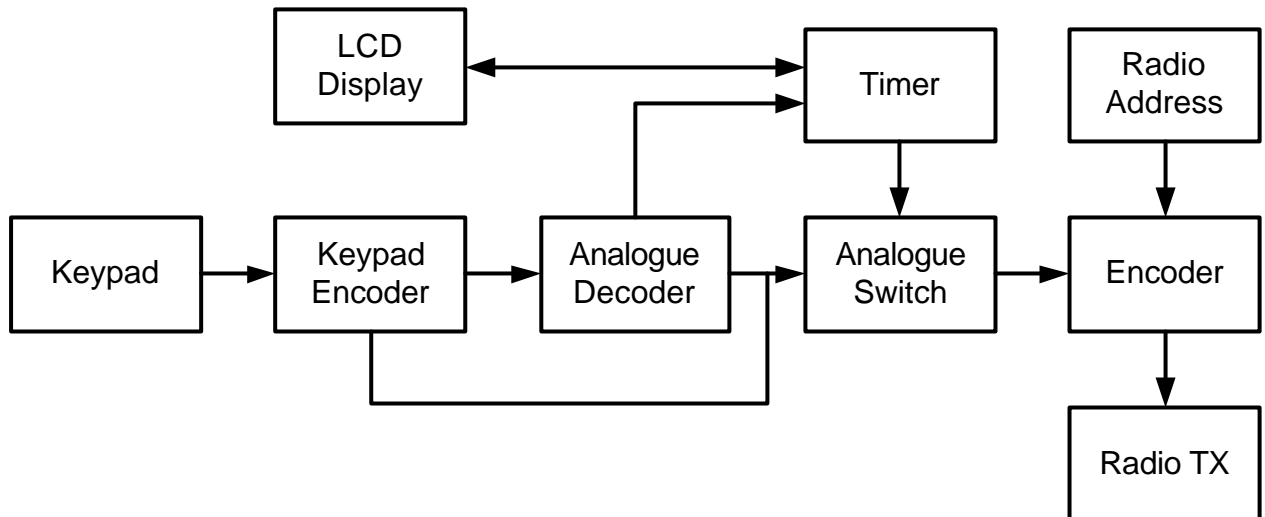
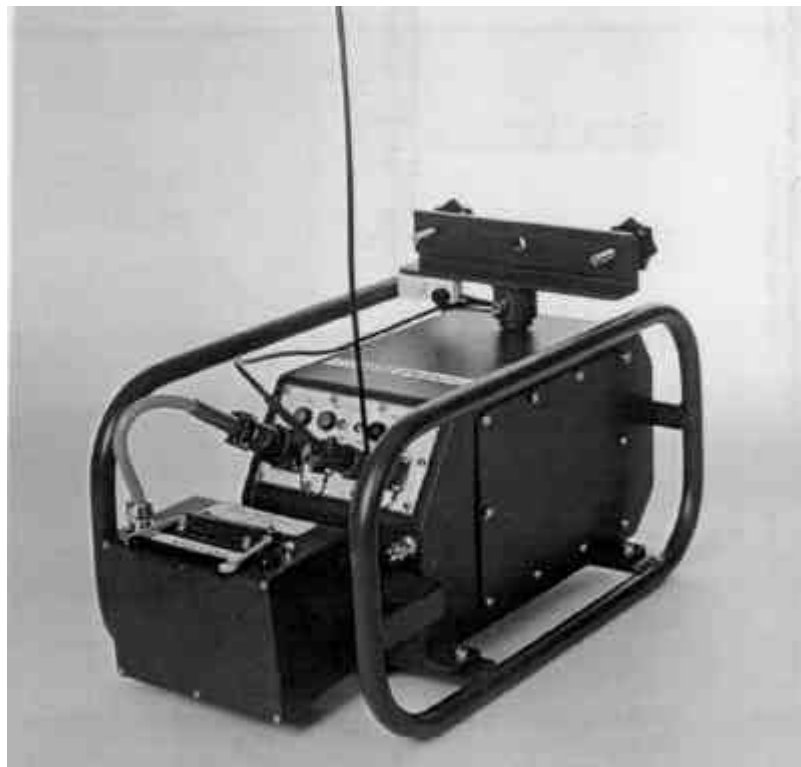


Fig.2 Radio Transmitter Handset



Photograph 1: The Existing Product

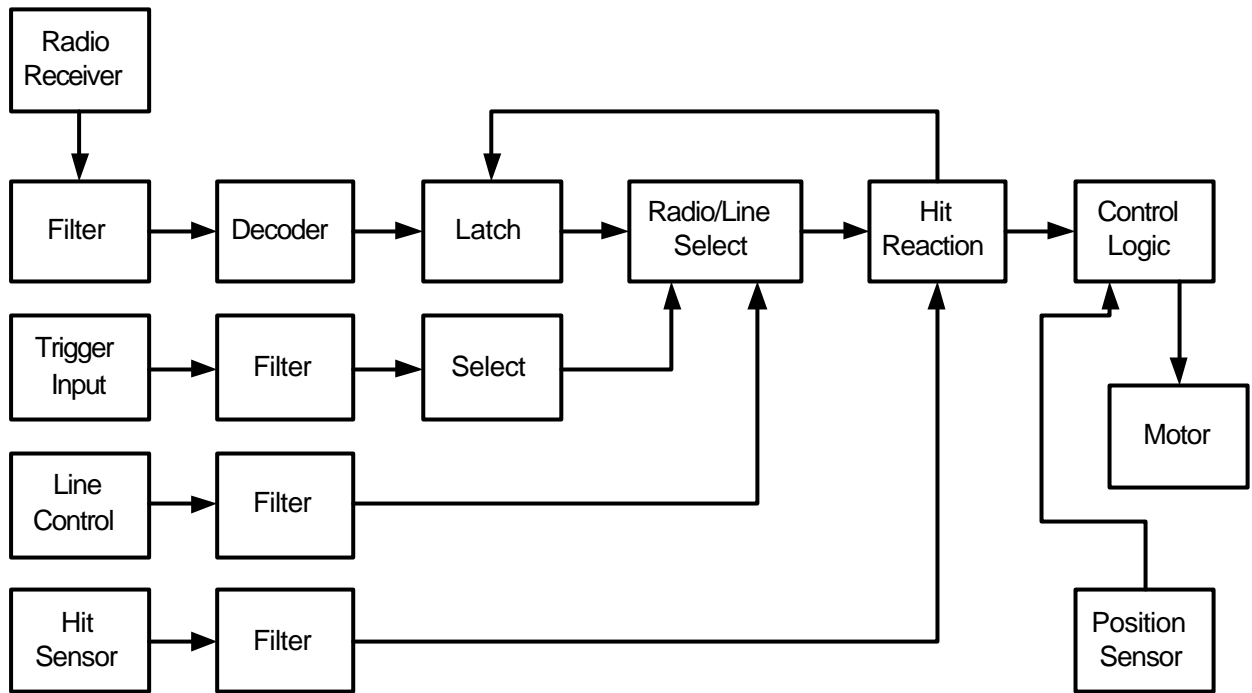


Fig. 3 Existing Product



Photograph 2: Existing Product Circuit Boards (3)

7. Description of the product improvements

The aim of this application experiment was to utilise FPGA technology to improve the main unit. The proposed improvements resulted in the integration of the discrete logic of the base unit into a single FPGA device. The base unit functions included within the FPGA are shown in Fig. 4.

Both the handset and the base unit are currently implemented with standard discrete integrated circuits (ICs) and passive components. The base unit currently requires 3 PCBs, the benefits of integrating these on to a single PCB are as follows:

- Significant reduction in the cost and size of the system (as illustrated in photographs 2 and 3).
- Large reduction in costs of assembly, soldering, inspection and test. This is estimated to be 50% of the previous costs of assembly.
- A single PCB will cover all variants of the design, hence fewer need to be kept in stock.
- A reduction in Electro-Magnetic Compatibility (EMC) related problems due to the reduction in the number of components, PCB tracks and interconnections. On average a reduction of over 20 dB in emission levels were achieved.
- Elimination of large amount of interconnecting cables.
- Inherently improved reliability through integration and simplification of manufacture.

Using FPGA technology within the main unit will allow Militec Ltd to have a single base unit PCB, which can serve several applications and different customer requirements. The different requirements can quickly and cheaply be implemented, without the need for PCB or component changes. To make these changes, it is just a matter of programming the FPGA with different configuration files. With the existing product, different applications require different PCB assemblies, thus resulting in multiple versions of the unit in stock, and the development costs incurred for each variant.

Functional enhancements in the improved FPGA-based turning target include:

- Extended decoding in the main unit to enable an improved range of user input via a keypad, extending the effective number of keypad entries to 20 key presses from the original 6.
- Provide the potential to return hit statistics to the hand set unit using the Radio transceiver's capabilities. The return of information to the handset is a new user feature.
- Incorporating a selectable trigger out signal to control external devices such as other targets and sound effects. The output control is 12 volt relay compatible.
- Improved target hit sensors, based on the use of foil targets, to provide 'kill' and 'wounded' information to the controller, and to influence the target reaction and update the target statistics accordingly. This is a new product feature.
- Inclusion of a 'realism' mode, which will randomly display the target, while retaining range safety. This includes the controlled provision of up/down and turn movements of the target (amalgamation of pop-up and turn into one unit).
- Self-Checking diagnostic circuitry to ensure satisfactory operation on power-up and at regular intervals during normal operation, enhancing range safety.

In addition the FPGA re-configurability will allow the use of alternative data format interfaces, enabling the unit to be utilised along-side existing in-service equipment with the incorporation of suitable interface circuitry in the FPGA.

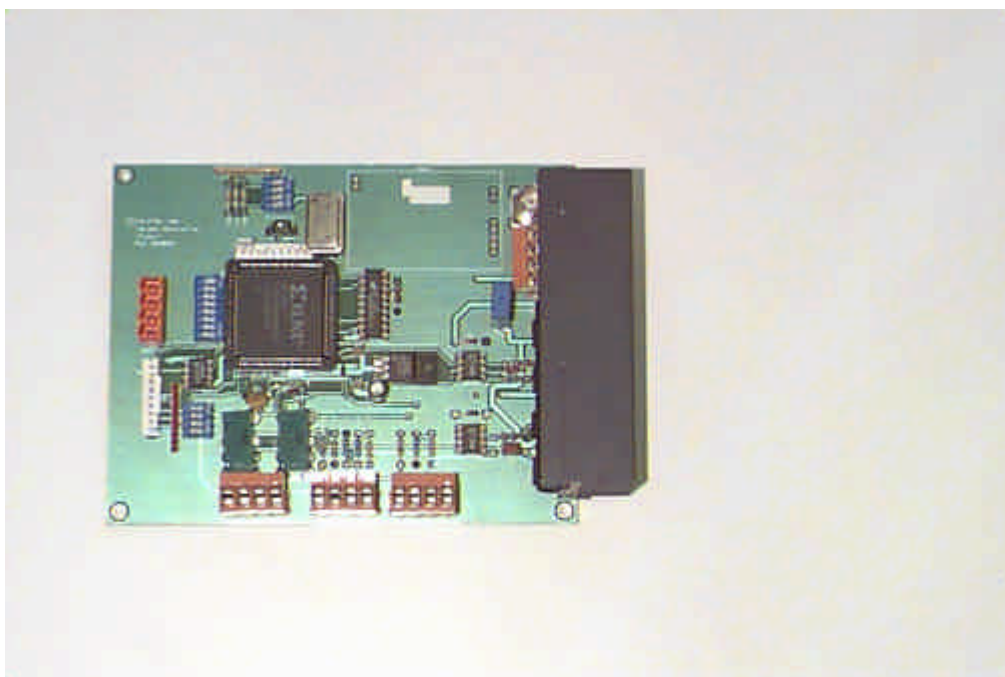
The functional block diagram of the main control unit is similar to that of Figure 3 for the existing product, with the exception of:

- a) A counter to record the time of hit and number of hits, and the control to return this information via a transceiver to the remote handset.
- b) The incorporation of a control facility for the trigger output control previously provided by external equipment.

The original unit utilised 20 discrete 4000 series CMOS devices (mostly flip flops, quad gate packages, and shift registers) and a driver while the FPGA version has 1 FPGA and 2 others. The FPGA device employed was an 84 pin device, operating at a 5 MHz. clock speed, and incorporating approximately 5,000 gates. The enhanced functionality would have required the addition of about 7 more logic chips, however due to size limitation piggy-backing the boards would have been the only viable solution with potential reduction in reliability.

As has been shown during this project the cycle time for a new variant has been reduced from typically two / three months down to one month and could have utilised the existing PCB, making greater economic savings and the option of upgrading existing customer units viable.

The ability to customise the unit to customers requirements with out having to go through a full redesign will enhance the ability to deliver to the customers' requirements in a shorter time scale and at reduced costs and will provide competitive advantage.



Photograph 3: Improved Product Circuit Board (1)

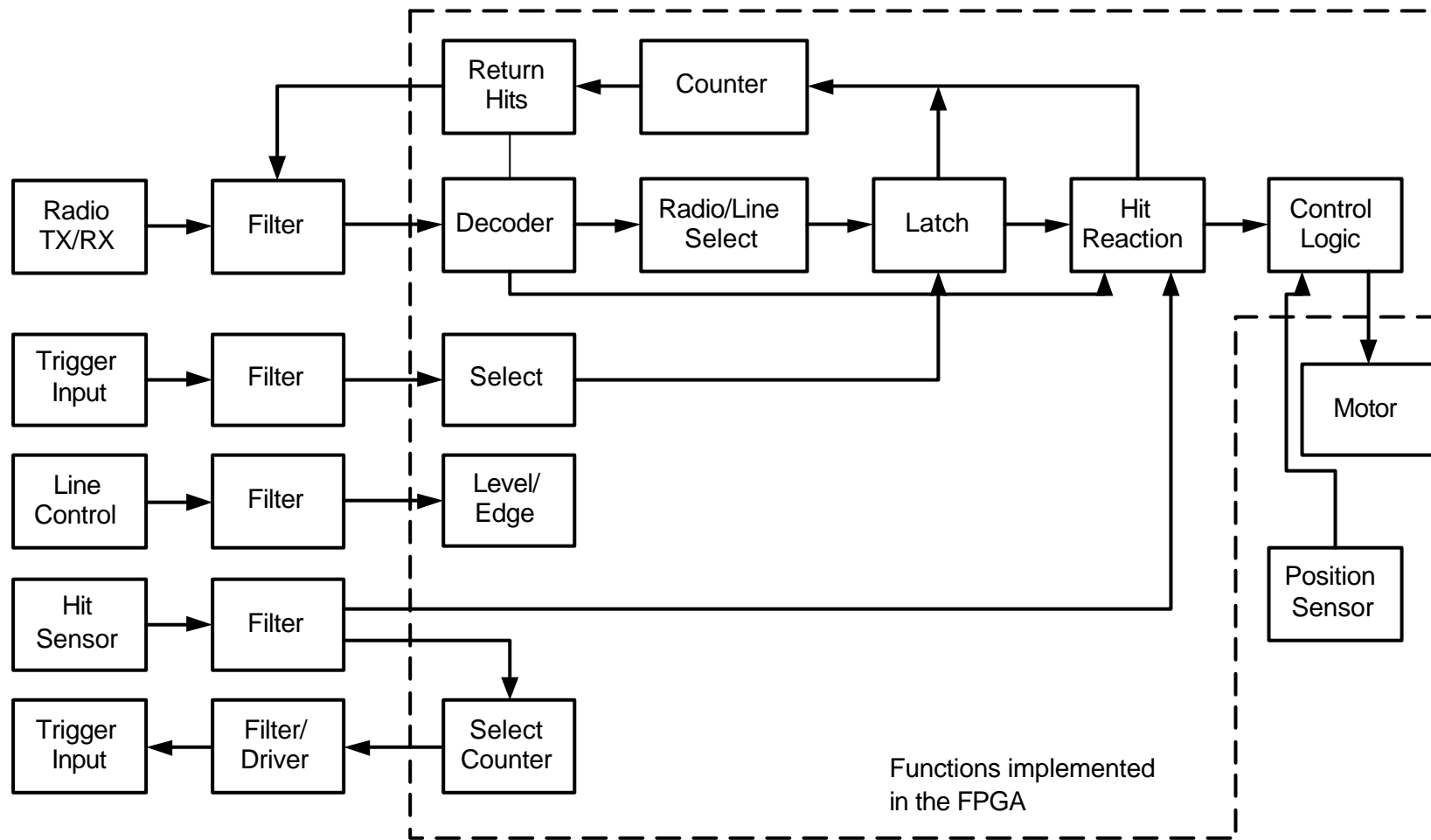


Fig. 4 Improved Product

8. Choice of rationale for the selected technologies, tools and methodologies

8.1 Technology

Several technology options were investigated in the search to improve the main unit of the existing Turning Target product. These included: microprocessor/microcontroller, complex programmable logic device (CPLD), field programmable gate array (FPGA) and application specific integrated circuit (ASIC).

A summary of the circuit requirements is:

- Decoding the received data.
- Interfacing and filtering for external trigger inputs.
- Detecting a hit and producing a programmable reaction to a hit.
- Reading a keypad and displaying the unit's status on LED's.
- Provide low battery cutout protection.
- Motor control and position sensing (this includes monostables to set the time the target is shown to the user).

FPGA technology offers the only suitable option for implementing the digital section of the main unit, given the low volumes and the need to be able to vary the specification. FPGA technology will provide Militec Ltd the required flexibility to modify the design of the product to suit different applications and ensures a low risk approach in designing with microelectronics. The low sales volume of the Turning Target also makes FPGA the best choice of technology.

Microprocessor and microcontroller technologies were considered, but were not suitable for implementing the logic required for many reasons;

1. There are a large number of inputs and outputs required for the improved product. These are needed for the keypad, display, trigger and line inputs, hit sensors and the trigger outputs, motor sensor and drive.
2. The three timers/counters are operating in parallel. Most microprocessors and microcontrollers only have two timers that can operate in parallel.
3. There is the need to process long chains of serial data, from the radio interface. The chain contains both the address and the data for each unit, and needs to be decoded.
4. The sensed hit signal must be loaded in parallel into the hit reaction and select counter circuits.

CPLDs are primarily designed for applications that require both relatively high operational speeds and require mainly combinational logic. As the design requires many registers, this approach was deemed to be unsuitable.

A digital ASIC option was a possible solution on purely technology grounds, a single digital ASIC can implement all the current and additional features required. However, this option removes the flexibility to make modifications to the design. Also the low number of units sold made this approach economically unjustifiable.

8.2 Design Methodology

The main FPGA technologies available in the market are one-time programmable devices, which are usually based on auto-fuse technology, and reconfigurable devices that are based on SRAM cells. The latter is usually configured at power-up from a memory device located on the same board. As there will be many customer-specified features required for each unit manufactured, it was decided the best approach would be to use a reconfigurable FPGA technology. This would also allow the company to program the FPGA device in-circuit, improving the flexibility of the design further

An important reason for selecting FPGA technology for this application experiment was the low risk involved in the development process. Any errors or design iterations were very low cost, this cost being the designer's time and the reprogramming of an EPROM. Militec Ltd felt that it was essential to resort to a low risk strategy in its first attempt at integrating the electronic circuits of the product. The experience gained would allow the company to consider technological solutions with higher risks in the future.

The functional specification of the improved product was generated first, a process of developing detailed technical specifications of each block of the system then followed this. The design methodology for the FPGA followed a top-down design approach using modern design capture and synthesis tools.

The PC-based FPGA development system used in the application experiment was a low cost development tool supplied by the device supplier, and this system incorporated all of the necessary design capture, simulation, and synthesis requirements.

The design system accepted design entry using schematics and VHDL. In addition, it had a macro generator to synthesise the most common logic blocks. The design was partitioned into functional blocks and the top-level schematic was entered. The functional blocks that represented standard functions such as registers and counters were realised using the macro generator. VHDL was used to specify the other functional blocks including the state machines and other control circuitry. Functional simulation was performed on each block and then the whole system.

The system was then synthesised and further simulation was carried out when the simulation matched the specification. The design netlist was then written. The FPGA was then placed and routed. This stage can be repeated readily within the constraints of speed and device utilisation. The routed FPGA was then re-simulated to discover any timing problems. Subsequently a design iteration was found to be required. The resultant bitstream file was then either downloaded into the FPGA in-circuit, or by re-programming a serial EPROM that was read by the FPGA on power-up.

9. Expertise and experience in microelectronics

Militec Ltd designs and manufactures Target Systems for the target shooting market. The company has developed expertise and skills in the areas of mechanical, electrical and electronic engineering.

Electronic design experience has hitherto utilised only standard electronic components for analogue and digital electronic systems. The products that have digital sections have been designed using standard CMOS logic parts. The company had not had any experience in designing FPGA-based designs. The company also had no experience of any modern CAD tools including: schematic capture, VHDL, simulation and synthesis.

There are 4 people in the company, one management, one mechanical, one an electronic engineer and one electronic technician.

The personnel allocated to the application experiment were the electronic design engineer and the technician engineer. The electronic engineer had no previous FPGA or high level digital systems design experience. He was qualified to degree level, and had 6 years design experience at the discrete device level. The technician engineer, qualified to technician level, had 8 years experience in commissioning and fault finding discrete device systems.

10. Workplan and rationale

The workplan followed by Militec consisted of the following tasks. The underlying rationale was that the reputation of the company was in no small part due to its engineering design competence. It was therefore essential that the knowledge and skills transfer should be effected thoroughly, with a view to internal replication without the need for external technical support.

Training

This task required the design engineer to attend 2 courses addressing top-down design methods and FPGA technologies, and the use of CAD development tools for FPGA design. The outcome of this task was to establish a theoretical FPGA design capability within Militec.

The subcontractor provided training in top-down design methods, together with a structured approach to digital design, formal VHDL training and the required coding style for FPGA implementations. Training also included a detailed explanation of the CAD tools required to implement the FPGA, and an introduction into the test methodology required to evaluate a FPGA design.

Systems Requirement Specification

This task involved the formal capture of all the system requirements, including the identification of the control system interface to the target and RF modules, and the definition of critical timing requirements for the system. The outcome of this task was an approved design specification to enable the design to continue. The role of the subcontractor was to assist in obtaining the functional requirements of the improved product, and detailing the performance and interface specifications.

Design

This task included several stages including:

High Level System Design

This task involved the design engineer, together with subcontractor support, in producing a system design using a behavioural VHDL programming style. The outcome of this task was to identify the functional requirements of the FPGA device, and consolidate the device knowledge gained during the training activity.

FPGA Design 1

The VHDL behavioural description was broken down into functional blocks and simulated to verify the functionality of the design. Once all the blocks simulated correctly then the design was integrated and a full functional test was performed on the design. A design netlist was produced when simulation results met the specification.

FPGA Design 2

This task involved the production of layout and routing solutions for the FPGA device. Several options were investigated to produce the most efficient design layout solution for the FPGA device after consideration of the timing requirements identified during the parallel simulation activity. The outcome was an FPGA design, and confirmed pin allocation for the device.

Timing Simulation

Using the layout data generated the timing delays associated to each node were back annotated to the design netlist. A simulation of the design with delays was then executed.

PCB Design

This task involved the use of printed circuit board (PCB) layout tools to produce a new PCB design for the improved equipment. The task was conducted after FPGA pin definitions had been confirmed. The outcome for this task was PCB design data to enable procurement of the PCB.

Test Strategy Design

This task involved the design and development of a test strategy for the FPGA and the improved equipment. The outcome of this task included the test procedures required for the FPGA and improved equipment, special-to-type test equipment needs and approvals testing.

Special to Type Test Equipment Design

This task involved the design and development of special purpose test rigs required to confirm the operation of the FPGA and the improved equipment, and was undertaken solely by the company engineer.. The outcome for the task was a complete set of drawings to facilitate the build of the test equipment.

FPGA Redesign

This task involved the incorporation of any necessary design amendments, including layout and routing changes, identified during the FPGA testing. This process was carried out by the First User alone and was conducted in parallel with the final FPGA Testing phase. The outcome for both tasks was a finalised FPGA design.

The subcontractor's role throughout the design phase was to provide design assistance. This included design assistance in partitioning of the original specification, capturing the design using VHDL, functional simulation, synthesising the code to a netlist and routing the FPGA. Particular effort was made in the areas of VHDL coding style for synthesis, constraint editing for routing, timing error reduction and floor-planning of the FPGA.

Evaluation and Test:

The evaluation task consisted of the following detailed stages:

PCB Build & Preliminary Test

This task involved the construction of the prototype equipment's PCB, and the testing of the populated PCB (less the FPGA) to eliminate any design or production errors on the PCB. The outcome of the task was a tested PCB to allow further FPGA integration testing.

Test Equipment Construction & Test

The outcome from this task was a tested special-to-purpose test rig to allow further equipment testing.

FPGA Testing

This task involved the use of standard test equipment (for example, logic analysers) and the special purpose test equipment to demonstrate that the functionality of the FPGA met the design requirements. The outcome for this task was a proven FPGA device.

Equipment Validation Testing

This task involved the final confirmation testing of the improved equipment under typical operating conditions. The outcome of the task was a field proven prototype equipment design.

Subcontractor assistance was provided in debugging the results of the timing simulation was provided to minimise the risk of design errors due to timing violations. A review of the draft test procedure for both the FPGA device and the entire product was also conducted by the subcontractor.

Technical Management

This task involved the selection of appropriate device technologies and the evaluation and purchase of the CAD support tools, as well as the project (cost, time and technical risk) management activities required to deliver the successful completion of the application experiment. The outcome of the task included the provision of FPGA CAD equipment, other resources and several iterations of management plans.

The workplan costs and programme milestones for the first iteration of the application experiment were as defined in Tables 1 and for the re-design iteration as in Table 2.

Workplan	Planned Days	Actual Days	Subcontractor Costs (KECU)
Training	10	12	2.2
Management	15	12	-
System Design	25	24	2.5
FPGA Design	35	47	9.93
PCB Design and Construction	12	14	-
Test and Evaluation	39	37	1.8
TOTAL	136	146	16.43

Table 1 – Workplan definition (person days)

The major cause of the additional times required to complete the design task when compared to the original estimate was the difficulties identified in working with the CAD tools. These included the reversion to different default settings if precise care was not taken, and the time required identifying the cause of these ‘faults’, even with the assistance of the design subcontractor in resolving these issues.

A redesign of the radio encoding part of the project was required due to a problem becoming apparent with the existing equipment in service exhibiting faults when located within an indoor range and less than 1 meter from a steel venetian bullet trap. This was shown to be caused by the sampling and encoding method previously employed and multi path effects. A new timing and sampling system was evaluated and proved be reliable in such conditions. The entire re-design took approximately one month to complete, including the redesign of the circuit board to ensure that further iterations were not unduly restricted by pin locking at this stage, as the circuit board had not been manufactured yet. The resources required to complete this design modification is identified below:

Workplan	Redesign Iteration
Management	1
System Design	4
FPGA Design	12
PCB Design and Construction	5
Test and Evaluation	5

Table 2 – Re-design Workplan (person days)

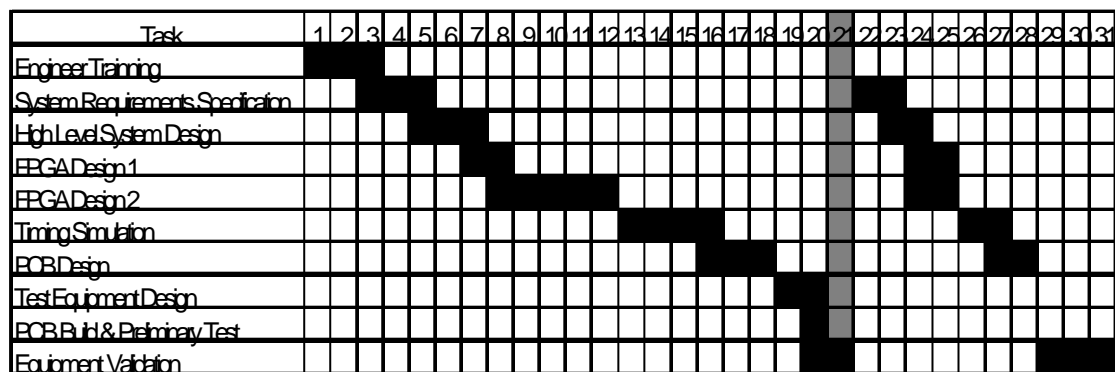


Figure 5: Actual and Planned work Programme

The actual workplan adopted indicates the design iteration required to resolve the communications problems identified in initial testing. Until this time (indicated by the vertical shaded bar in the work plan of Figure 5), the programme of work was as per plan. The design iteration extended the completion of the application experiment slightly, but not in the same degree as would have been required for a hard wired, discrete technology solution.

The re-design which was required towards the end of the experiment proved that the knowledge and skills transfer had been carried out very effectively.

11. Subcontractor information

Militec selected a local training and support provider, the Centre for Electronic Product Engineering (CEPE) as its preferred subcontractor.

Factors that influenced the selection of the subcontractor included:

- **Locality:** as a very small company demands on the business demanded a high responsiveness if problems were encountered with the technology. This meant that a local FPGA training supplier was required. Given the geographic position of the company this reduced the number of eligible subcontractors significantly.

- Previous experience in the design and development of electronic systems using CPLD and FPGA device technologies. This is crucial, as the nuances of the development tools are potentially a significant learning curve for the company to assimilate.
- Availability of the same CAD tools as were procured by the company. The subcontractor, CEPE, was a wide range of workstations and PC based CAD facilities and FPGA development systems from most FPGA vendors. This factor was important in the selection process as demonstrating the potential for a range of experiences to be provided to support the company during the application experiment.
- Independent qualification of the subcontractor's expertise (in this case as a recognised Regional Centre of Expertise in Electronic Product Engineering by regional and national government agencies and departments).
- Their commercial impartiality.
- Their previous training experience, which offered good knowledge transfer prospects.

As a minimum requirement for the selection of the sub-contractor, the following were regarded as being of major importance:

- Current experience in the application, and real world use, of the technology to be utilised.
- Proven track record in keeping within budget and time scales agreed at the outset.
- Willingness to provide evidence of previous undertaking and satisfied customers
- Due to the nature of information transfer it was also considered important that both parties could work together and share information and expertise.

The subcontract identified one final payment for the satisfactory performance of the identified training, and design support roles. The Intellectual Property Rights (IPR) were identified as residing with the subcontractor. As the subcontract required payment at the end of the application experiment the company did not request a penalty clause in the subcontract, viewing the retention of payment as a sufficient mechanism for ensuring sub-contractor performance.

12. Barriers

Militec were very experienced players in the target equipment market, and had a wide range of skills in this technologically intensive area. However, the company is very small in terms of personnel, and as such there were a number of barriers that were perceived:

1. Lack of knowledge of FPGA technology. Not only did FPGAs represent a change in technology from the point of view of manufacture and test, but more importantly, from the viewpoint of design. In such a small company virtually its whole design resource had to be committed to the AE. It was therefore essential that the technology transfer was successful.
2. Fear of change. The reputation of the company was established on conventional technology which worked and was understood. Any problems with a change in technology would have serious repercussions, particularly in view of the world-wide customer base and the difficulty of attending to the equipment once it was in the field..

3. Fear of Commercial Risk. For the reasons above, the very existence of the company was at stake if the AE failed. The incentive to change had to be balanced against the risk of losing everything.
4. Retrospective compatibility. The existing products, although they had a number of variations to suit individual customers' needs were essentially variations on a few basic designs. It was highly desirable that these should be able to be upgraded to take advantage of the FPGA technology.
5. Competitive position. There was a perception that since some of the competition was from multi-national companies, the niche market enjoyed by the first user could only be sustained by maintaining maximum flexibility. It was by no means immediately appreciated that the means of achieving cost reductions in manufacturing could also be the means of improving flexibility and speed of design changes.

13. Steps taken to overcome barriers and arrive at an improved product

Militec were conversant with traditional analogue and digital electronics but were not conversant or familiar with FPGA technology. As part of the feasibility study required to put the proposal together, Militec had to liaise with the TTN and design subcontractor CEPE to be able to understand how FPGA technology could benefit their products. This process continued throughout the AE, thus transferring knowledge directly into Militec. A by-product of this knowledge transfer exercise was that Militec developed the confidence not only to maintain the revised FPGA-based products, but also to carry out new FPGA designs without the need to resort to subcontractors.

Fear of change can be difficult to overcome, as it is a psychological barrier in essence. Militec concentrated their minds to embrace change, as the company realised that it could only regain a competitive position in the market place, particularly the USA, by taking cost out of the product. A step-change in technology was required, and this very requirement helped to reduce the fear of change. Militec felt reassured in that they will had the full support of the TTN and the design subcontractor, throughout the duration of the experiment.

The cost savings available by introducing FPGA technology made the analysis of the payback calculation fairly attractive. This in itself ought to be sufficient cause for companies to adopt new technology, but often it is not the case. Companies need that helping hand to lead them through the sometimes-difficult maze of technology transfer. This is where the role of the TTN played a vital part in the equation. By providing high quality, impartial advice based on experience, the TTN provided both help and confidence to Militec to understand and get to grips with the process of technology transfer, and thus allow Militec to manage and minimise the commercial risks.

14. Knowledge and experience acquired

The knowledge development goals of the application experiment were to allow Militec Ltd to gain knowledge and expertise in the specification, design and evaluation of the FPGA-based product.

The knowledge development goals were to establish an independent capability to enable the:

- Technical and project management of FPGA-based designs.
- Selection of FPGA device technologies for integrating digital circuits.
- Apply top-down design methodologies.

- Use the FPGA CAD system for design capture (schematics and VHDL), digital simulation, logic synthesis, test pattern generation and fault simulation.
- Ensure the correct placement and routing of FPGA devices, based on a knowledge of speed-area trade-offs.

At the end of the application experiment the company had gained knowledge in all of these areas successfully.

This application experiment allowed Militec Ltd to gain for the first time knowledge in using modern microelectronics technologies to integrate the electronic circuitry in its other turning target products. The technical management skills and the design expertise resulted in a clear increment in the company's electronic design capabilities. This provided Militec Ltd with the ability to develop more versatile and lower cost products in the future. This application experiment allowed the company to overcome a major technological barrier which will enable future products to attack new markets, especially those requiring more complex functionality, lower power consumption and cheaper to manufacture.

15. Lessons Learned

Once over the initial problems of learning the basics of a new programming language and system the majority of the problems encountered were due unfamiliarity with the working environment and subtleties within it. There included:

1. Syntax errors and unfamiliarity with the programming environment. The importance of simulation was highlighted by the introduction of such errors, some of which were not detected by the entry tool.
2. Incorrect driving of the simulator, driving input isolates all other parts of the net.
3. Difficulty in reverting to default setting have altered constraints and settings. The importance of ensuring the correct default settings for the design tools before use was quickly noted.
4. Bugs / inaccuracies with the software its self. The vendor of the development tool advised that many of the 'errors' reported were due to the version being used. The importance of identifying some form of software maintenance to obtain the upgraded (corrected) software should be noted.
5. Support and licence files for the software. A formal process for recording this information should be defined, as the company experienced problems when the information related to the purchased tools was recorder incorrectly, thereby affecting the update configurations.
6. Ensuring good design practice was used highlighted the tendency to incorporate asynchronous logic into the design solution.
7. Easy at which, when using design wizards, check blocks can be omitted. Some basic checking of the results of the use of such support facilities should be undertaken.
8. The documentation provided by the supplier for circuit board layout and download procedures was poor. Therefore, the company has learned that close contact with the subcontractor and FPGA manufacturer should be maintained for better information transfer.

The company has already learned of the benefits in terms of reduced stocking costs because of the reduced number of components to be applied in the improved product. An additional lesson has

been the recognition of the benefits of alternative programmable logic devices (PALs) in other simpler application areas as a result of applying the programmable FPGA technology to yield similar benefits. These lessons indicate that further utilisation of this technology is guaranteed due to its flexibility and ability to reduce both cost and size of the final unit while increasing reliability.

The benefits of the technology in allowing compensation of system under-performance by enabling digital compensation to be incorporated within the FPGA device was also an important lesson learned by the company. In the particular problem faced during the application experiment the company was able to improve the performance of its RF system by incorporating design changes in the FPGA device to implement new sampling, frequency and mark / space ratio adjustments to optimise the RF system performance.

One very major advantage of the use of FPGA technology is its ability for the functionality of the circuit to be greatly altered with out the necessity of a new PCB. As can be seen from this project a late change in the specification of what is in effect a major part of the design could be incorporated and effectively only delayed the entire project by about 1 month. If this project had been implemented using the old style technology then a large proportion of the work completed would be scraped and the project delayed by about 3 months with any PCB work done becoming useless. This re-design phase was in effect arguably the first internal replication exercise carried out by the First User.

16. Resulting product or process, industrialisation and internal replication

A working prototype has been completed, and is operational. The stages required to transfer this prototype into full production include:

- Finalisation of field trials, and the collation and full evaluation of customer comments. This information should be available in 1-2 months time.
- Incorporation of customer requests for modifications. This task will be accommodated without any circuit board layout changes by the use of the redevelopment of the FPGA device. This task will be conducted entirely using company engineering resources; no input from subcontractors are expected to be required. This task is estimated to require 12 weeks (maximum) to complete.
- Formal evaluations, including EMC testing (2 weeks)
- The production of final production drawings, related documents, tooling, and marketing information (6 weeks).

The complete industrialisation process is expected to require 5 months to complete, as some of the above tasks can be conducted in parallel.

Once the pre-production units have been tested locally they are to be loaned to existing customers for their appraisal and comments. This involves shipping to various countries around the world, with the associated costs and licences, at Militec's expense.

The use of pre-compliance equipment for EMC testing and the attention in the design stages means that the EMC costs are anticipated as 2.5 KECU. Tooling set up costs were approximately 4.5 KECU.

The final costs of industrialisation and product launch will depend largely upon the alterations requested by customers during field trials. However, based on previous experience and the

shortened iteration times enabled by the more flexible FPGA technology, the costs of the design revision and drawing upgrade se stages is anticipated to be less than 7.5 KECU.

The total cost of the industrialisation process is therefore approximately 14.5 KECU.

The company has already considered the use of this technology in other application areas. As a direct result of this project a series of position sensing circuit boards has been re designed into one using a single PAL, and by the use of 4 links replaces three different boards and two variants of one. This has already shown in a reduction in stocking cost and reduction in component costs due to purchasing one component in larger volume as opposed to small quantities of different components.

17. Economic impact and improvement in competitive position

A significant advantage in introducing FPGA technology to the Militec range of products is that of cost reduction. The following table shows the estimated reduction in the material and assembly (i.e. labour) costs on the company’s existing and improved products:

	Existing Unit Cost (normalised)	Improved Product Unit Cost (relative)
PX180 Target Turner	100	69
PX536 Pop up Target	100	78
Moving Target System	100	88

Table 3: Cost Savings of Improved Product Relative to Existing Products

Therefore the percentage savings by introducing FPGA technology range from 12% for the moving target system through to 31% for the PX180 Target Turner. This substantial reduction in the manufacturing costs will enable Militec to offer target equipment at very competitive prices. This will allow Militec to make significant inroads particularly into the US market, where the company is currently at a price disadvantage compared to the competition.

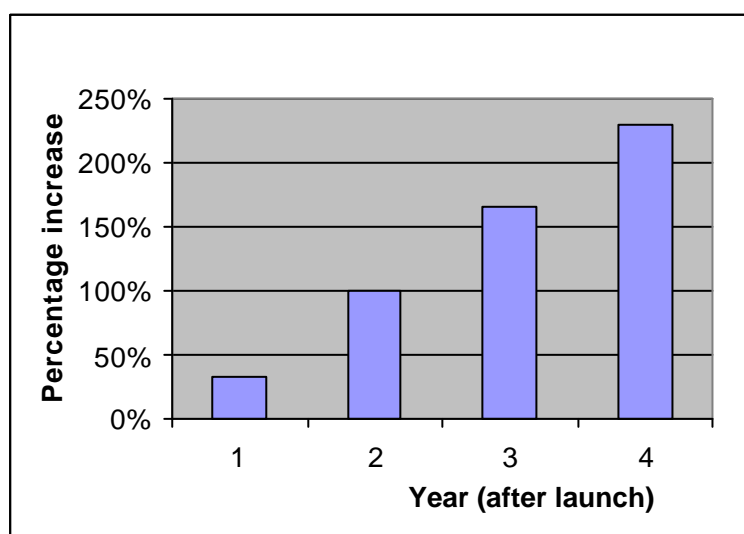


Figure 6: PX180 additional sales (units relative to 1996)

Taking the base level 1996 figures, the impact on sales in terms of units and revenue is illustrated in Figures 6 and 7. Figure 7 indicates that without the product improvement a slow decline in sales levels would have been experienced.

Given an investment in the FUSE Application Experiment of 48 KECU, payback is achieved in slightly over 8 months. This equates to a return on investment of 882% during the 6 year product life over the 6 year life before product re-design will be undertaken. These commercial benefits are achieved because the modular FPGA based design solution allows the FPGA technology to be incorporated into 2 products simultaneously (the PX 536 unit as well as the PX 180).

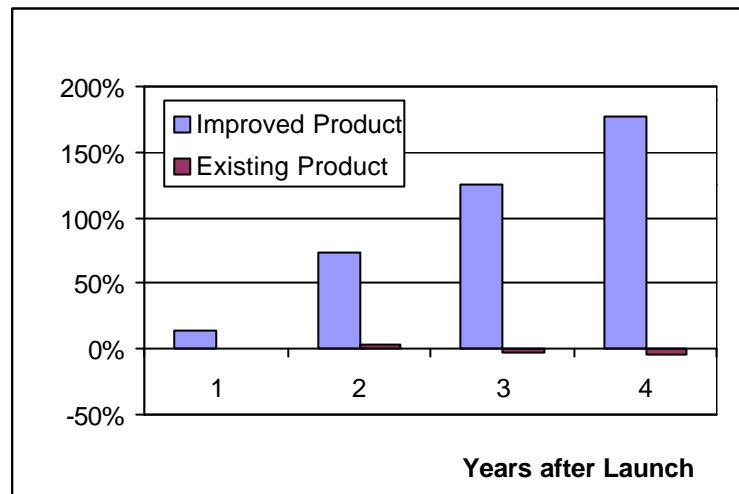


Figure 7: Increase in sales revenue

18. Best Practice and Target Audience

This application experiment demonstrates best practice in the areas of high level systems design, appropriate design routes (schematic and VHDL) for functional blocks, design flexibility enabled by the FPGA device technology and in the area of cost benefits derived from the use of this technology.

The cost savings, reduction in circuit board numbers, and improvements in system performance made available by the use of FPGA device technology will be of interest to a wide range of organisations including the following:

- Companies in the electro-mechanical manufacturing sector looking to cost reduce their products.
- Companies who use electronic modules in their products, containing discrete analogue and digital circuitry.
- Small companies who may think that the transition to microelectronics is beyond their resources (Militec have only four employees).
- Small companies who compete in a global market and who have to stay competitive with the best.
- Companies whose products need to be able to be adjusted or updated in the field.
- Companies who need to enhance the features of their products, but anticipate having to do so again in the near future.

Companies in industry sectors defined by the following NACE codes will therefore benefit: 2956, 3162, 3320, 3330, 3550.